Adam Baird (s.a.baird@rl.ac.uk)
Rutherford Appleton Laboratory

Status of Calice ECAL Readout Board.

17 March 2003

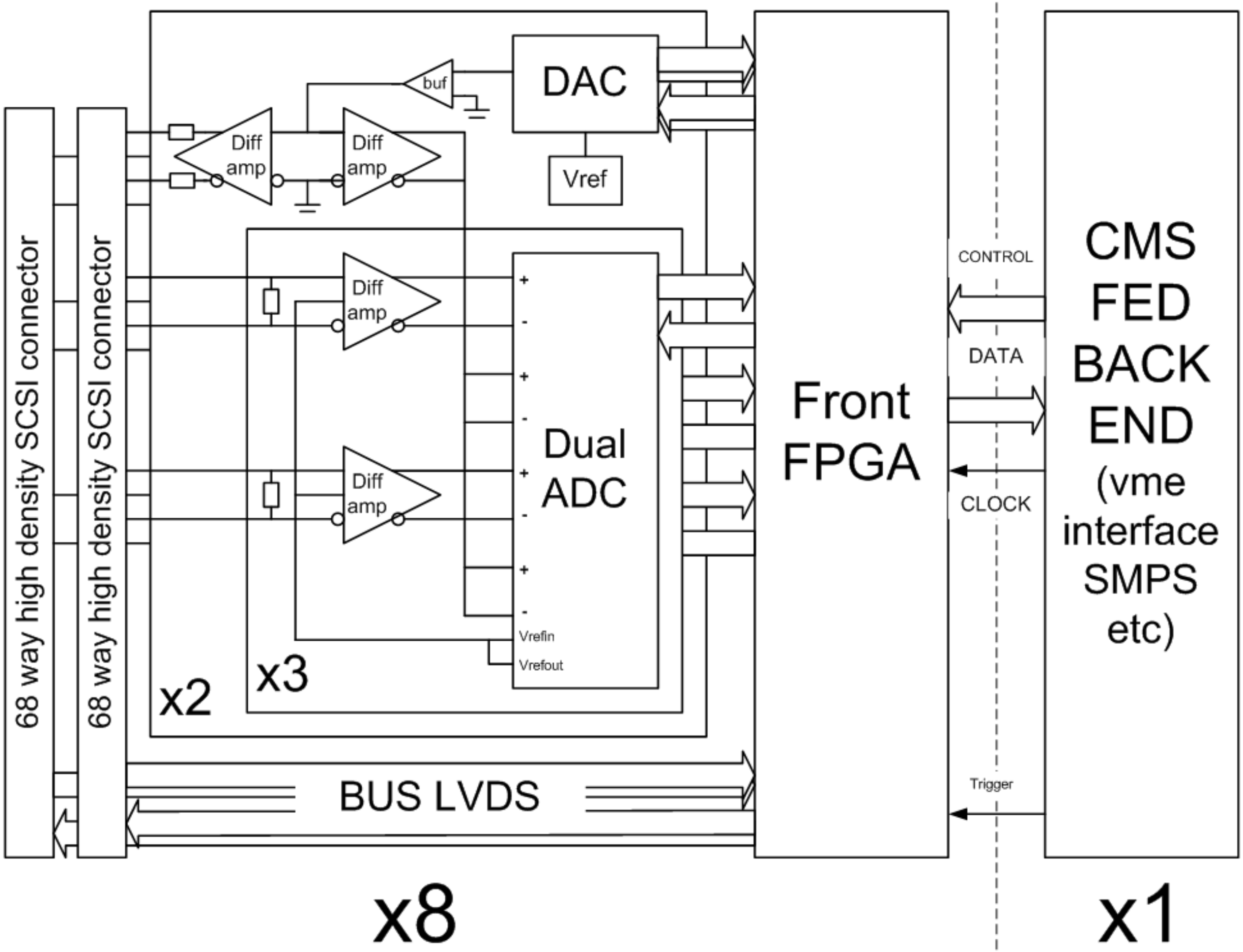
Circuit diagrams must be printed A3 to view fine detail.

This file is printed best when printer is set to "flip on short edge"

This version of the acrobate file is for printing. Some text is missing from the diagrams, which is present in the screen version.

notes

Block Diagram of Calice ECAL Readout board



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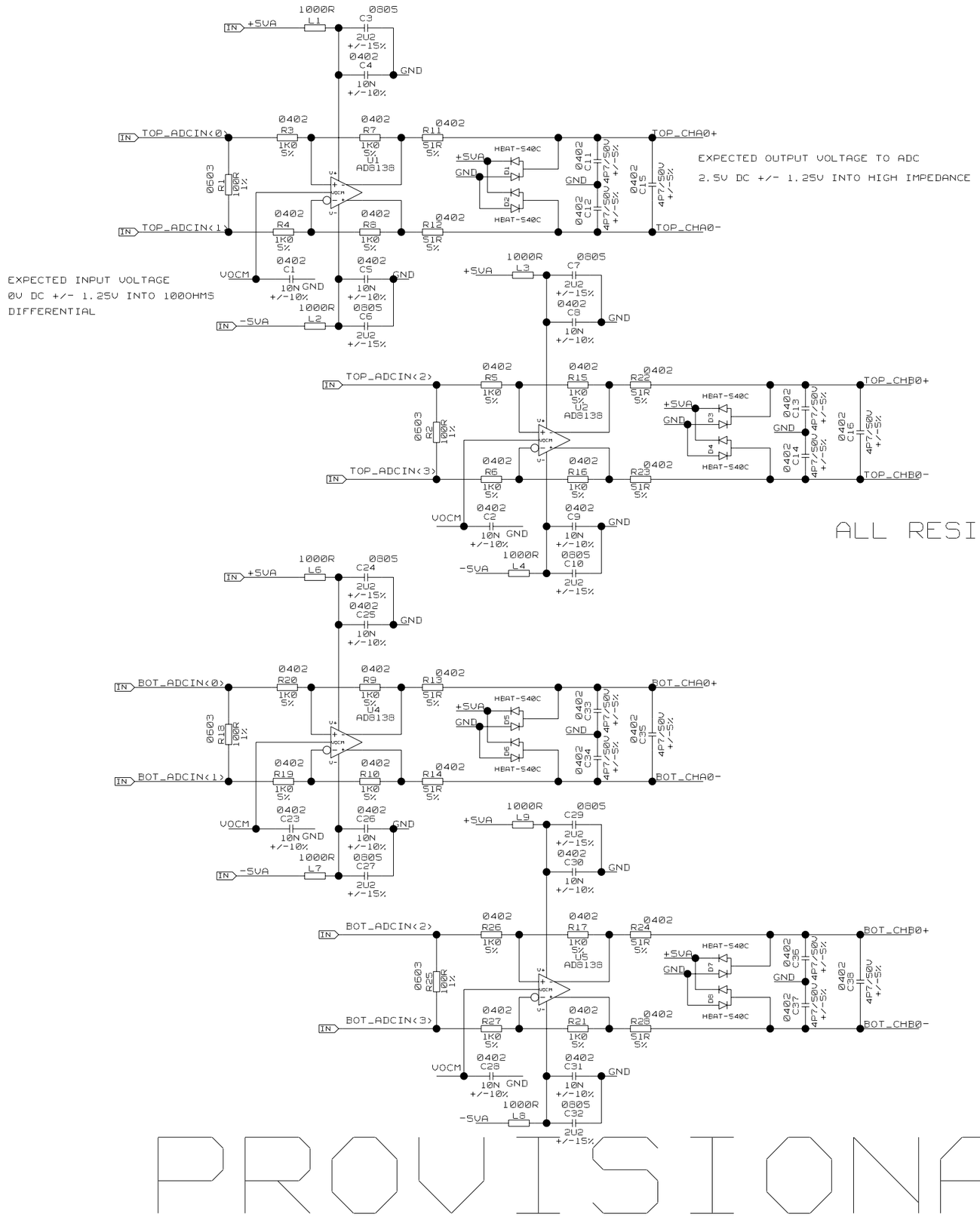
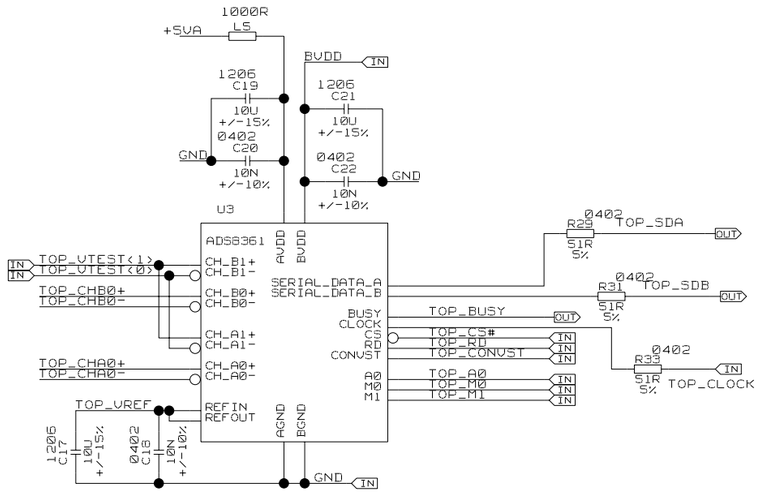
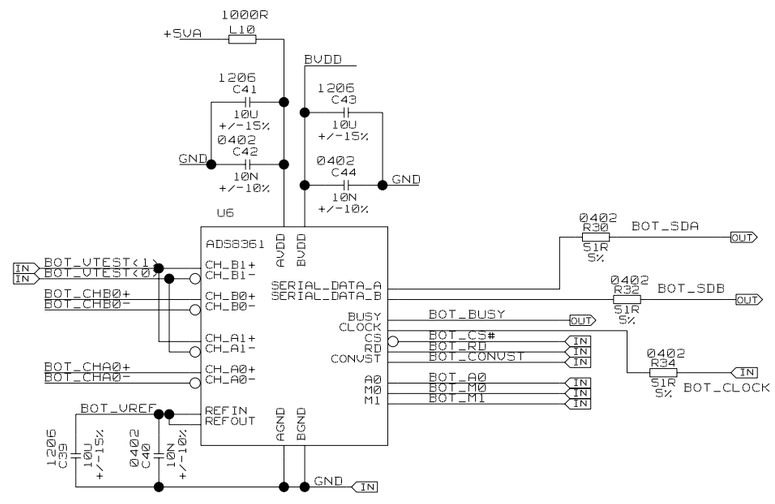






ALL RESISTORS MUST BE CHANGED TO 1% TOLERANCE

PROVISIONAL

ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

USED ON

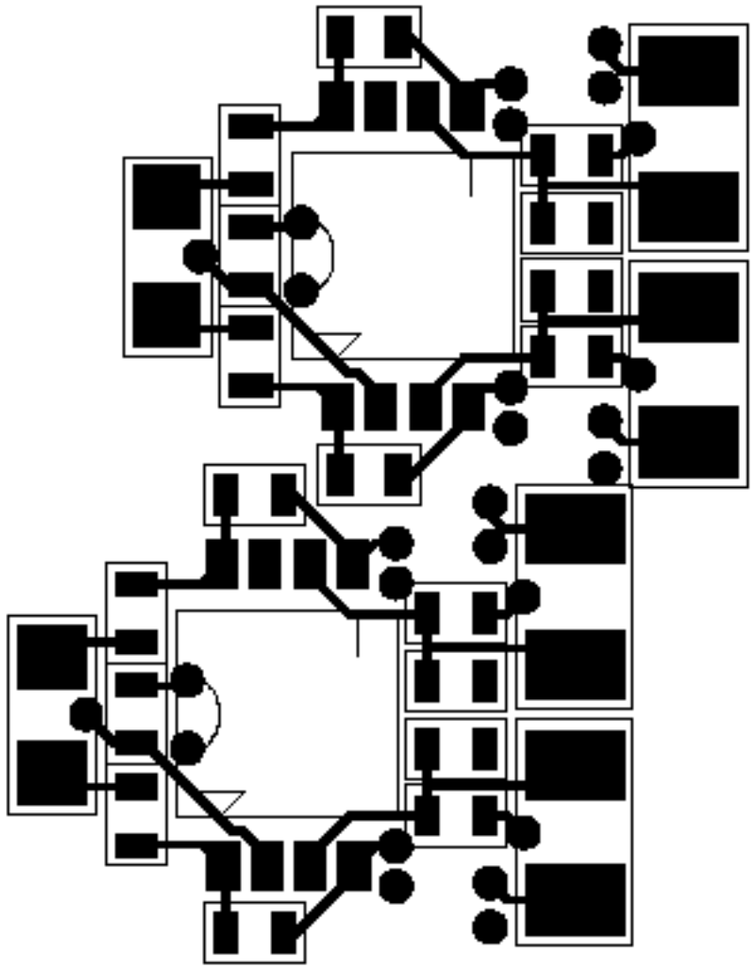
CCLRC
COUNCIL FOR THE CENTRAL LABORATORY OF THE RESEARCH COUNCILS
RUTHERFORD APPLETON LABORATORY, CHILTON, OXON OX11 0QX.

TITLE

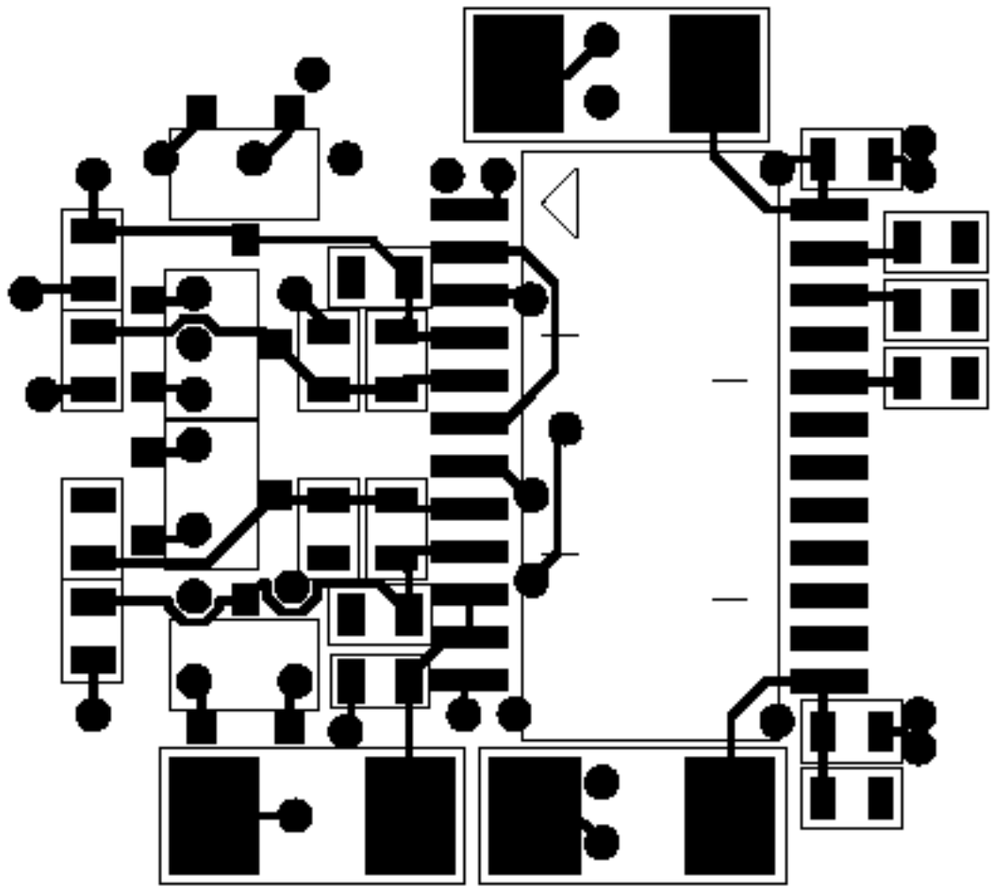
CALICE ADC DESIGN

A2

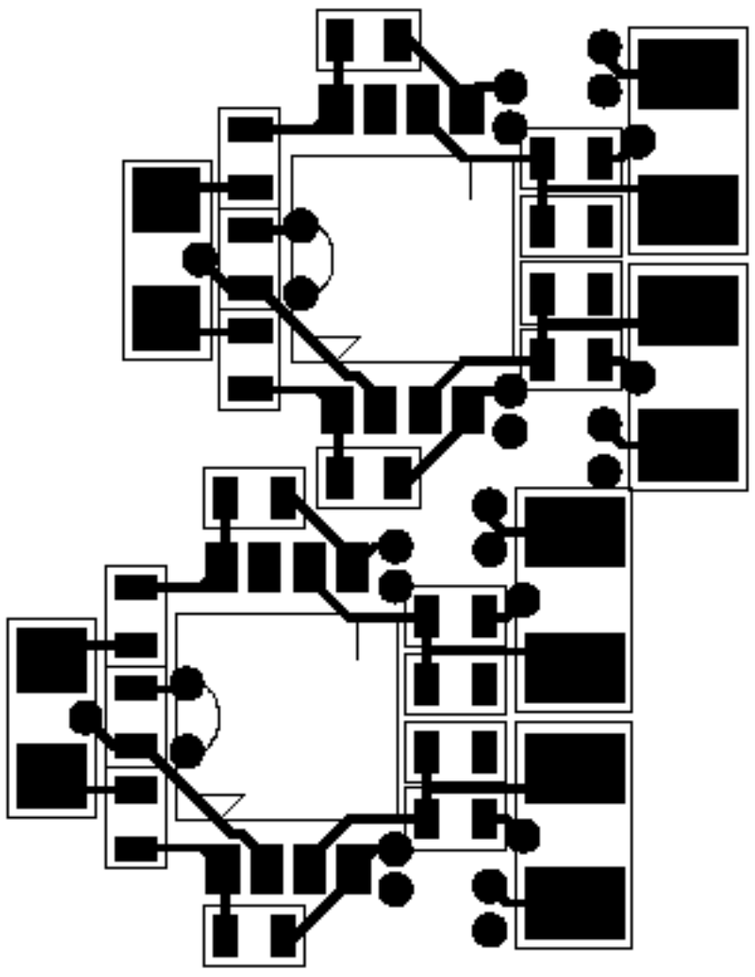
TOTAL NO. OF SHEETS



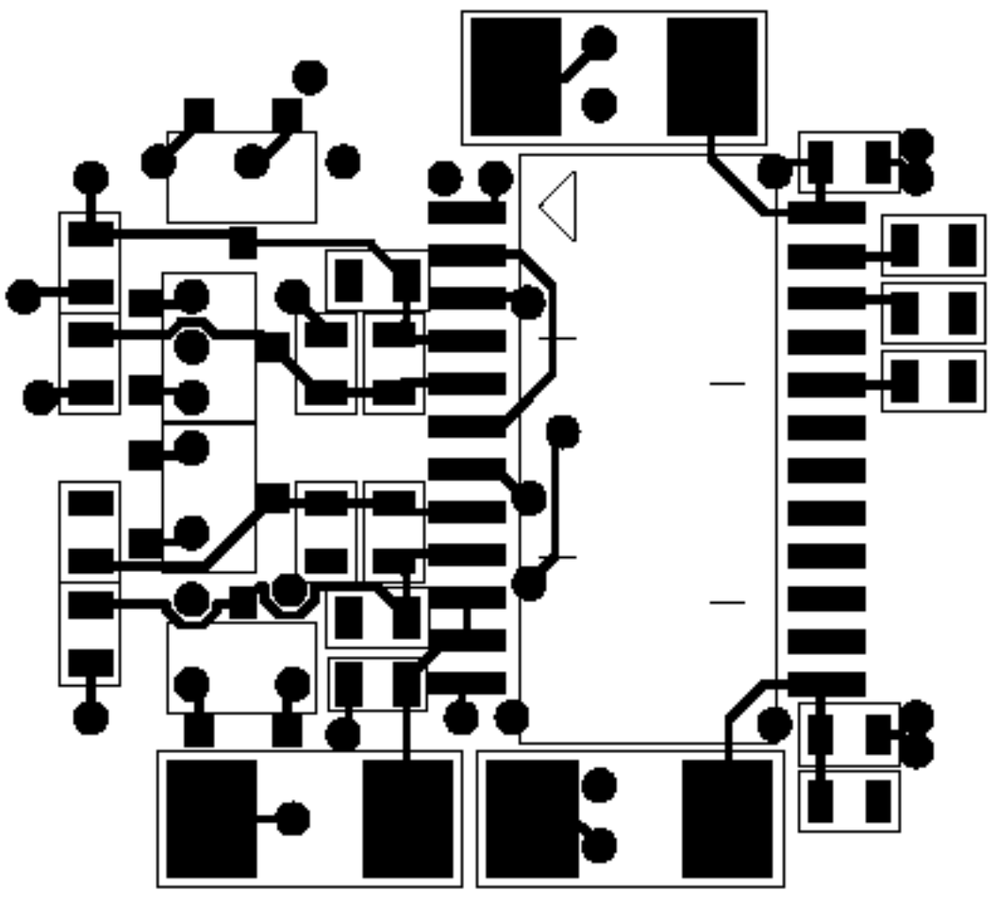
Top view
<-- dual pre-amp
and
dual ADC -->



ADC Module

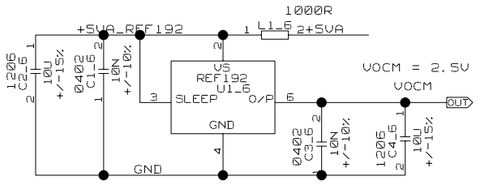


Bottom view
<-- dual pre-amp
and
dual ADC -->

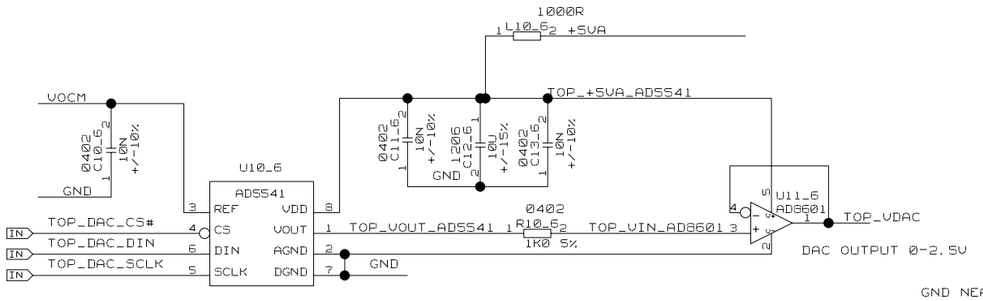


A	2	THIS DRAWING CONFORMS TO B.S. 3939

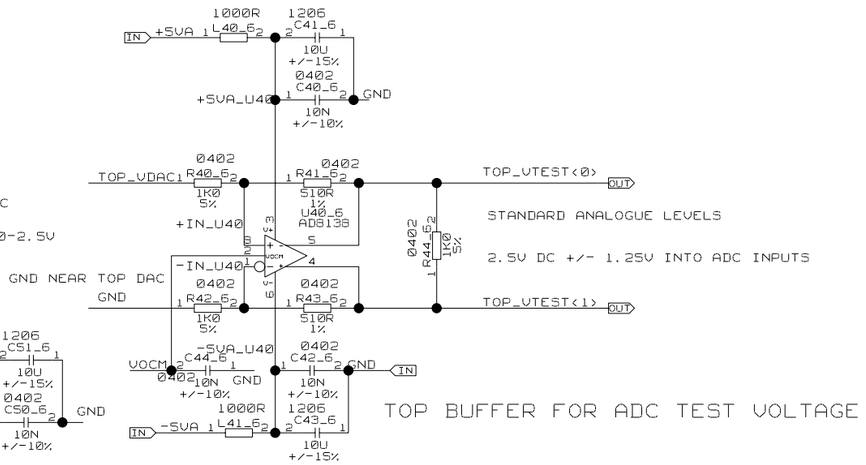
VOLTAGE REFERENCE



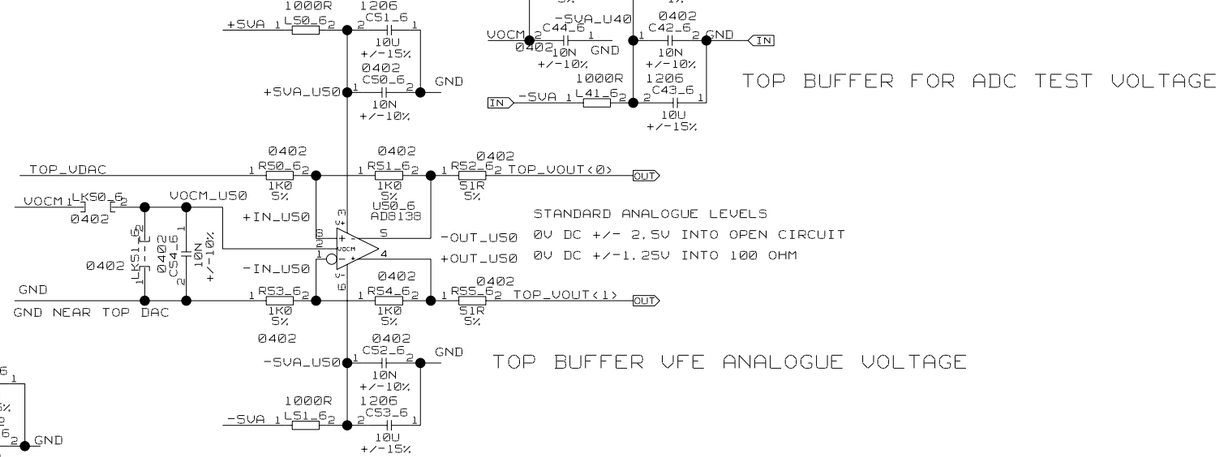
TOP DAC



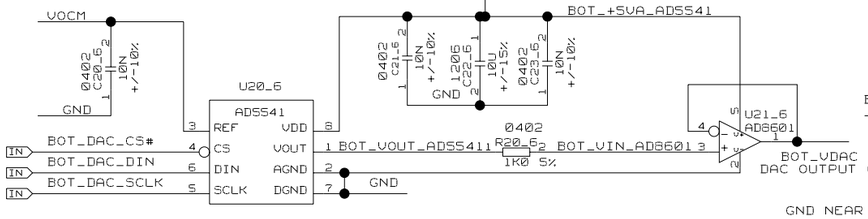
TOP BUFFER FOR ADC TEST VOLTAGE



TOP BUFFER VFE ANALOGUE VOLTAGE



BOT DAC



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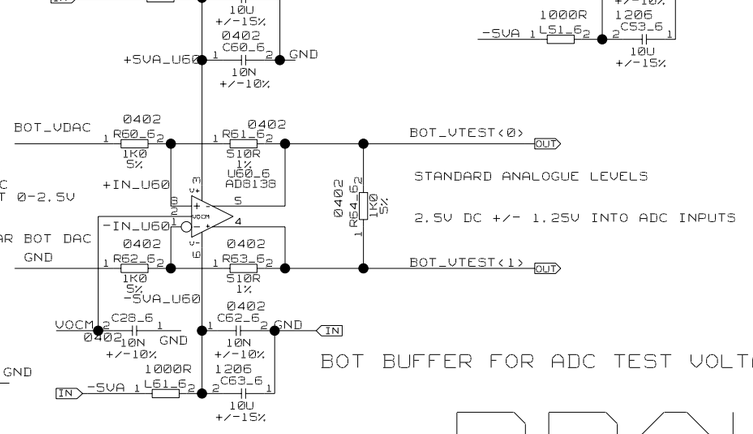
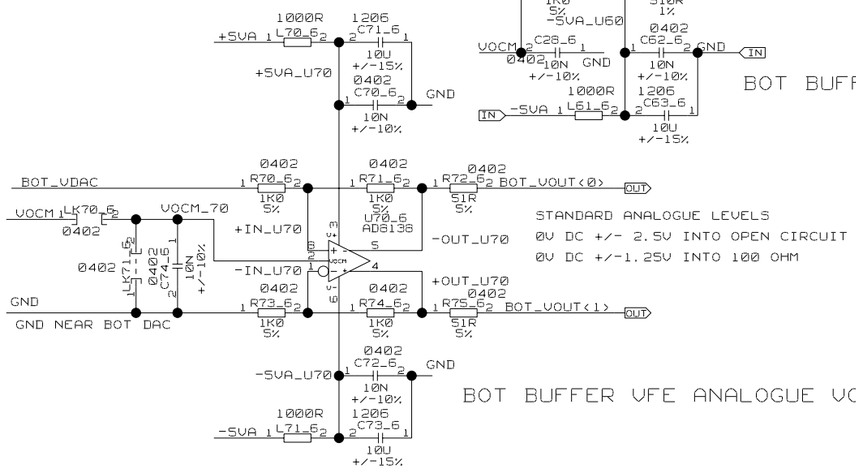


BOT BUFFER VFE ANALOGUE VOLTAGE



PROVISIONAL

ALL RESISTORS SHOULD BE CHANGED TO 1% TOLERANCE

ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

USED ON

CCLRC
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RUTHERFORD APPLETON LABORATORY, CHILTON, OXON OX11 0QX.

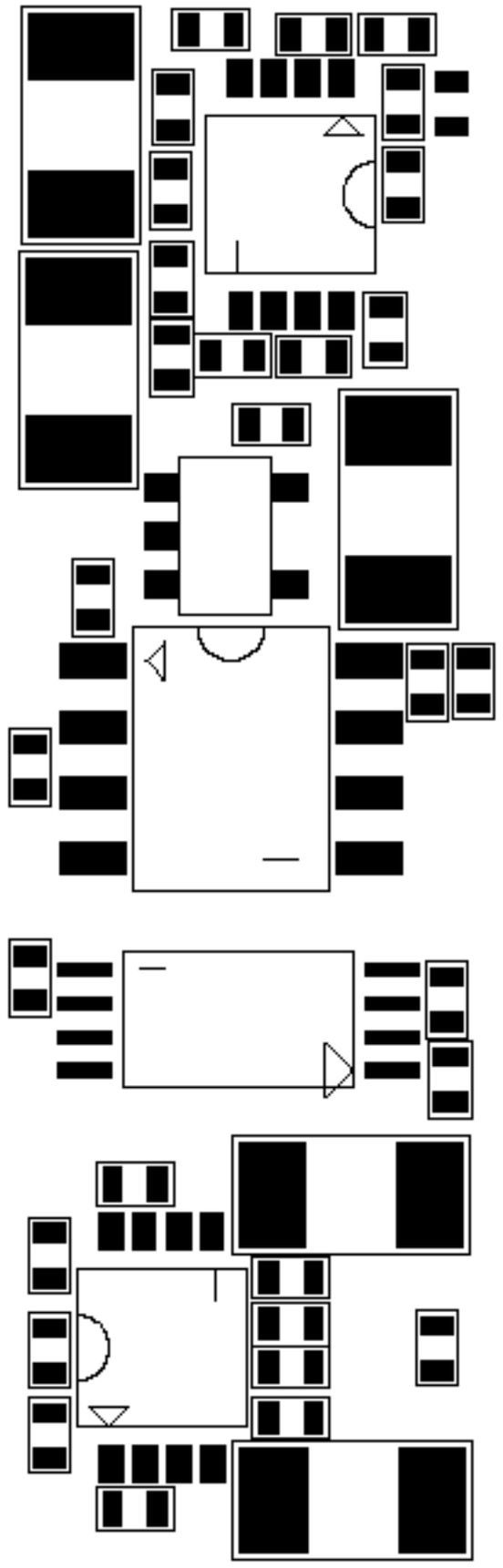
TITLE

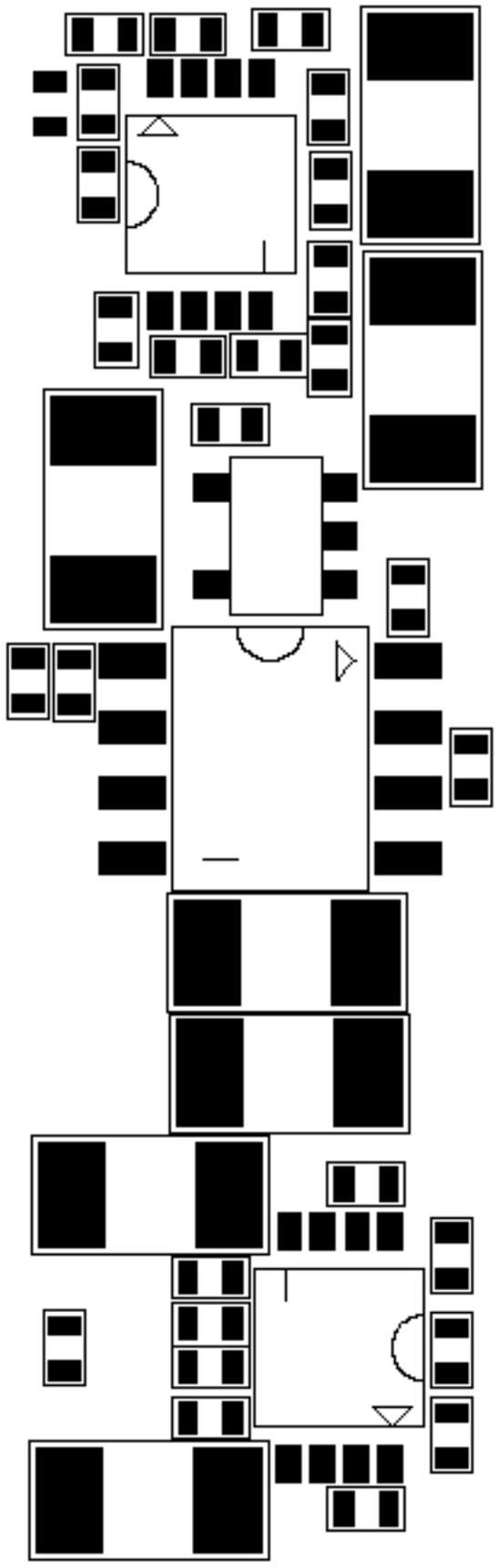
CALICE DAC DESIGN

A2

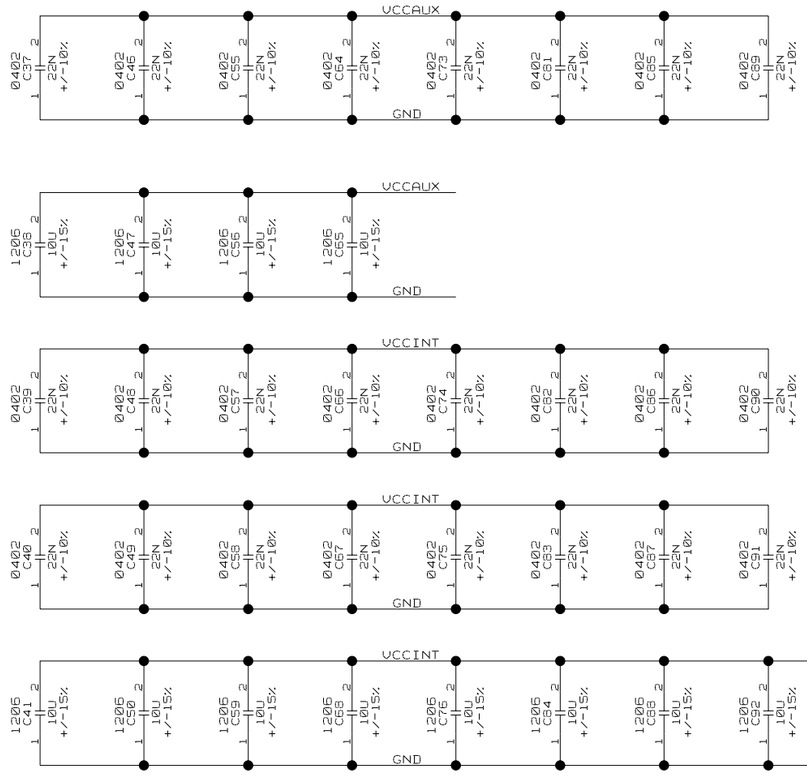
TOTAL NO. OF SHEETS

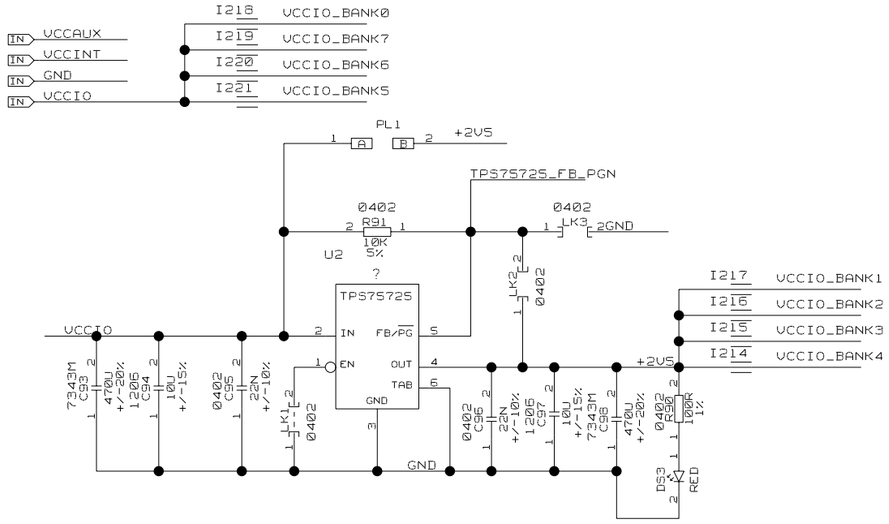
DAC Module
top view left
bottom view right



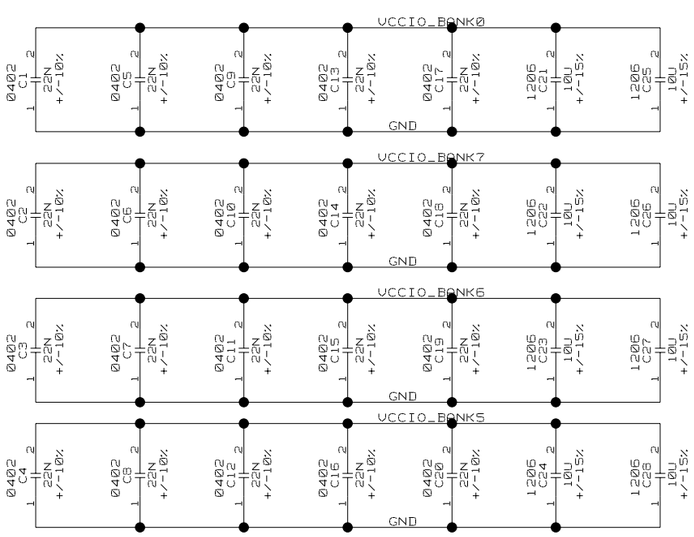


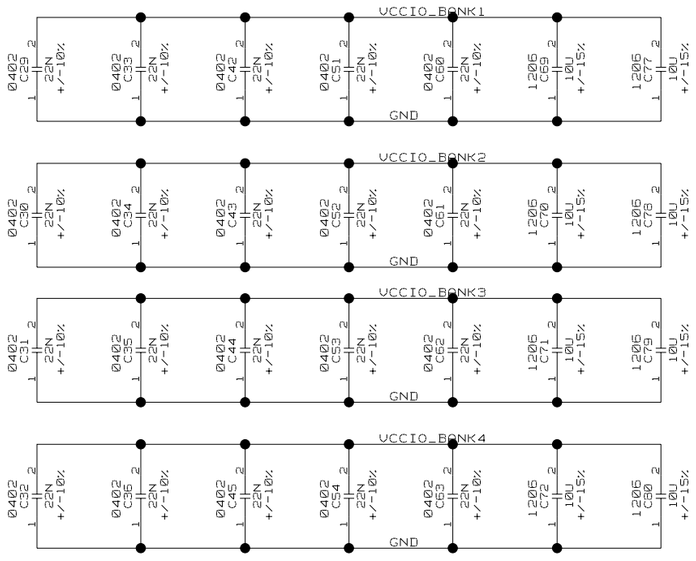
A2 | THIS DRAWING CONFORMS TO B.S. 3939





PROVISIONAL





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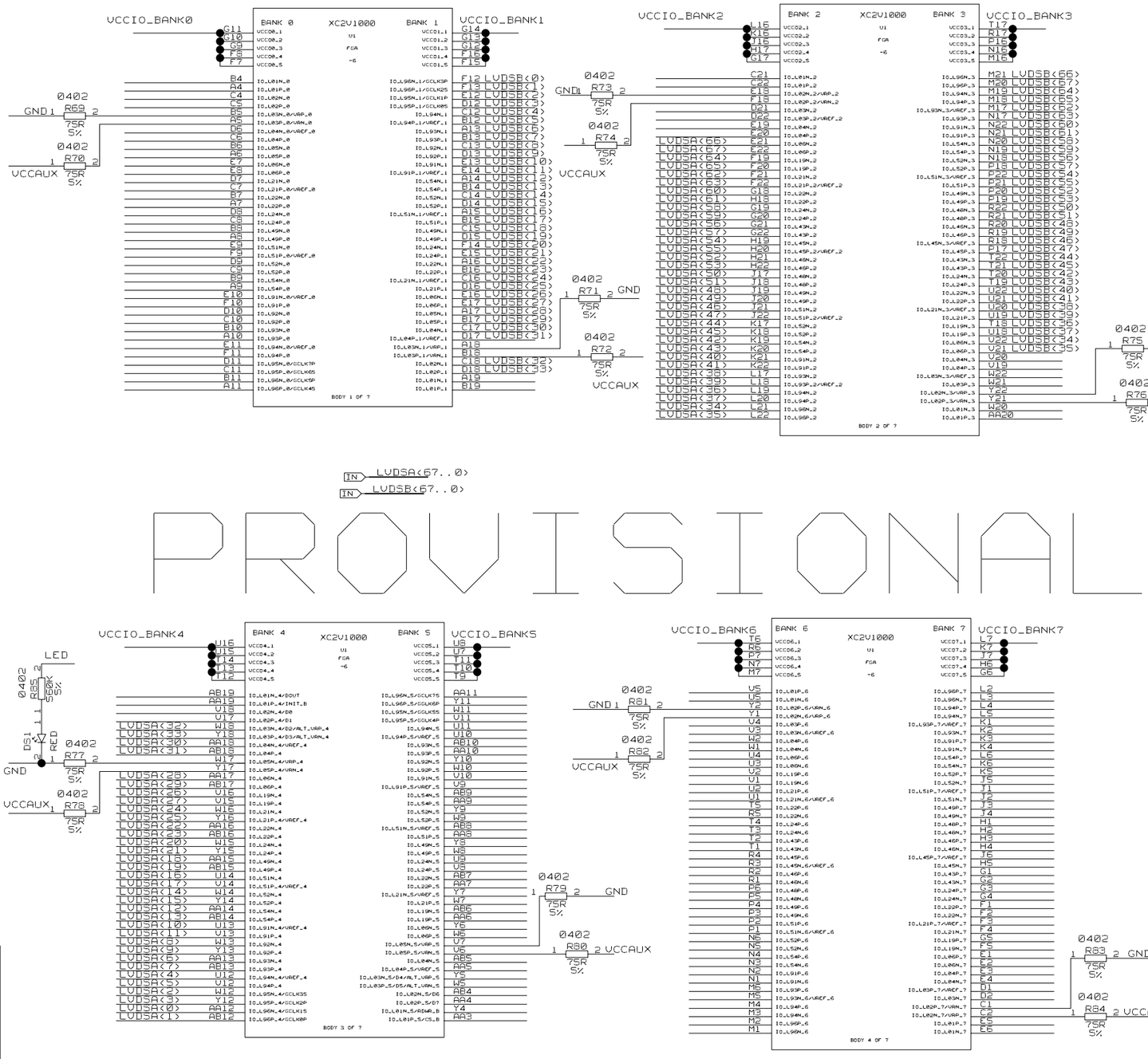
TITLE

FPGA DECOUPLING AND 2V5 LVDS VCCIO PSU

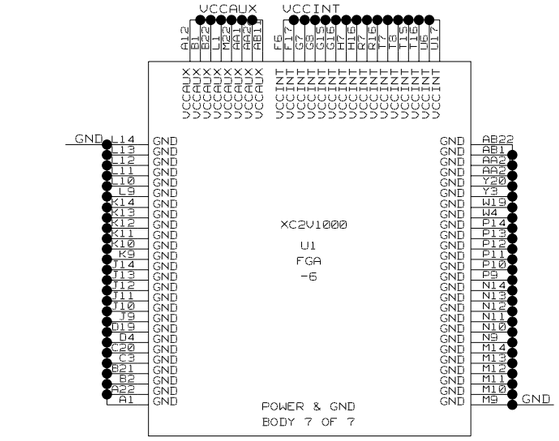
A2

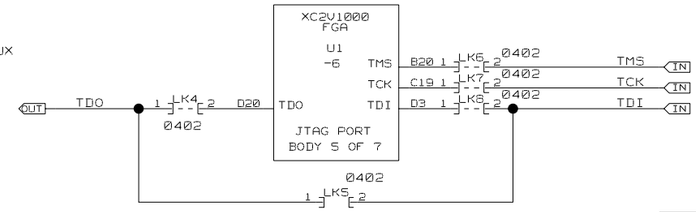
TOTAL NO. OF SHEETS

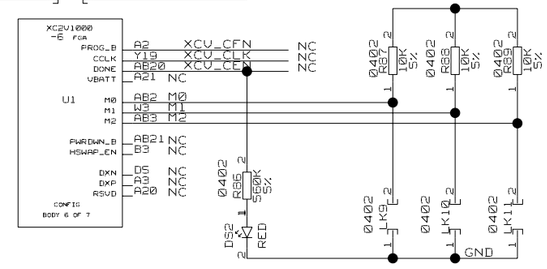
A 2 | THIS DRAWING CONFORMS TO B.S. 3939



PROVISIONAL







ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

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CCLRC
COUNCIL FOR THE CENTRAL LABORATORY OF THE RESEARCH COUNCILS

RUTHERFORD APPLETON LABORATORY, CHILTON, OXON OX11 0QX.

TITLE

FRONT FPGA

A2

TOTAL NO. OF SHEETS

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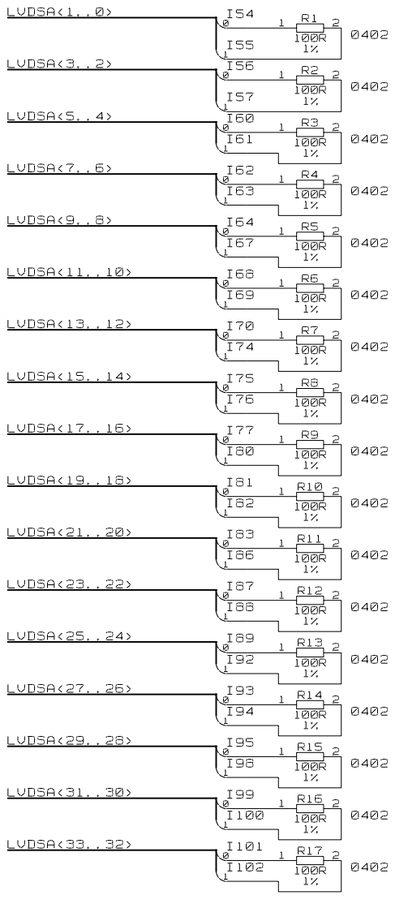

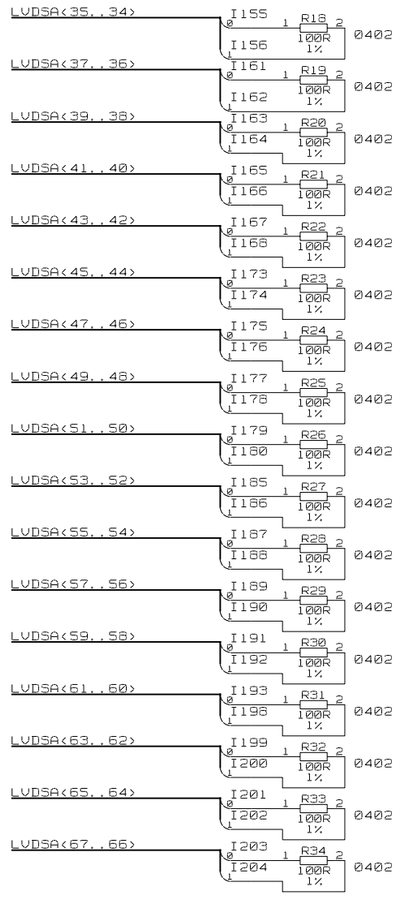

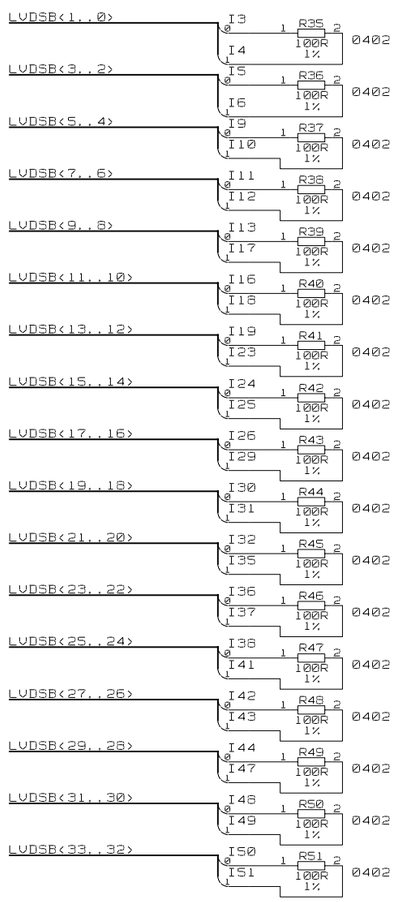

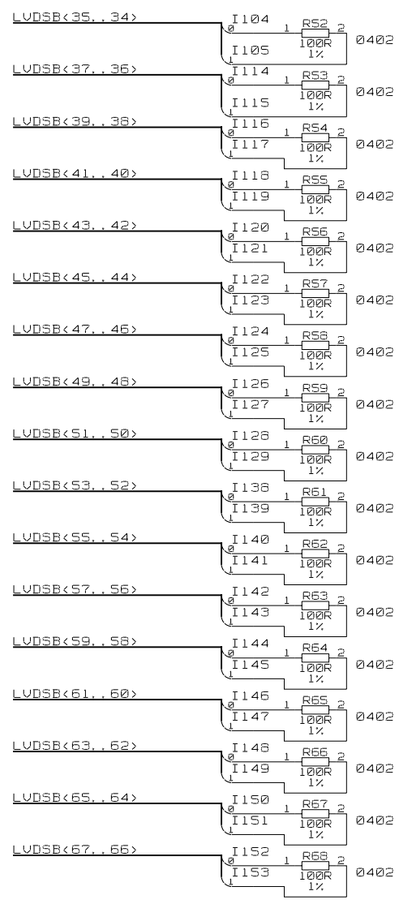

PROVISIONAL

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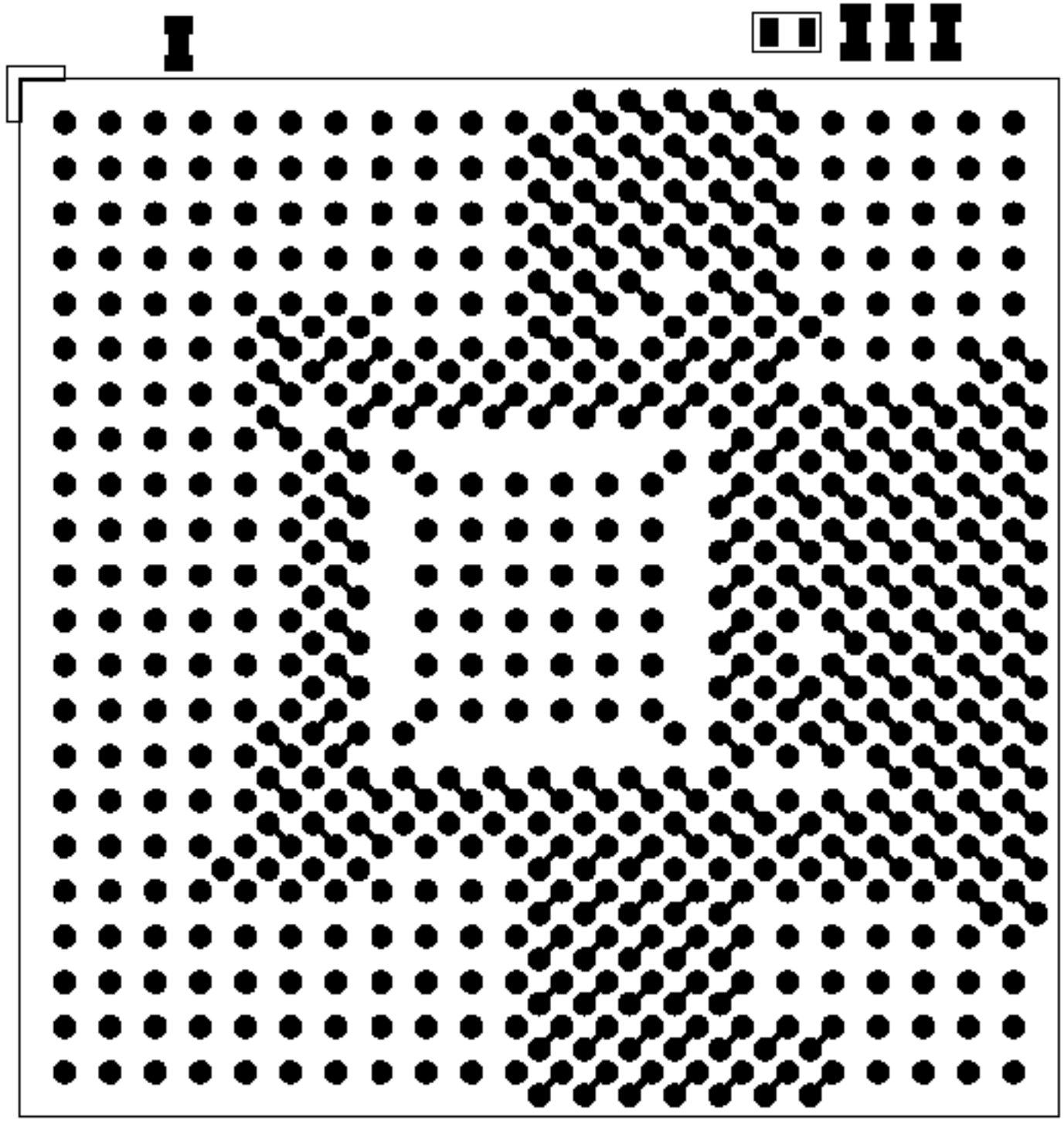
TITLE

LVDS TERMINATIONS

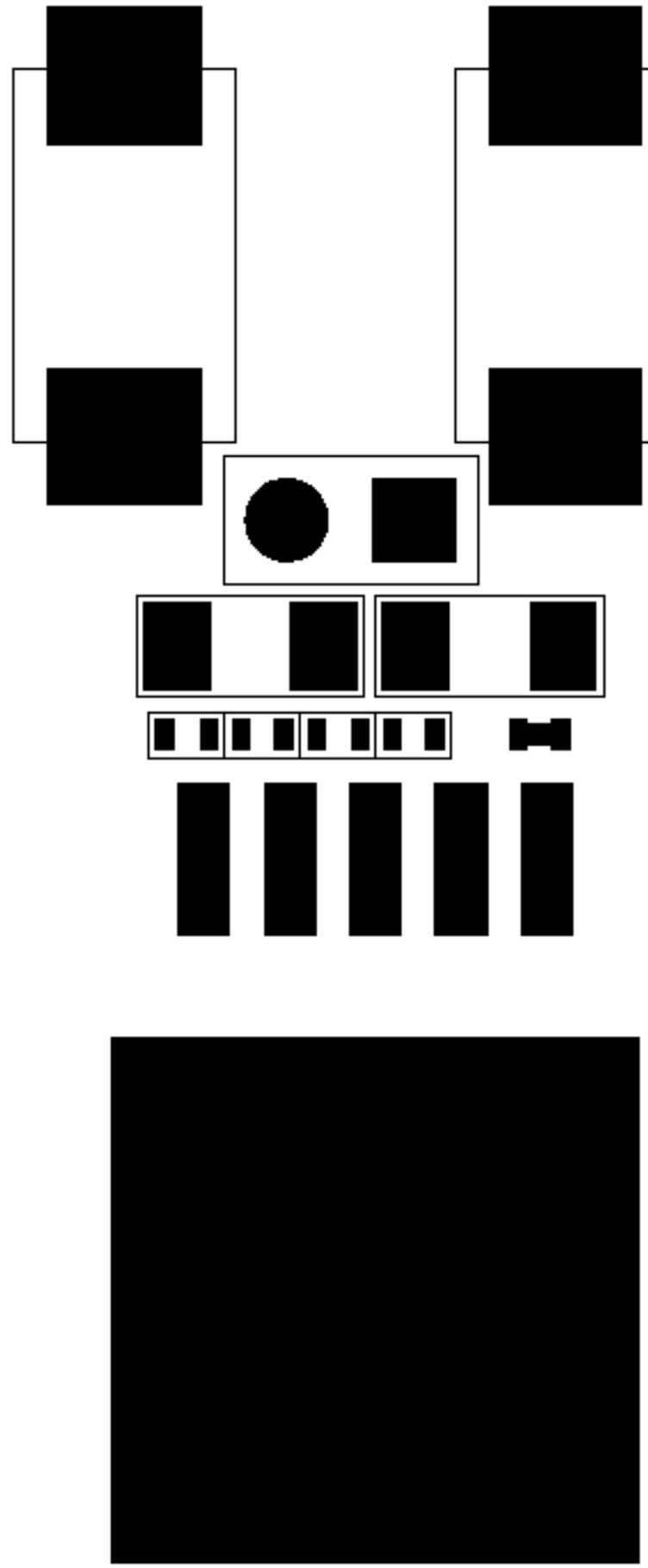
A2

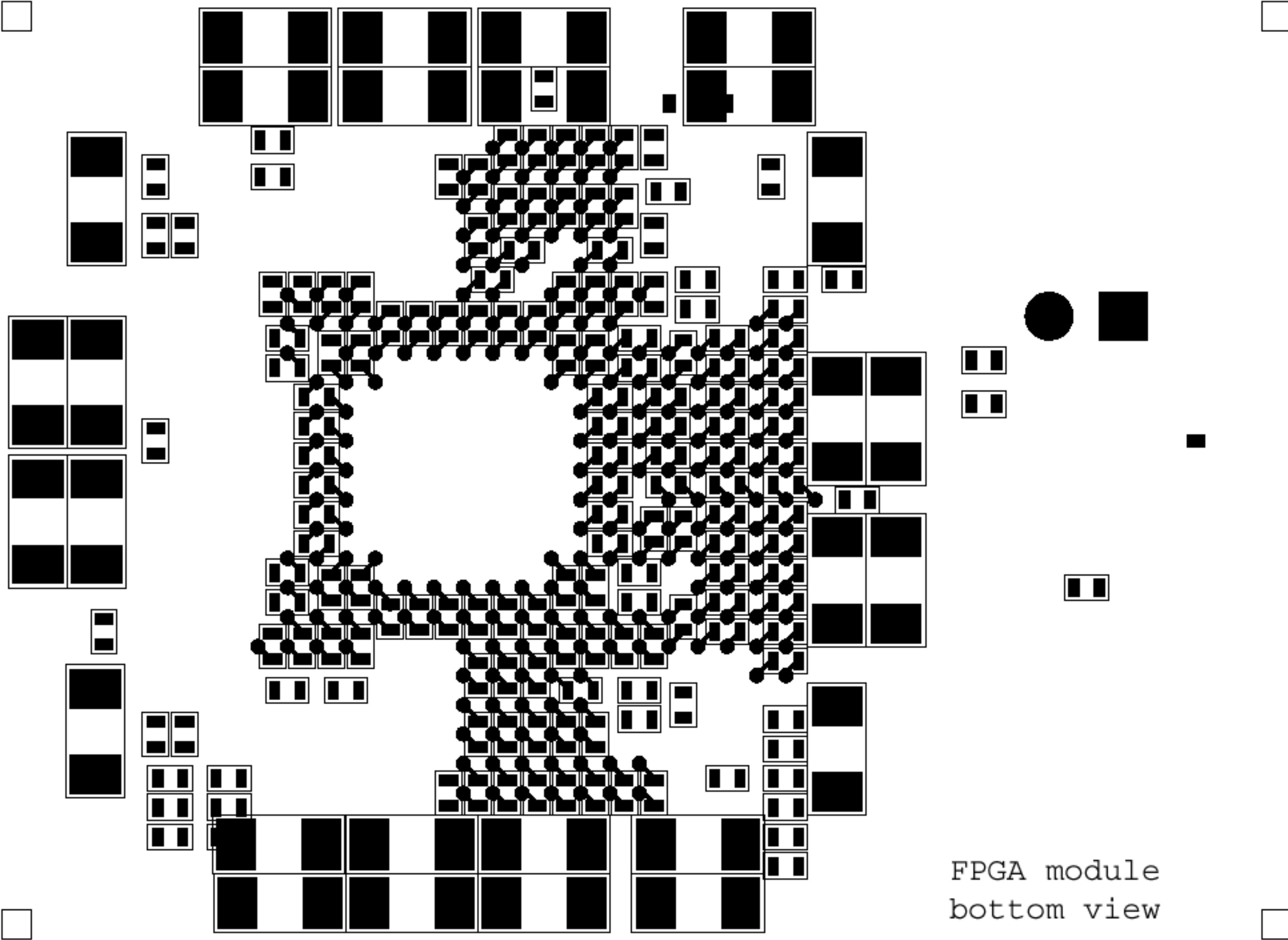
TOTAL NO. OF SHEETS

notes



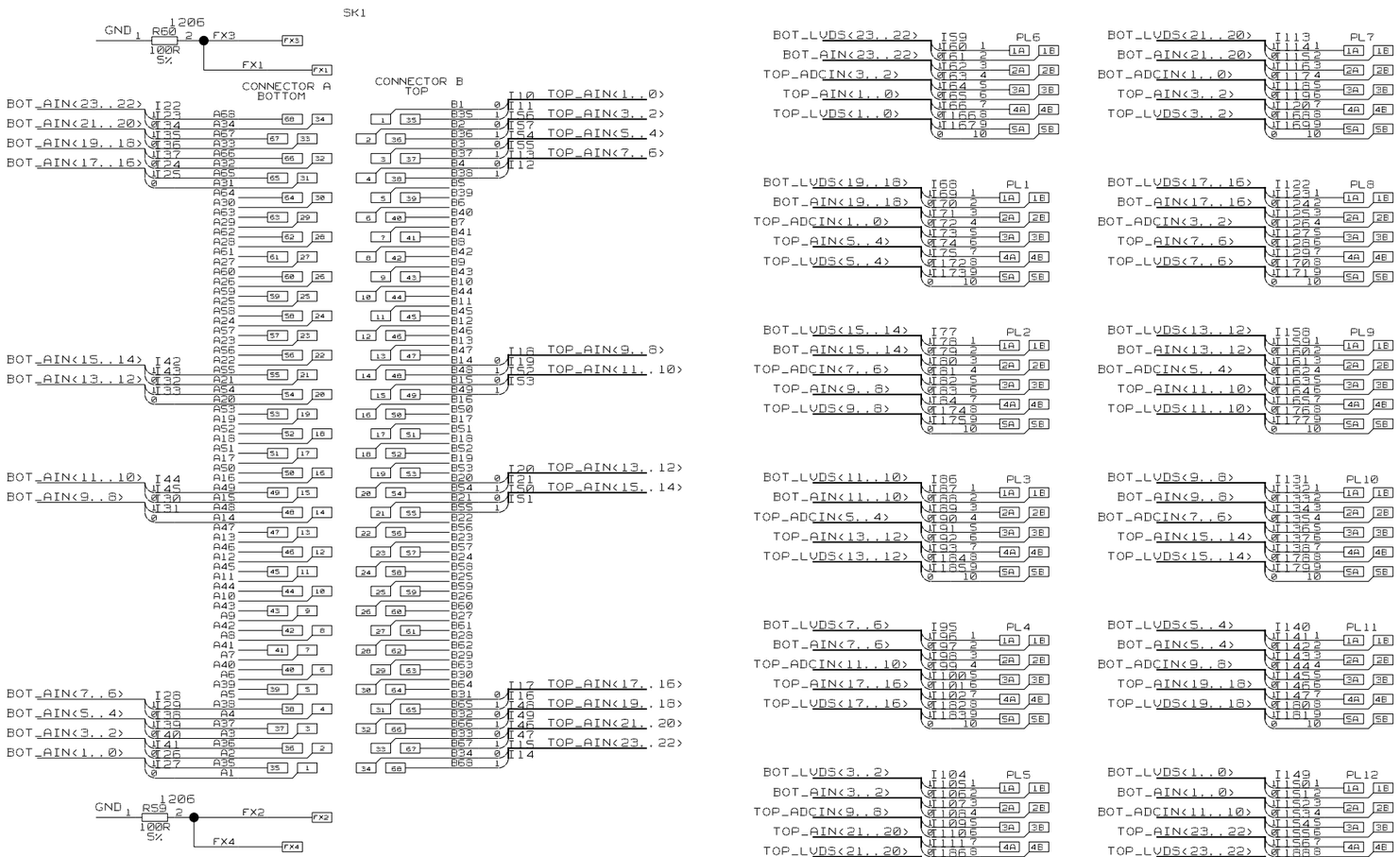
FPGA module top view




FPGA module
bottom view

	1	2	3	4	5	6	7	8	9	10
A	2	THIS DRAWING CONFORMS TO B.S. 3939								

THIS PINOUT WILL CHANGE



PROVISIONAL

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TITLE

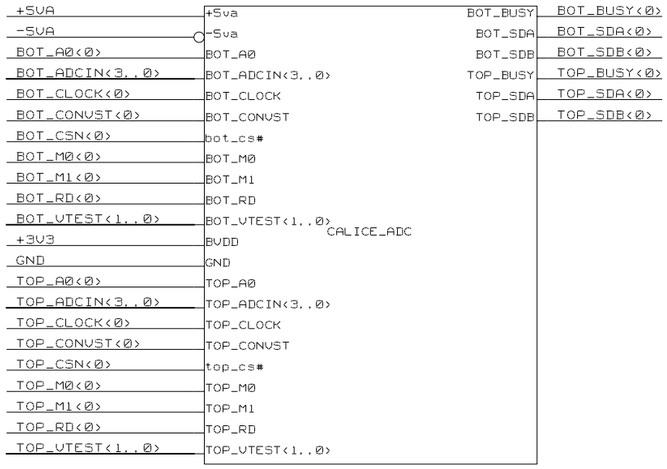
SCSI CONNECTOR AND SELECTION JUMPERS

A	2

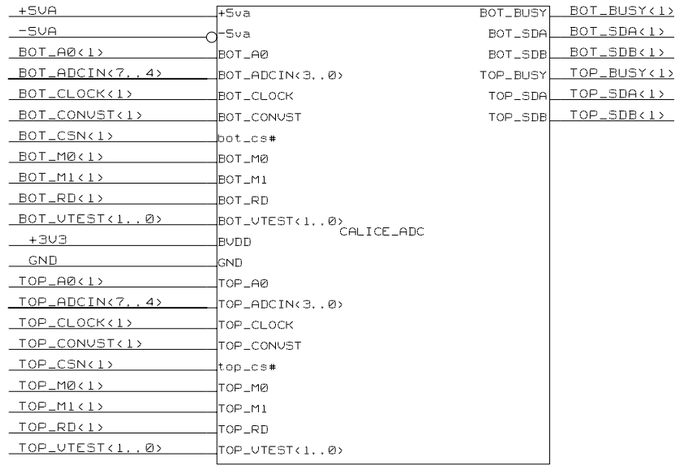
TOTAL NO. OF SHEETS

A2	THIS DRAWING CONFORMS TO B.S. 3939	

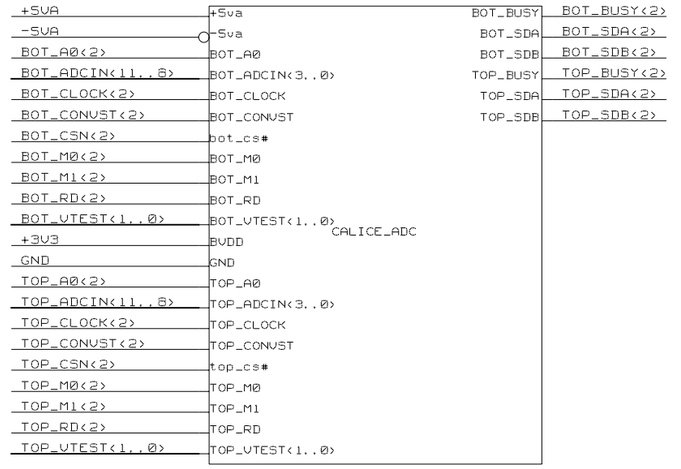
I3



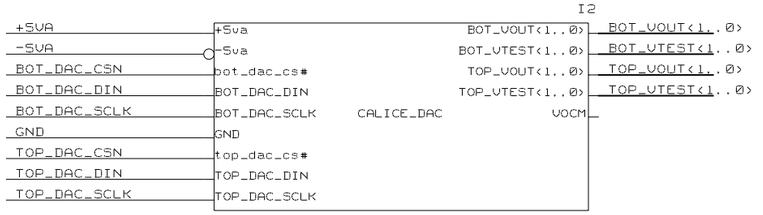
I1



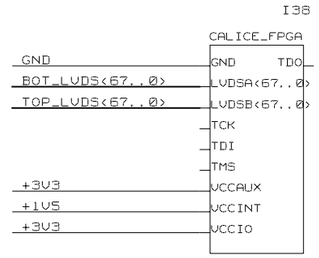
I37



I2



I38



PROVISIONAL

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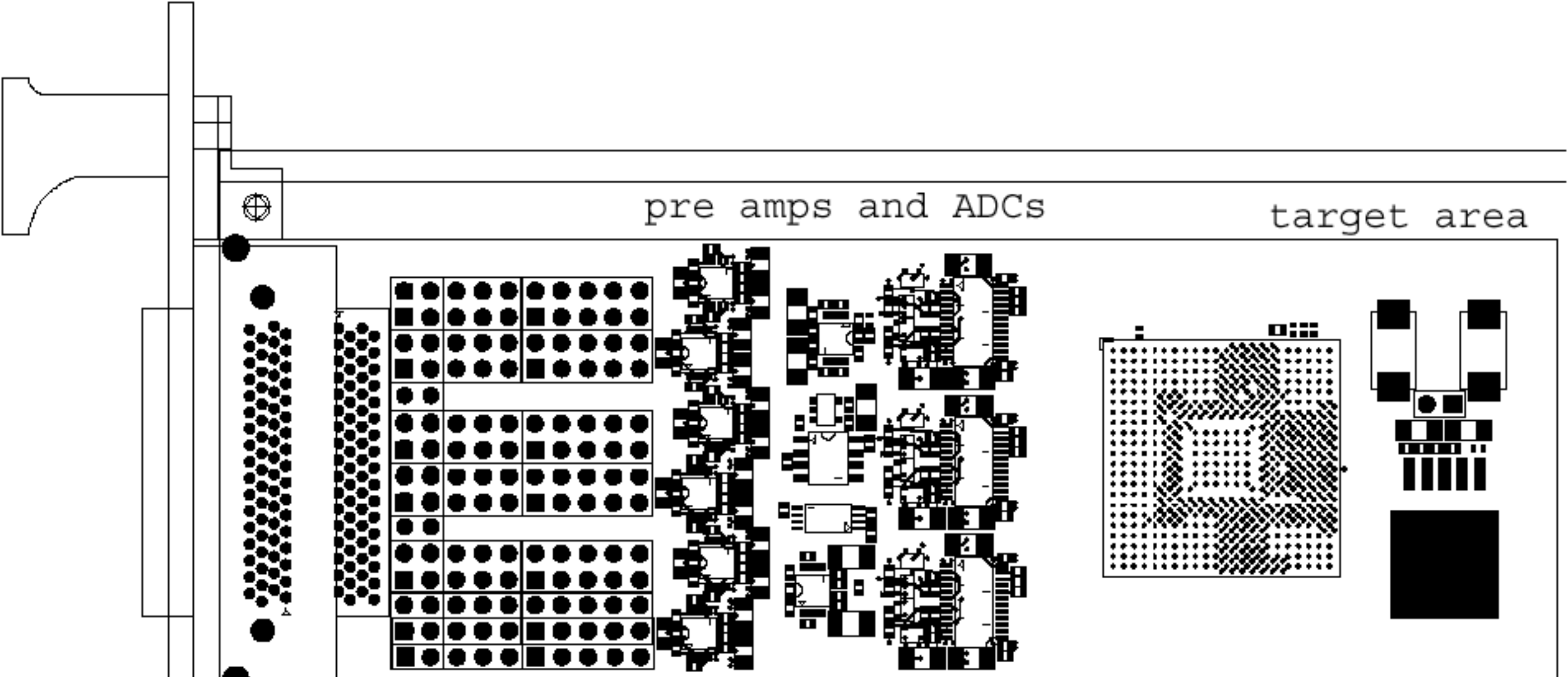
TITLE

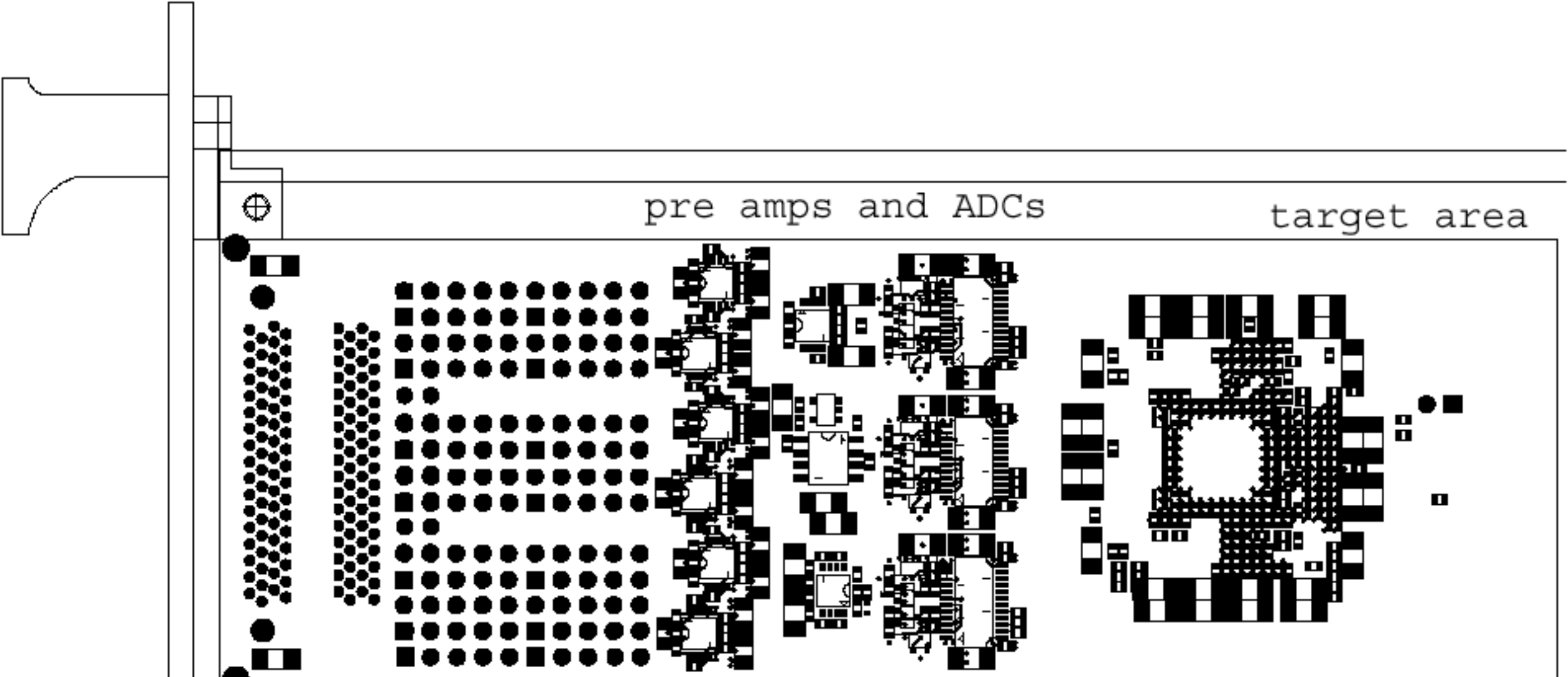
ALL MODULES

A2	

TOTAL NO. OF SHEETS



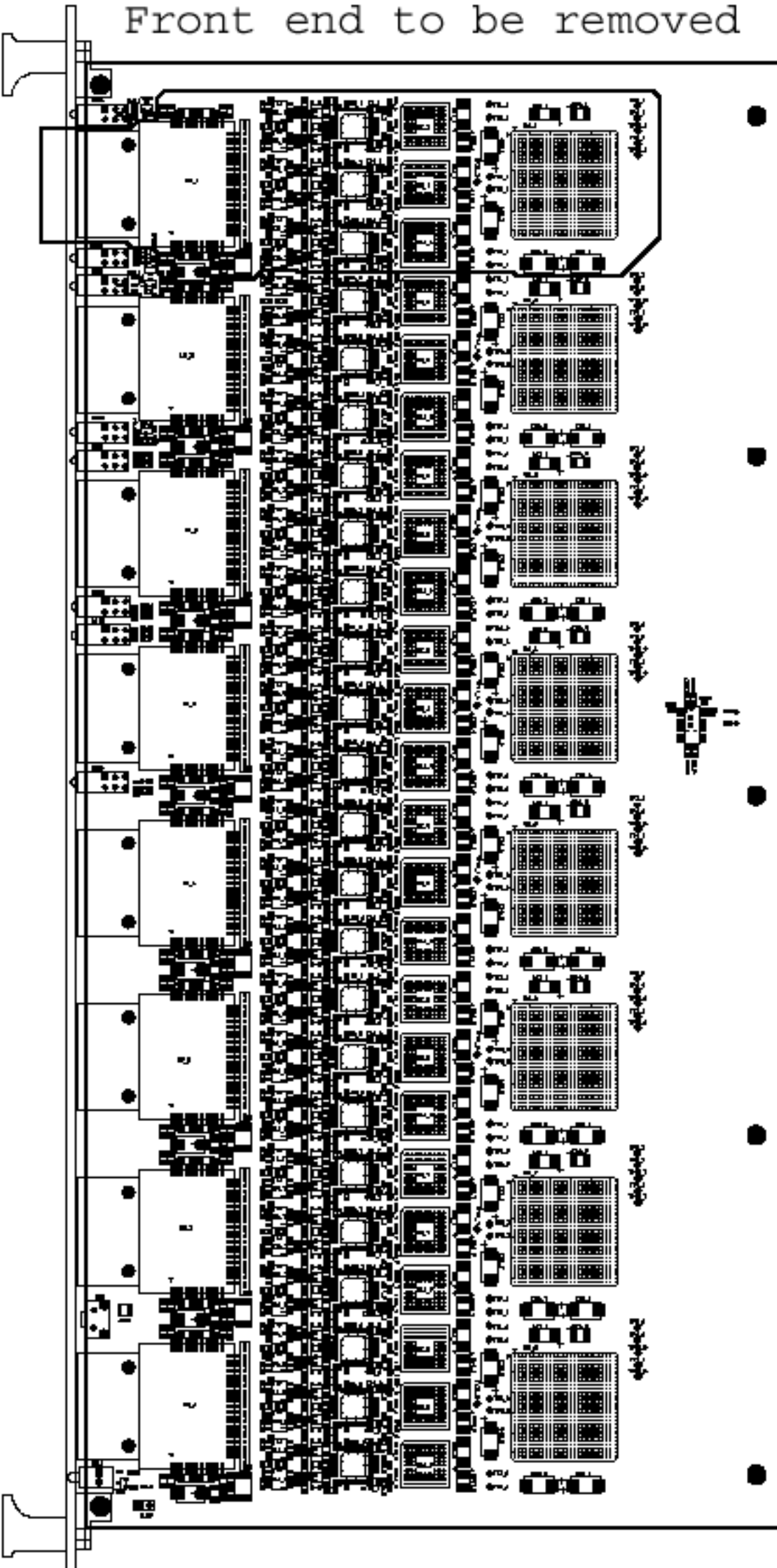
Arrangement of all modules, top view



Arrangement of all modules, bottom view

Front end to be removed

top view



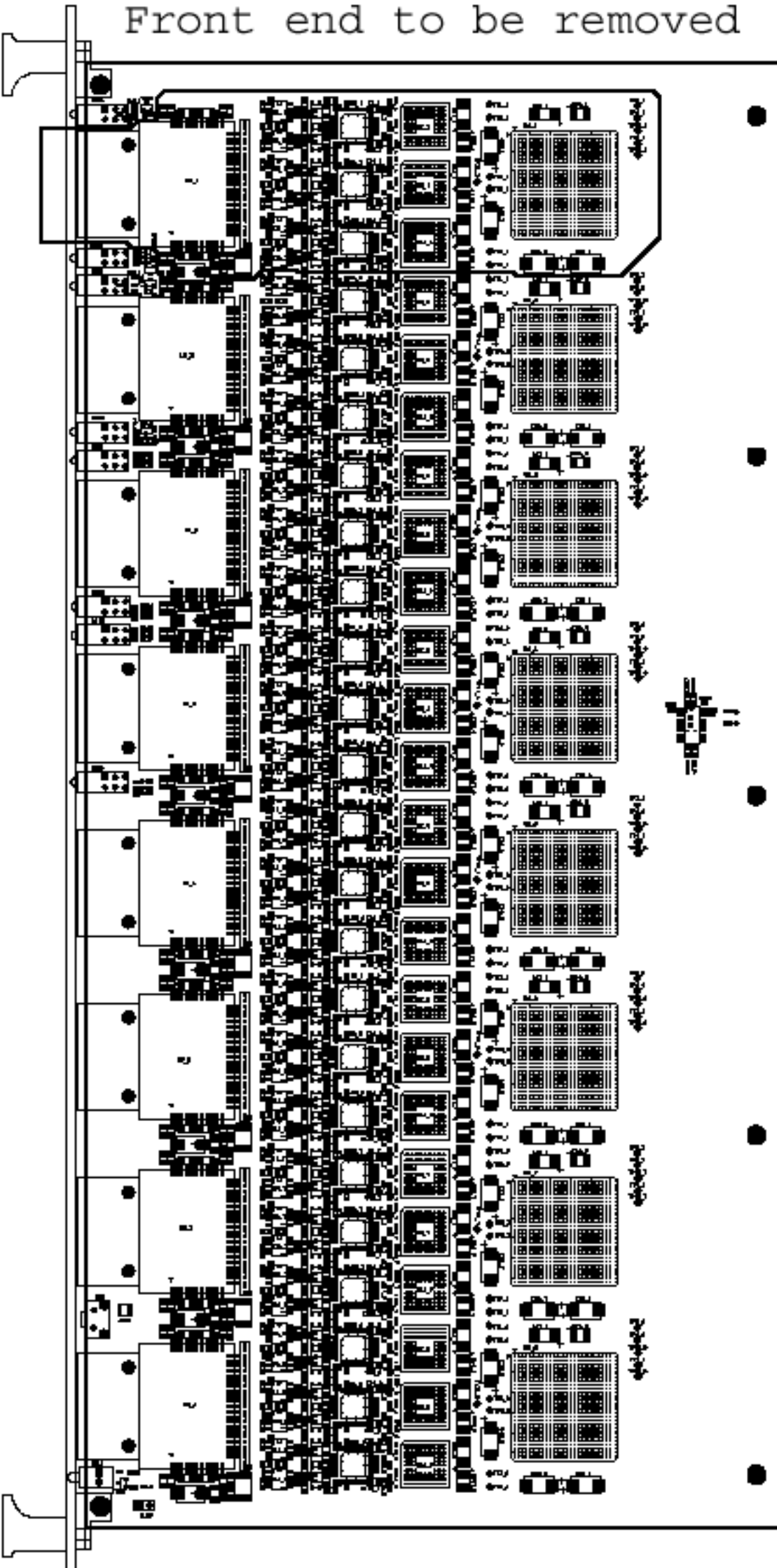
CMS

BACK

END

Front end to be removed

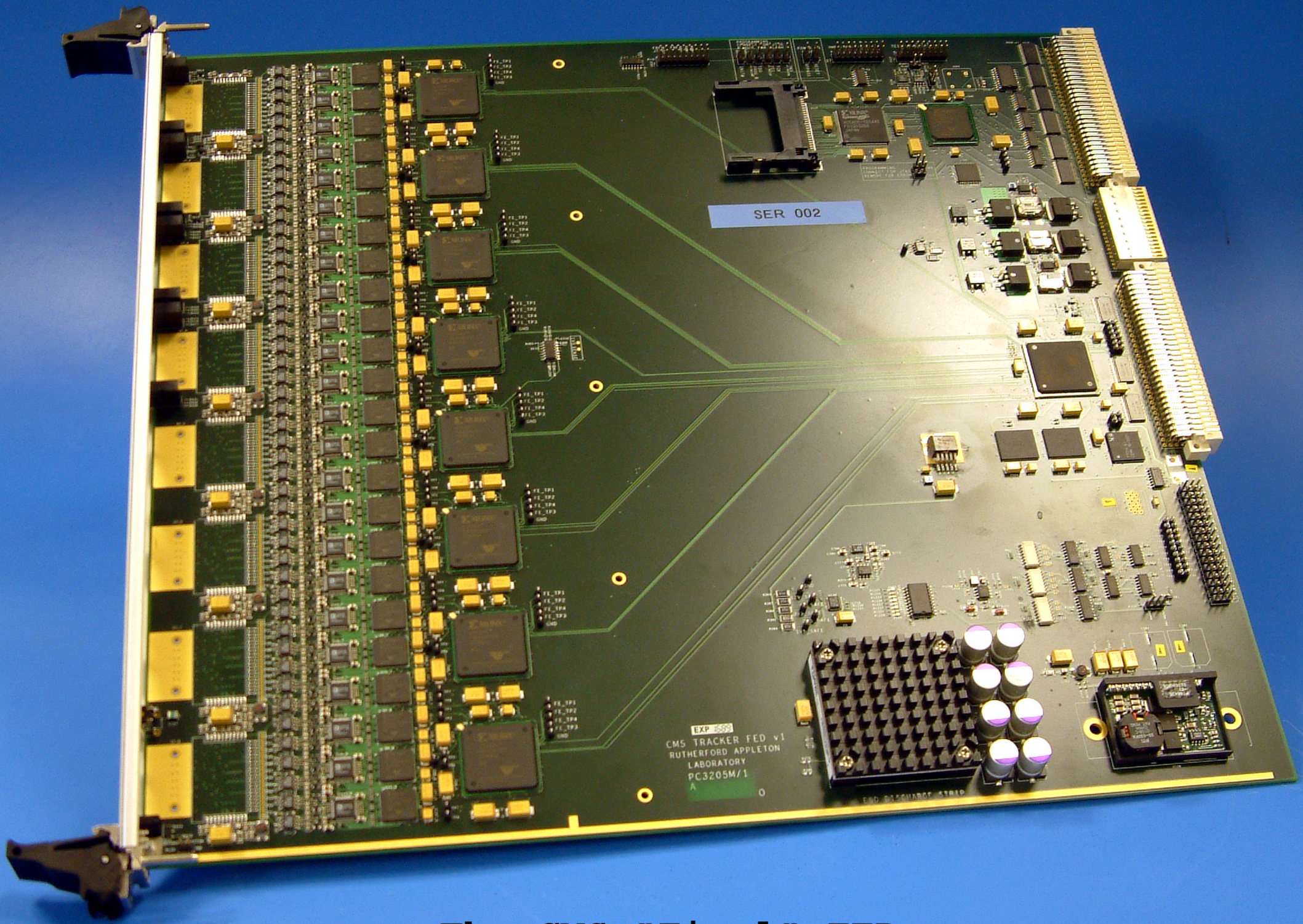
top view



CMS

BACK

END



The CMS "Final" FED

The CMS "Final" FED

showing the 12 way optical module and Analogue electronics.