UK ECAL Hardware Status

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People

Work presented here due to:

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- Imperial College London
  - Osman Zorba, Paul Dauncey
- University College London
  - Matt Warren, Martin Postranecky
- Manchester University
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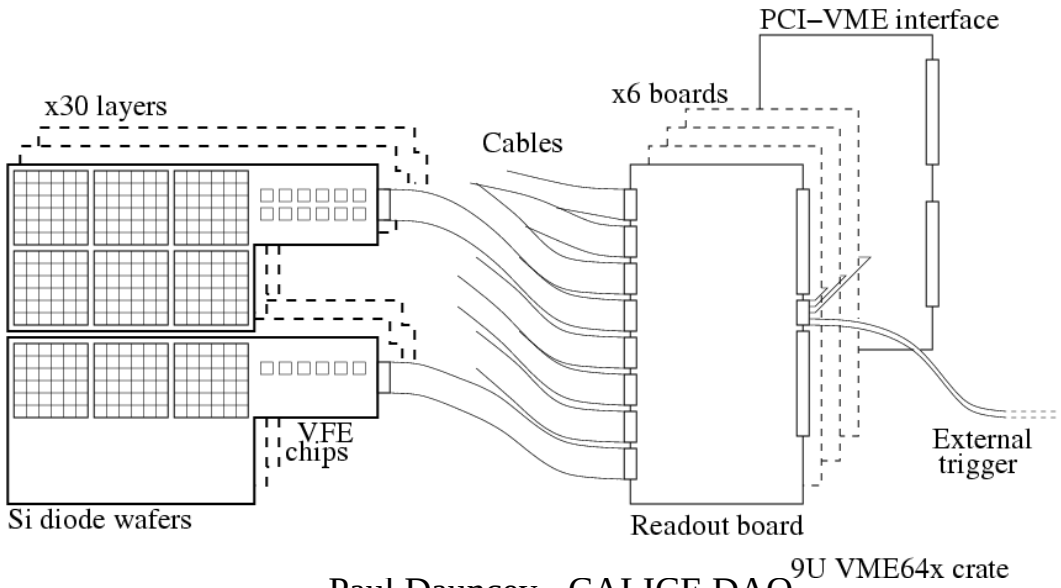
Readout electronics overview

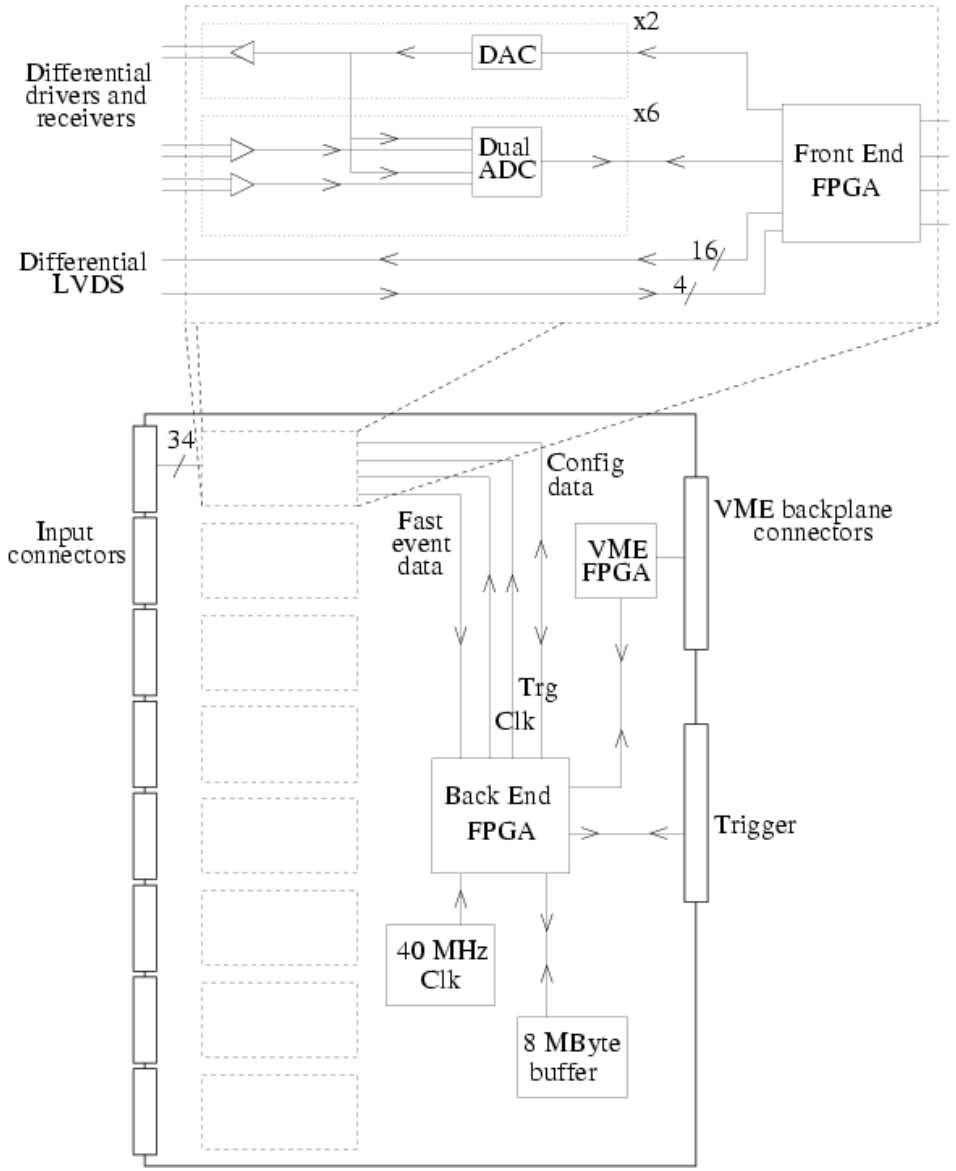
CALICE ECAL has 30 layers, 18×18 channels/layer, 9720 total

- Each gives analogue signal, 14-bit dynamic range
- Very-front-end (VFE) ASIC (Orsay) multiplexes 18 channels to one output line
- VFE-PCB handles up to 12 VFEs (216 channels)
- Cables from VFE-PCBs go directly to UK VME readout boards, called Calice Ecal Readout Cards (CERCs)



CERC overview

- Eight Front End (FE) FPGAs control all signals to front end electronics via front panel input connectors
- Back End (BE) FPGA gathers and buffers all event data from FE and provides interface to VME
- Trigger logic in BE for timing and backplane distribution; only active in one board
- Each input is one full or two half-full VFE-PCBs; need 45 inputs = 6 CERCs

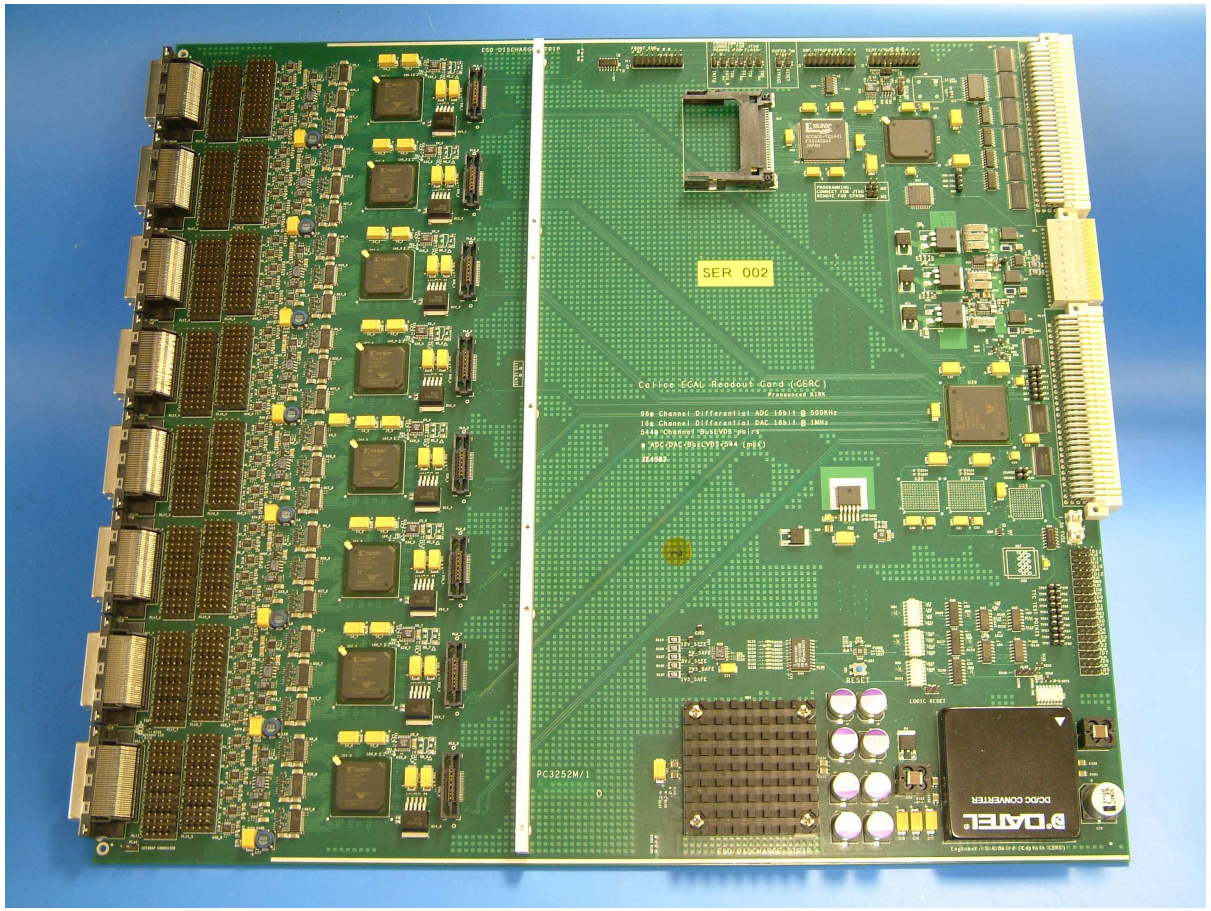


CERC features

- Based on CMS silicon tracker readout (FED)
  - Will “borrow” a lot of firmware from them
  - Unfortunately not yet as well-developed as hoped
- Dual 16-bit ADCs and 16-bit DAC
  - DAC fed back for internal as well as front end calibration
  - ADC 500kHz; takes ~80μs to read and digitise event data from VFE-PCB
- No data reduction in readout board
  - ECAL event size: 3.5 kBytes per board, 20 kBytes total per event
- On-board buffer memory; 8 MBytes
  - No buffering available in ECAL front end; receive data for every trigger
  - Memory allows up to ~2k event buffer on readout board during beam spill
  - VME readout speed ~20 MBytes/s; several seconds readout after spill
- Large amount of unused I/O from BE FPGA to backplane
  - Will implement trigger logic and control/readout interface to VME in BE

CERC status

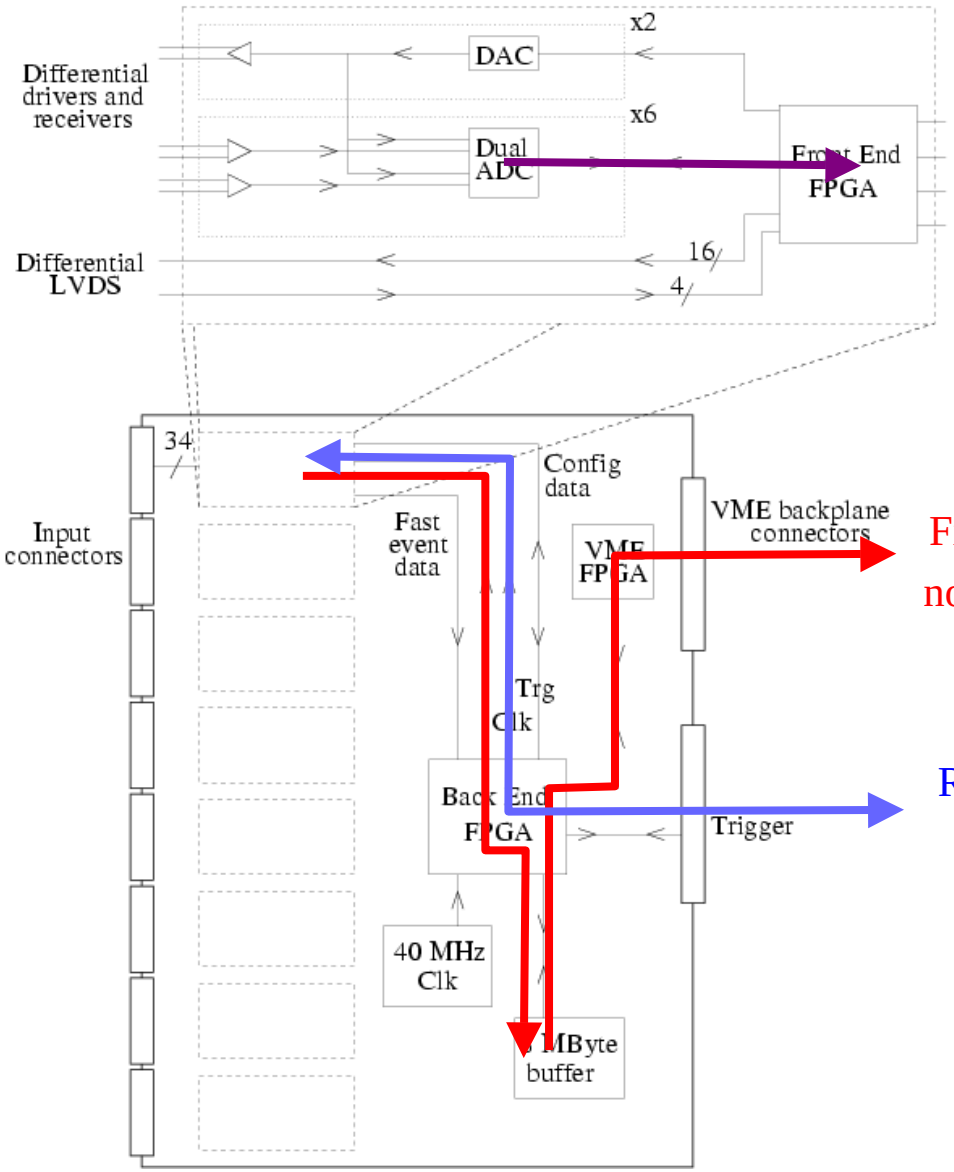
- Prototype design completed last summer
- Two prototype boards fabricated last year
  - Arrived on November 21 at Rutherford Laboratory
- Currently under stand-alone tests in the UK
  - Aim to test with a VFE-PCB in the UK very soon
  - Move UK hardware to Paris (Ecole Polytechnique) for cosmic tests with fully populated VFE-PCB with Si wafers in Feburary



Test setup

- Final path for data has several complex steps
  - FE digitises ADC data for each trigger
  - Automatically transferred to 8MByte memory
  - Memory read from VME when bandwidth available
- Needs data transfer, memory control and VME interface
  - BE FPGA firmware not yet functional
  - Memory components delayed in delivery; not yet mounted on CERCs
  - Aiming for end of March for all this to be working
- Backup for VFE tests
  - Implement simple RS232 interface from PC to BE and hence to FEs
  - FE digitises ADC data and stores in FIFO in FE
  - RS232 reads FIFO one word at a time directly to PC
  - 8MByte memories bypassed, must read each event before next trigger
  - Rate is slow ~1Hz for events; sufficient for cosmics

Test setup data paths



Common to both

Final VME path;
not yet functional

RS232 path;
functional

Test results

- RS232 path complete
  - Read and write configuration data to RAMs in FEs
  - Read and write fake event to RAMs in FEs
  - Read back fake event via FIFO on trigger
  - Tested for several hours continuous running; no errors seen
- Trigger input working
  - Can fire trigger from BE with RS232 command
  - Can send trigger as LVDS signal on spare backplane pins to BE
  - Both functional; allows external cosmic trigger for VFE tests
- ADC readout and DAC control still under development
  - ADC can be read, DAC can be set
  - DAC can be looped back to ADC internally and through front panel
  - All control at present only via Xilinx Chipscope tool
  - No way to take multiple readings; no noise measurement or DAC calibration
  - Connection to RS232 I/O path still needs to be implemented

Known CERC problems

- FPGAs do not always load correctly on CERC power-up
  - Sometimes need to press reset button several times
  - Firmware stored on CompactFlash card; replacing this also works
  - Thought to be due to power-up boot timing sequence
  - Can be adjusted but depends on firmware so wait until semi-final code ready
- Mismatch of DAC output op-amp differential range and ADC input op-amp differential range
  - DAC differential output only single polarity
  - Can only cover top half of ADC range
  - Problem in DAQ op-amp, not ADC, so real signals should be unaffected
  - Unclear if DAQ will have problem with VFE-PCB expected differential range? Wait until we get a VFE-PCB to find out!
- Not yet clear if these can be fixed or require redesign

Future plans

- VFE tests in Paris in February
  - Essential test of prototypes before moving to production
- Possible AHCAL test in March
  - Need more information on what this entails; number of channels, interface specification to VFE-PCB equivalent, etc.
- Finalise redesign by end March
  - Assuming tests successful
- Relayout and fabricated nine production CERCs in April-May
  - Simple fix for known problems may be possible
  - If so, may not relayout; save a month
  - Only have components for nine boards; need to know early if more wanted
  - Also need the money; UK has no money for extra CERCs!
- Full ECAL system tests from July onwards
  - On schedule for DESY ECAL beam test in Oct/Nov