The first testing of the CERC and PCB Version II with cosmic rays

Catherine Fry

Imperial College London

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- DAQ and electronics
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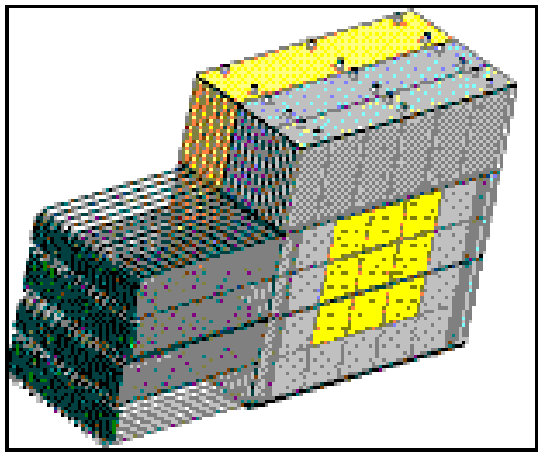
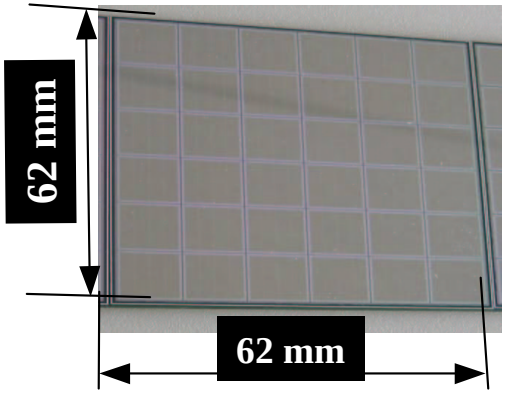
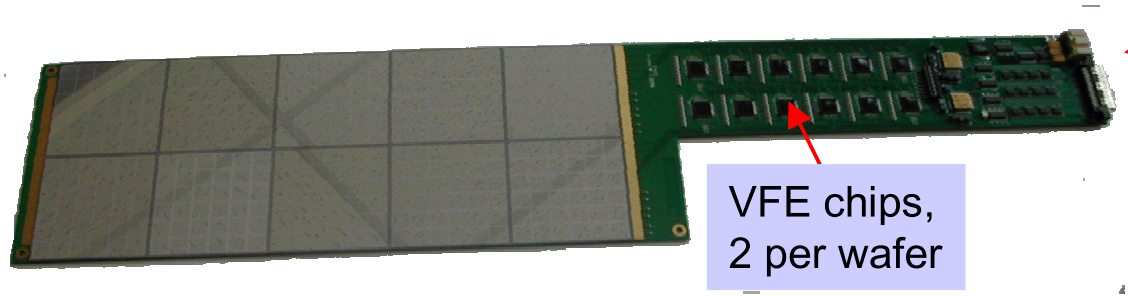
Prototype ECAL design



- 30 layers of silicon and tungsten
- Each layer of silicon contains 3 x 3 =9 wafers
- Each wafer has 6 x 6 =36 pads
- Each pad is 1 x 1 cm^2
- Wafers have been tested: low leakage current (few nA), thickness 525µm ± 3%

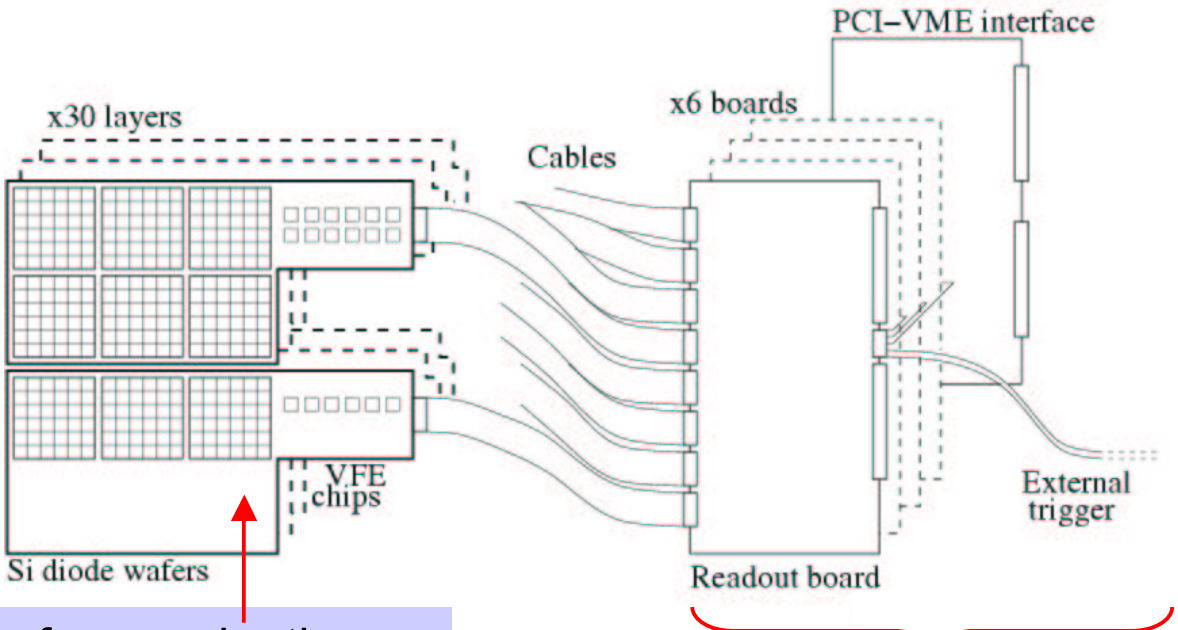
- Wafers mounted on VFE PCB with conductive glue
- 2 VFE PCBs per layer, one fully-filled with 6 wafers, one half-filled with 3 wafers
- 18 channel VFE chips amplify, shape and multiplex the signals from the pads





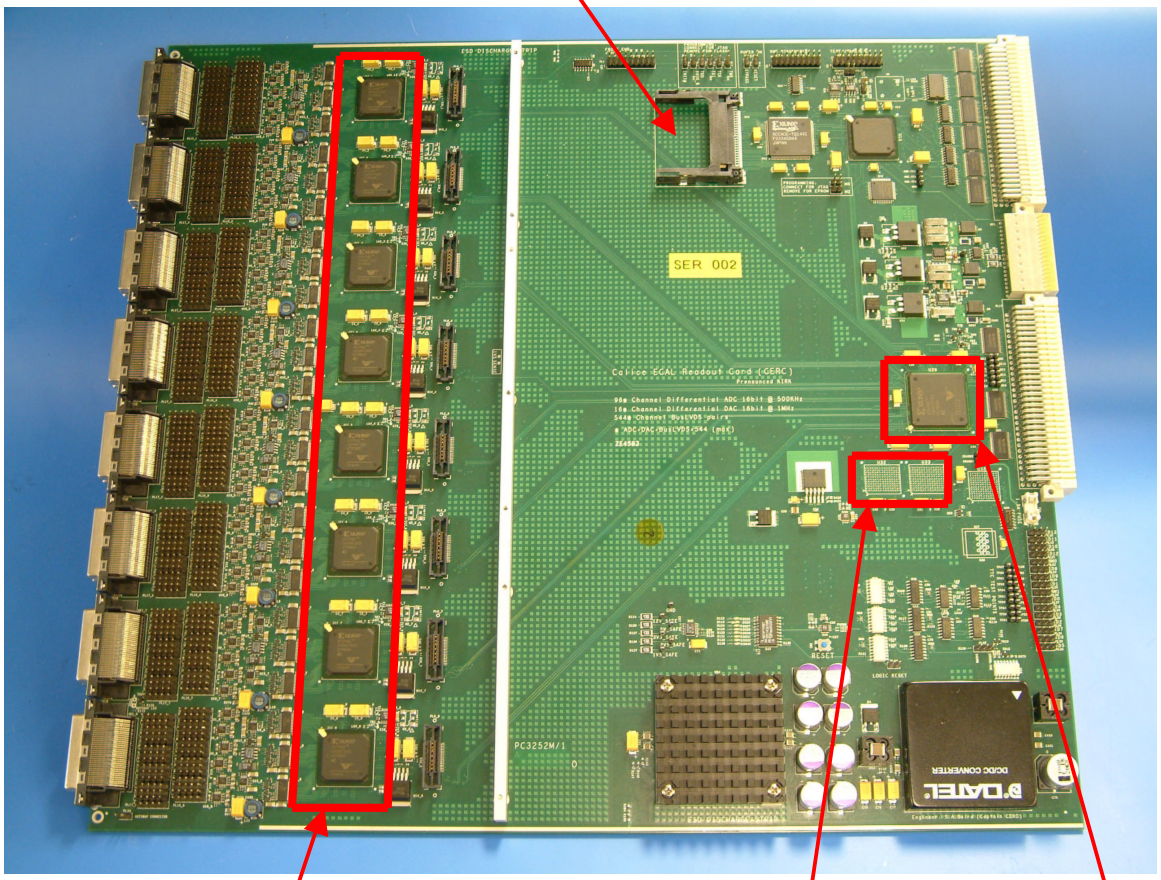
A VFE PCB with 10(!) wafers – the one tested had just one, then two wafers mounted

DAQ and electronics



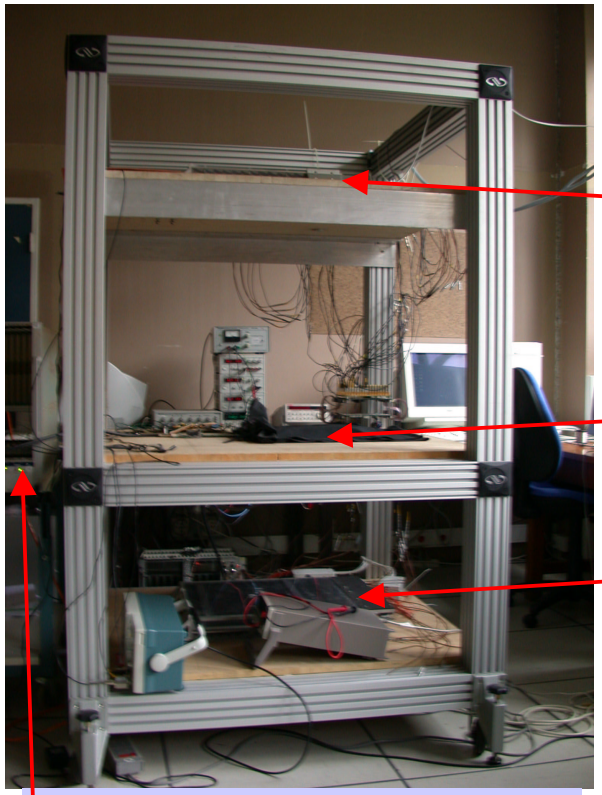
- The 30 layers of VFE PCBs are read out through 6 readout boards (CERCs) when triggered
- The readout boards are housed in a 9U VME crate

The CERC



- Based on CMS tracker FED
- 8 FE FPGAs on left which digitise over 200 multiplexed signals through twelve 16-bit 500kHz ADC channels
- Then through FIFO to 8Mbyte memory – read out when bandwidth available
- One BE FPGA on right, buffers data from FE, performs I/O, configuration, control, trigger control and data readout
- All raw data read out, no zero suppression

Cosmic test setup



Upper x and y planes of hodoscope

Silicon

Lower x and y planes of hodoscope

The cosmic test bench at LLR

Crate containing 1 CERC

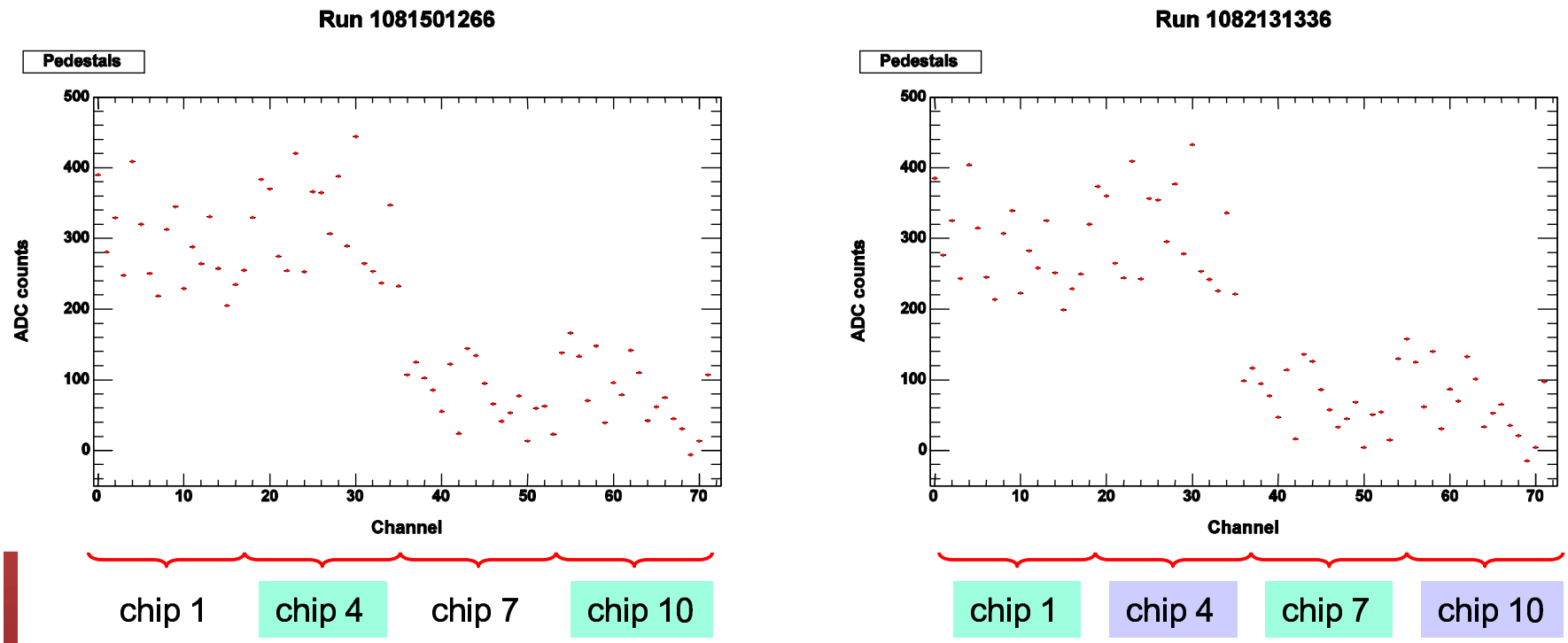
PC for run control and data storage

- Trigger from cosmic rays coincident in upper and lower hodoscope planes
- Each layer of hodoscope has 16 scintillator strips, slightly overlapping, but only first 8 connected
- BE firmware was not ready so PC connected to BE via RS232 interface
- Data read out straight from FE FIFO, one word at a time
- 8MByte memory not yet available so each event had to be read out before next trigger – not a problem as cosmic rate sufficiently low
- Data stored in ASCII format

The runs

- 2 cosmic runs taken over 2 weekends in April 2004:
  - 1st run: 35,100 events
  - 2nd run: 27,100 events
- 1st run: 1 wafer present, from Moscow State University, and 4 VFE chips: 1, 4, 7 and 10 (4 and 10 connected to the wafer)
- 2nd run: Another wafer added, from Prague Academy of Sciences, read out through VFE chips 1 and 7
- For the 1st run the Russian wafer was centred between the hodoscope layers to maximise the number of cosmic triggers actually passing through the wafer
- For the 2nd run the Czech wafer was centred
- In both runs for each event the data was read out from: 16 strips of the 4 hodoscope planes and all 18 channels of all 4 VFE chips, also some configuration data and the event number
- All data stored on PC

Pedestals

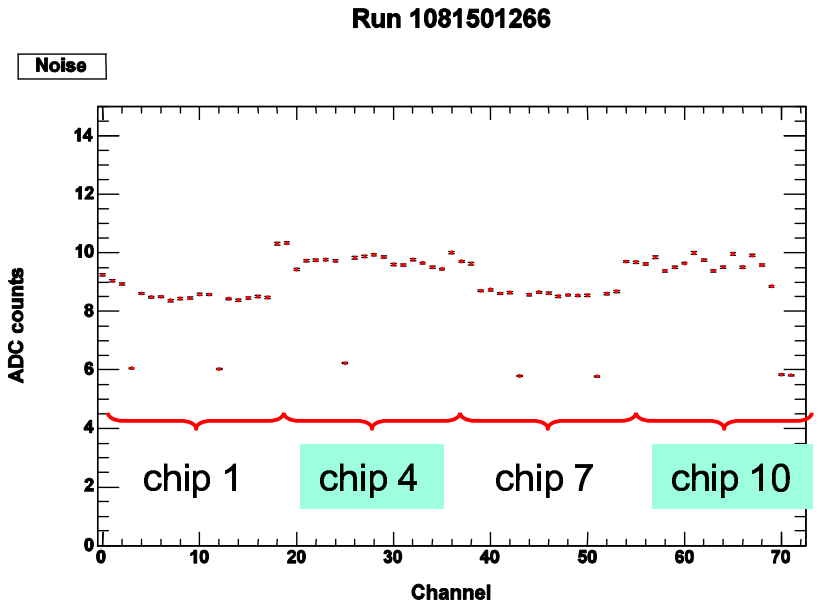


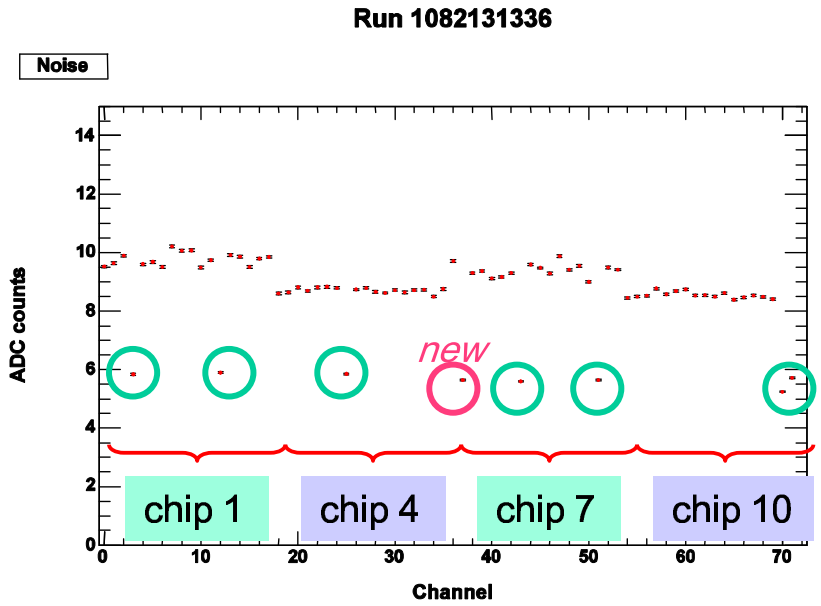
Chips: white = not connected to a wafer; turquoise = connected to centred wafer; purple = connected to un-centred wafer

- Pedestals ~constant between the two runs
- ADC range: -32768 to +32767 ADC counts (16 bits)
- Pedestals are a few hundred ADC counts → only half of ADC range available

RMS noise

= dead channels

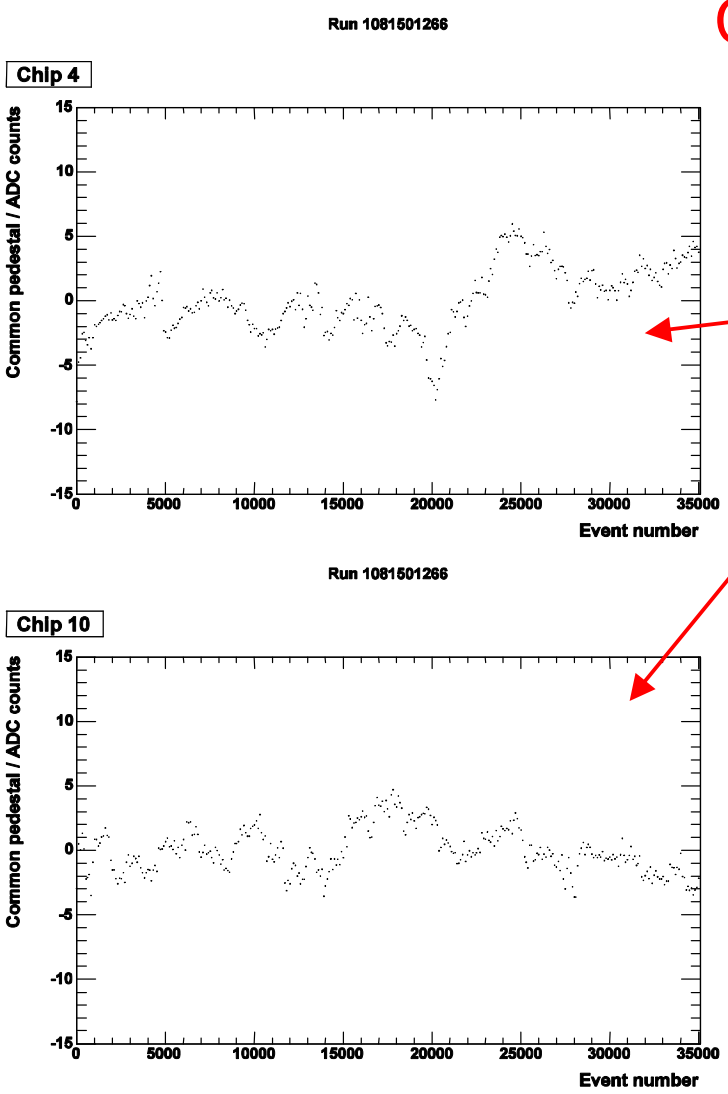




Chips: white = not connected to a wafer; turquoise = connected to centred wafer; purple = connected to un-centred wafer

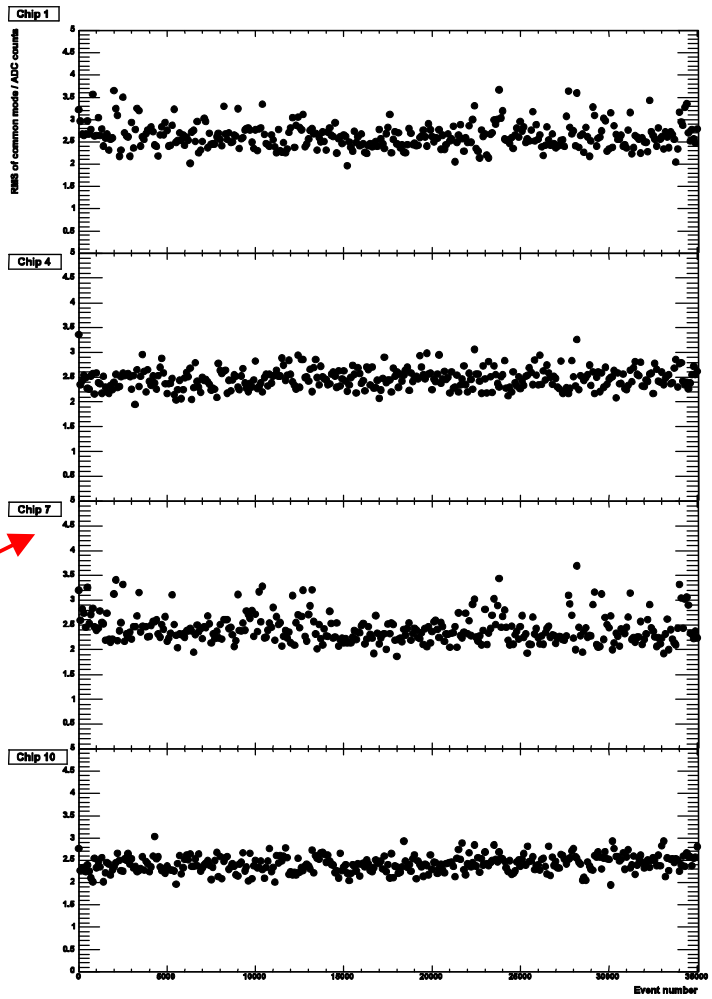
- RMS noise 8 – 10 ADC counts
- Dead channels have RMS noise around 6 ADC counts – 7 dead channels in 1st run, one extra dead channel in second run
- Dead channels ignored in further analysis
- Chips connected to wafers receiving cosmic rays when hodoscope triggers (4 and 10 in 1st run and 1 and 7 in 2nd run) have slightly higher noise

Common mode



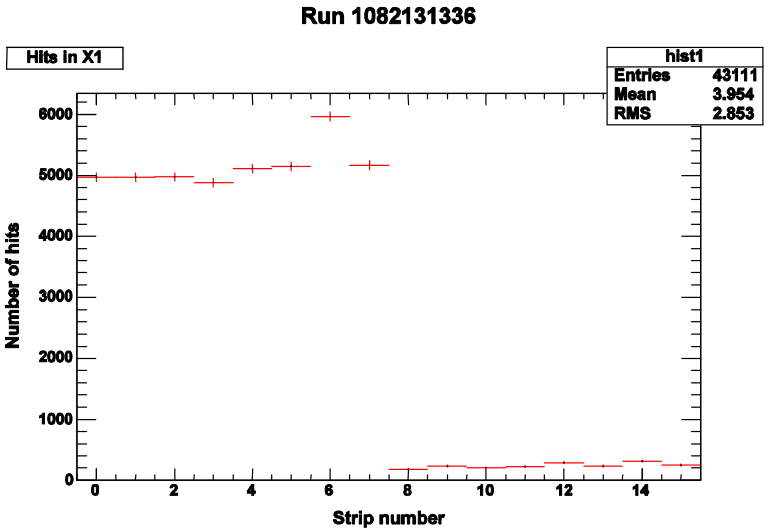
Pedestal variation for two chips connected to wafer throughout 1st run

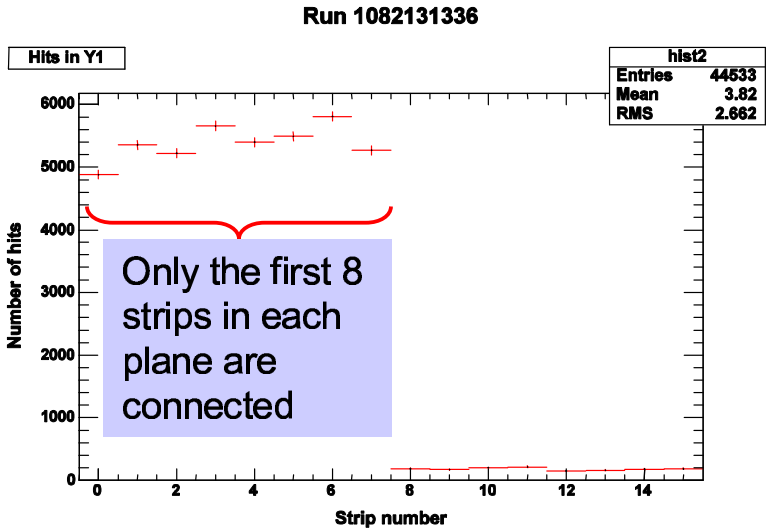
Common mode RMS for each chip throughout 1st run

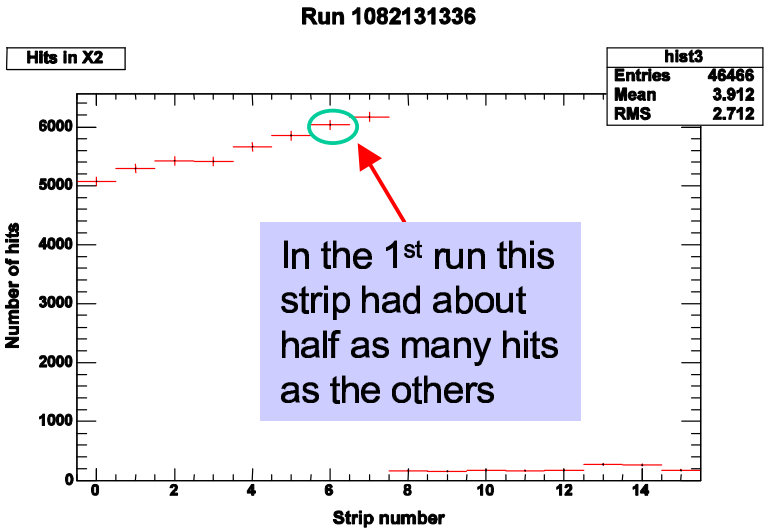


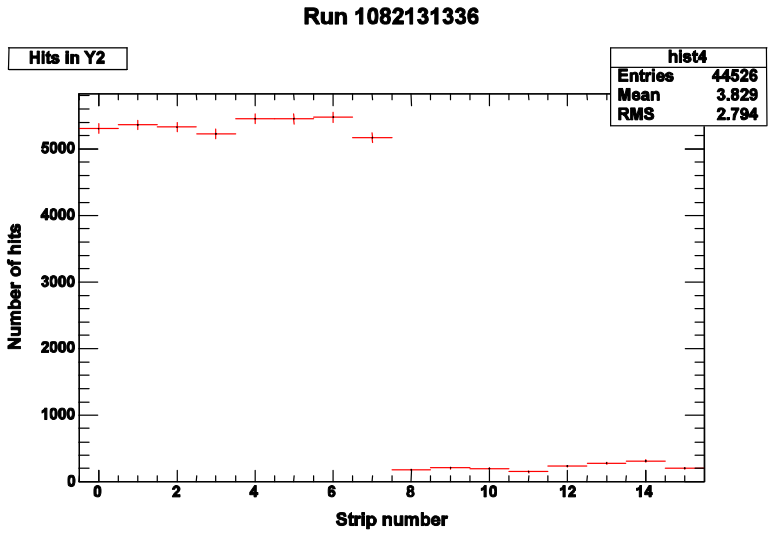
- Pedestals move by a few ADC counts throughout both runs for all four chips
- RMS of common mode > RMS / √18 → due to variation in common mode

Hodoscope data





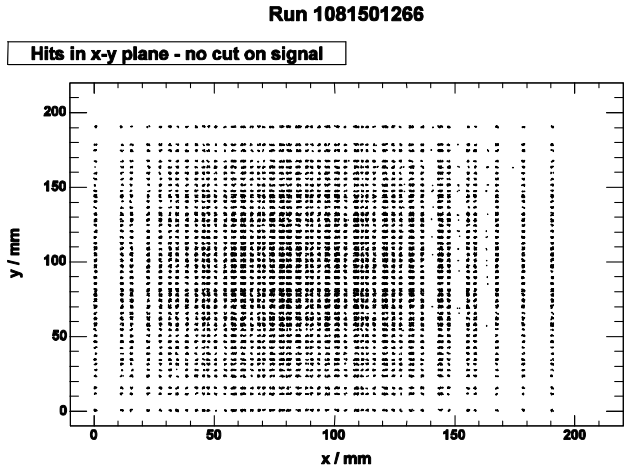


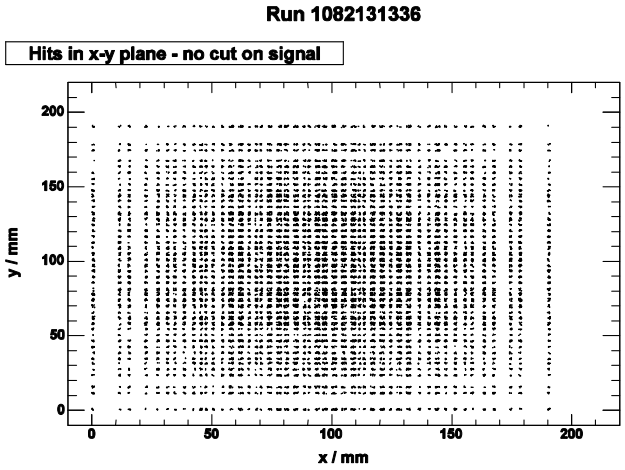


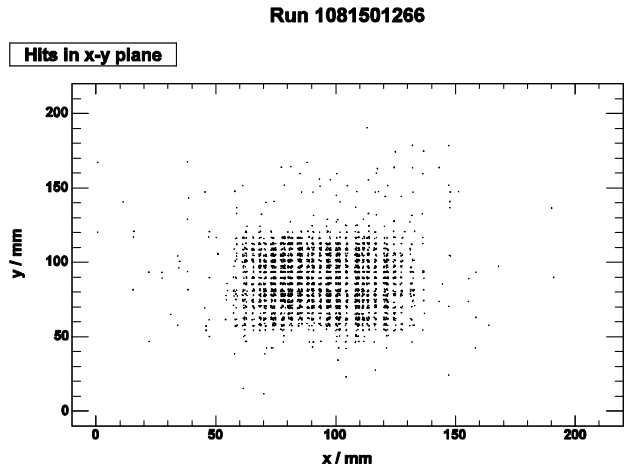
Fairly smooth response over the 8 connected strips in each plane

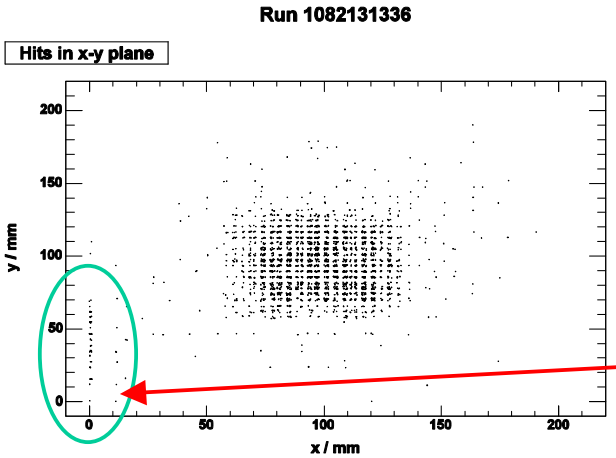
Wafer alignment

- From the hodoscope data, interpolate the (x,y) position where the cosmic ray crossed the wafer (top plots)







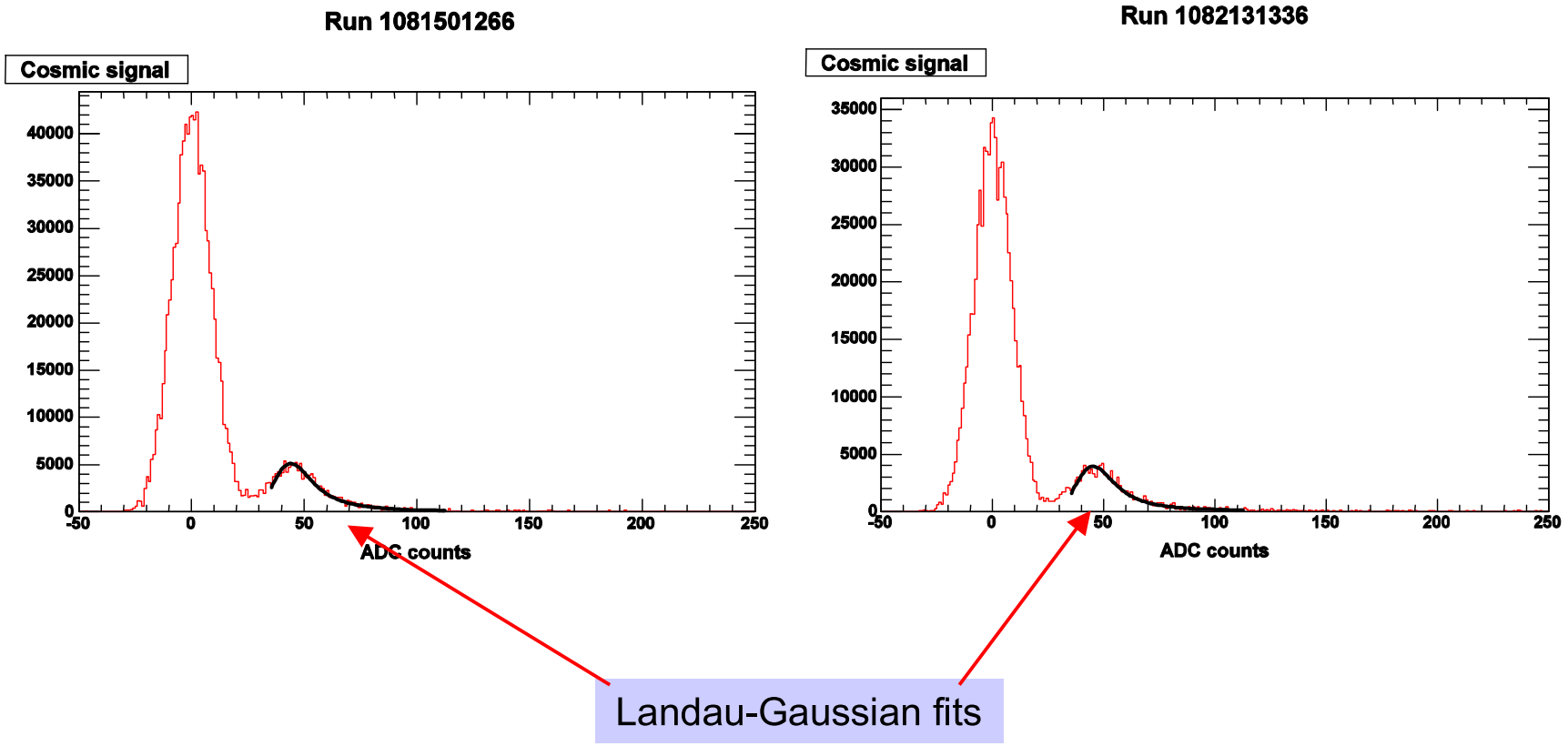


- Take all signals in wafer > 40 ADC counts (4 to 5σ) above pedestal
- Want to eliminate as much noise as possible
- For each pad find the average x and y position from the track interpolation
- Lower plots: hits in x-y for signals > 40 ADC counts → can see outline of wafer

here can see edge of 1st wafer

Cosmic signal

- For each event use hodoscope data to interpolate wafer (x,y) position
- Identify the 4 closest pads to this point and subtract common mode and pedestals
- Plot signal distribution fitting a Gaussian to the pedestal to measure the noise and a Landau-Gaussian convolution and a Landau to the signal to locate the m.i.p. peak

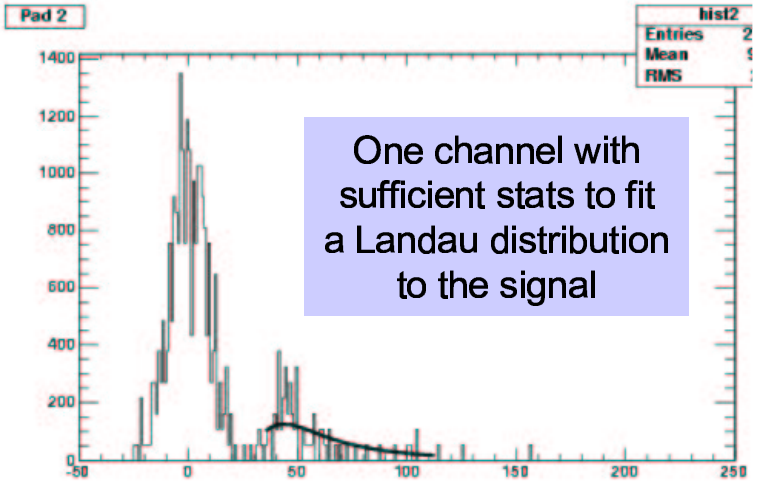


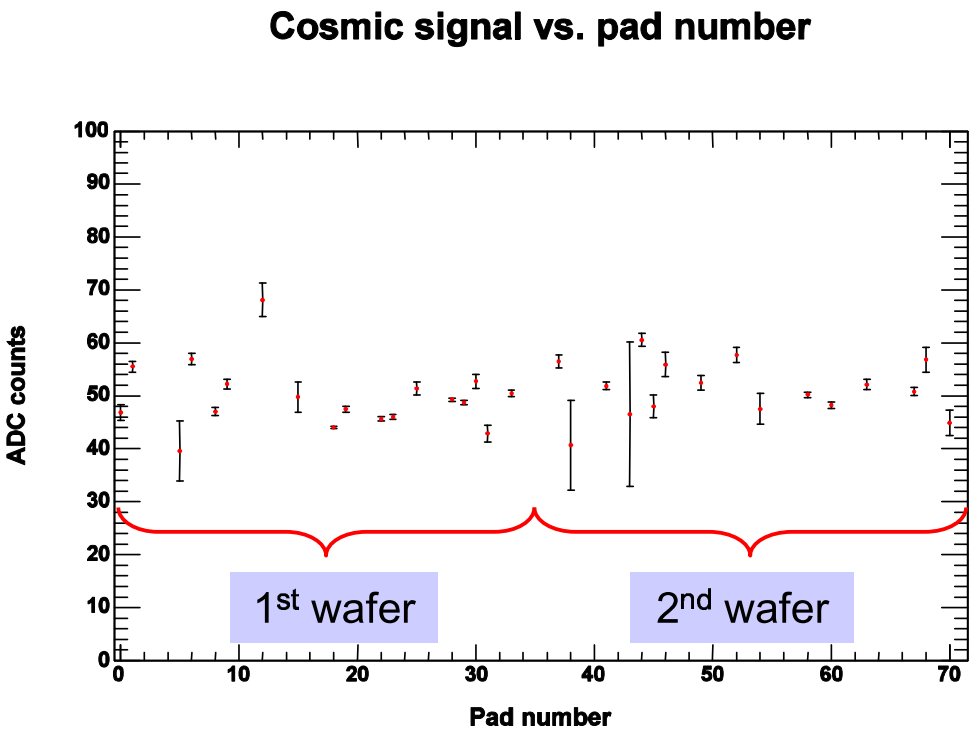
MIP, dynamic range, S/N and wafer comparison

Value	1st run (Russian wafer)	2nd run (Czech wafer)
Noise / ADC counts	8.64 ± 0.01	8.46 ± 0.01
Signal (L-G) / ADC counts	41.95 ± 0.05	43.08 ± 0.05
Signal (L) / ADC counts	43.35 ± 0.04	44.24 ± 0.04
S (L-G) / N	4.9 : 1.0	5.1 : 1.0
1 ADC count / keV	4.8	4.6
ADC dynamic range / m.i.p.s	800	800

- require S / N ≥ 4 : 1 → we have better than requirement
- require ADC dynamic range ≥ 600 m.i.p.s → we have better than requirement
- difference in m.i.p. between wafers ± 1.3%
- wafers manufactured to thickness ± 3%
- $\Delta E \propto \Delta x$ → m.i.p. difference consistent with possible difference in thickness
- difference in m.i.p. between fits → take L-G value and use other value to estimate systematic error

Signal vs. channel





- located signal with a Landau fit (insufficient stats per channel for Landau-Gaussian convolution to work)
- only 30 channels (out of 72) had sufficient stats to fit signal
- fit constant to each wafer:

$m.i.p._1 = 47.39 \pm 0.13$

$m.i.p._2 = 48.83 \pm 0.19$

- slightly higher than values from all channels together, even with Landau fit, but bigger errors
- Need to take longer runs for more stats to better estimate the signal for each channel of VFE chip

Summary

- RMS noise 8-9 ADC counts
- Pedestals few hundred ADC counts → lose half ADC range
- Some common mode noise, few ADC counts
- 1 m.i.p. = 42 – 43 ADC counts
- S / N = 5 : 1 → better than required
- ADC dynamic range = 800 m.i.p.s → better than required
- m.i.p. difference between wafers consistent with possible difference in thickness
- need more stats to accurately measure signal for each channel