TB Review: DAQ

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Scope of DAQ

- Short term view, i.e. next 18 months
  - DESY beam tests, ECAL only, AHCAL only
  - DESY ECAL/AHCAL integration
  - FNAL ECAL/AHCAL beam tests
  - With tail catcher as appropriate
- Systems included
  - ECAL: ~10k channels
  - AHCAL: ~8k channels
  - Tail catcher: ~300 channels
  - DESY beam line data; tracking TDC: 16 channels
  - FNAL beam line data; tracking, PID, trigger, etc: ? channels
- Ignor DHCAL for now
  - See end of talk

DAQ requirements

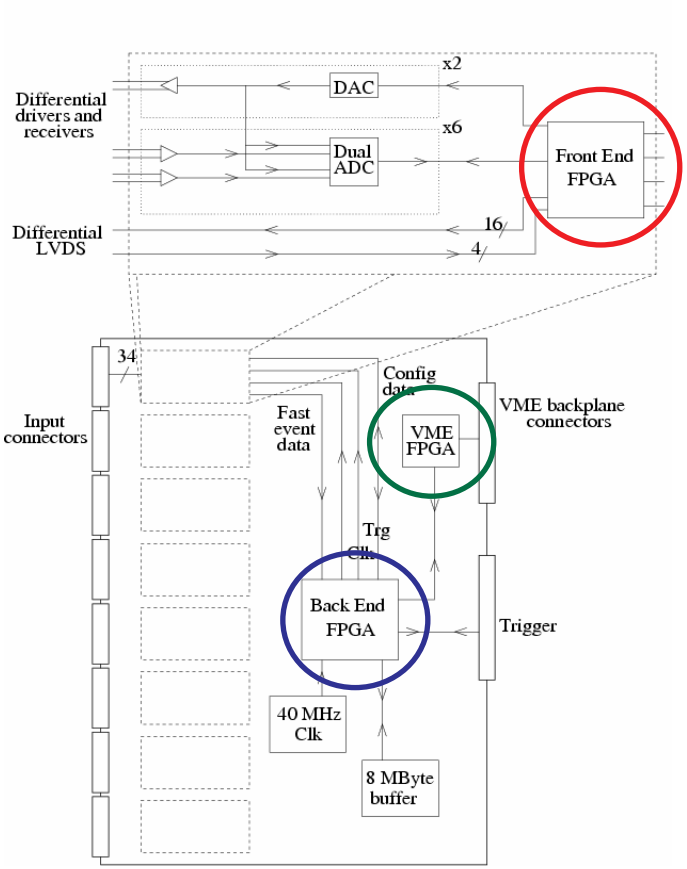
- Need ~10^6 events for each of ~10^2 configurations
  - Total sample of ~10^8 events
- Within reasonable time, take as ~1 month continuous running
  - 1 month ~ 10^7 seconds so need 10Hz event rate
  - Set requirement at 100Hz as can never run continuously
- For spill structure of e.g. 10% duty factor
  - Need 1kHz event rate during spill
  - FNAL might be as bad as 1 spill of 0.6sec/min = 1%; would need 10kHz
  - 100Hz is averaged rate
- No threshold suppression online
  - Want to study pedestals, etc, in detail
  - ECAL, AHCAL both ~10k channels × 16 bit ADCs = 20kBytes/event
  - Take total event size as 50kBytes; total sample = 5TBytes
  - Need averaged data rate of 5MBytes/s
  - Run duration will be limited by file size; 2GBytes takes 400 secs ~ 7 minutes

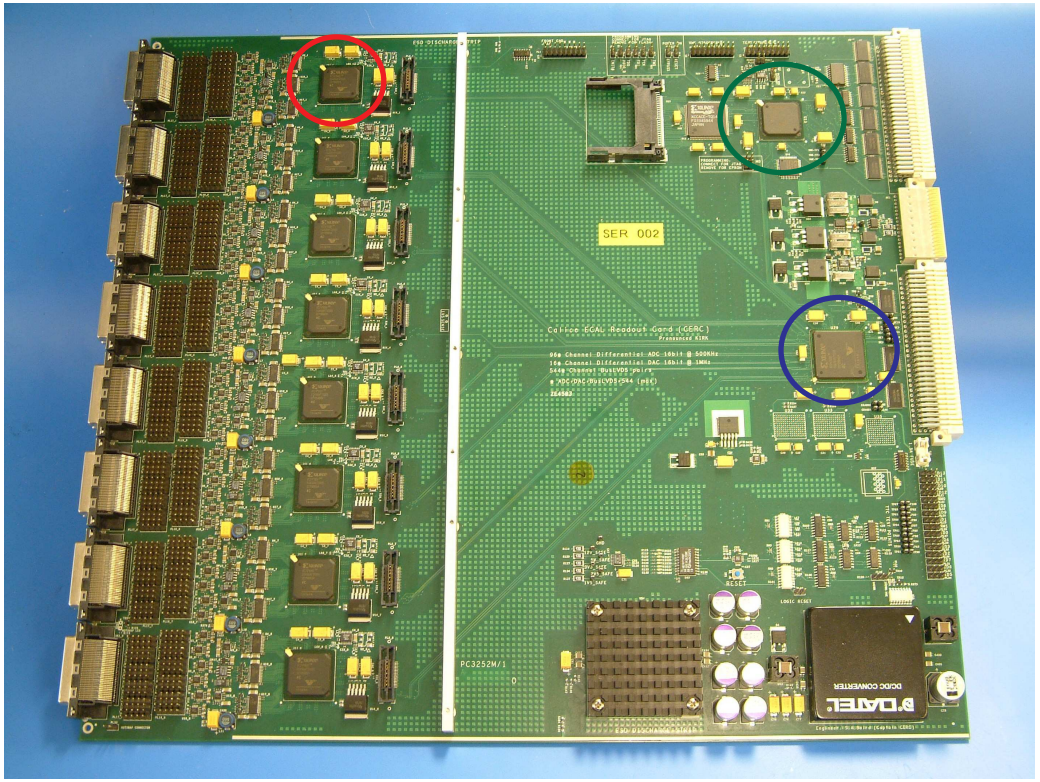
DAQ recent performance

- Current DAQ system is “prototype”
  - Wanted real experience before purchasing final equipment
- Cosmics at Ecole Polytechnique
  - ~2 weeks over Christmas/New Year
  - Ran effectively stand-alone
  - Took ~1M events, ~20GBytes
  - Will allow single pad calibration to < 2%
- Electron beam data at DESY
  - Last ~4 weeks
  - Took ~25M events, ~250GBytes
  - Different energies and incident angles
  - Drift chambers give tracking information
- Now think we know what we want…

DAQ description

- Mainly based on CRC VME board
  - Modified from CMS silicon tracker readout board
  - Firmware in FE, BE, VME



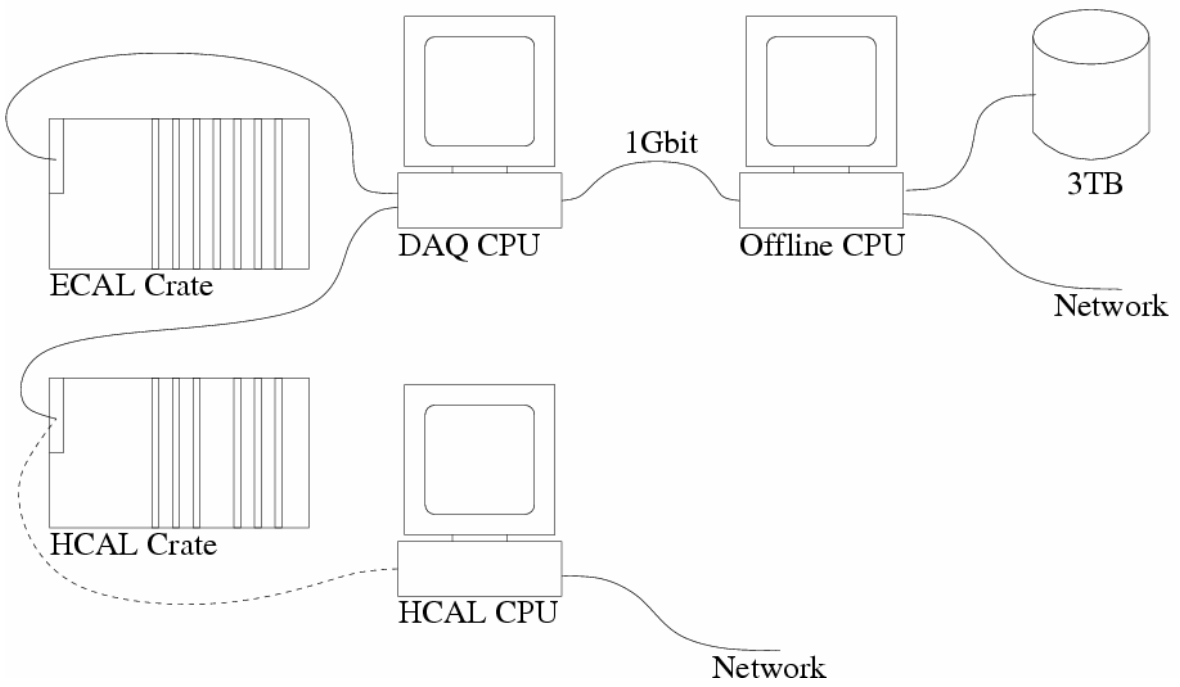


DAQ components

- More than just CRCs; consists of
  - Hardware:
    - Cables, VME boards (CRCs), VME crates, VME-PCI interfaces, PCs and local disk, trigger inputs (? if considered part of DAQ)
  - Firmware: within CRCs
    - FE, BE and BE-Trg, VME designs
  - Software:
    - Trigger handling, spill detection, CRC readout, slow data readout, data formatting, data transport, online monitoring, book-keeping
- Different components at different stages of development

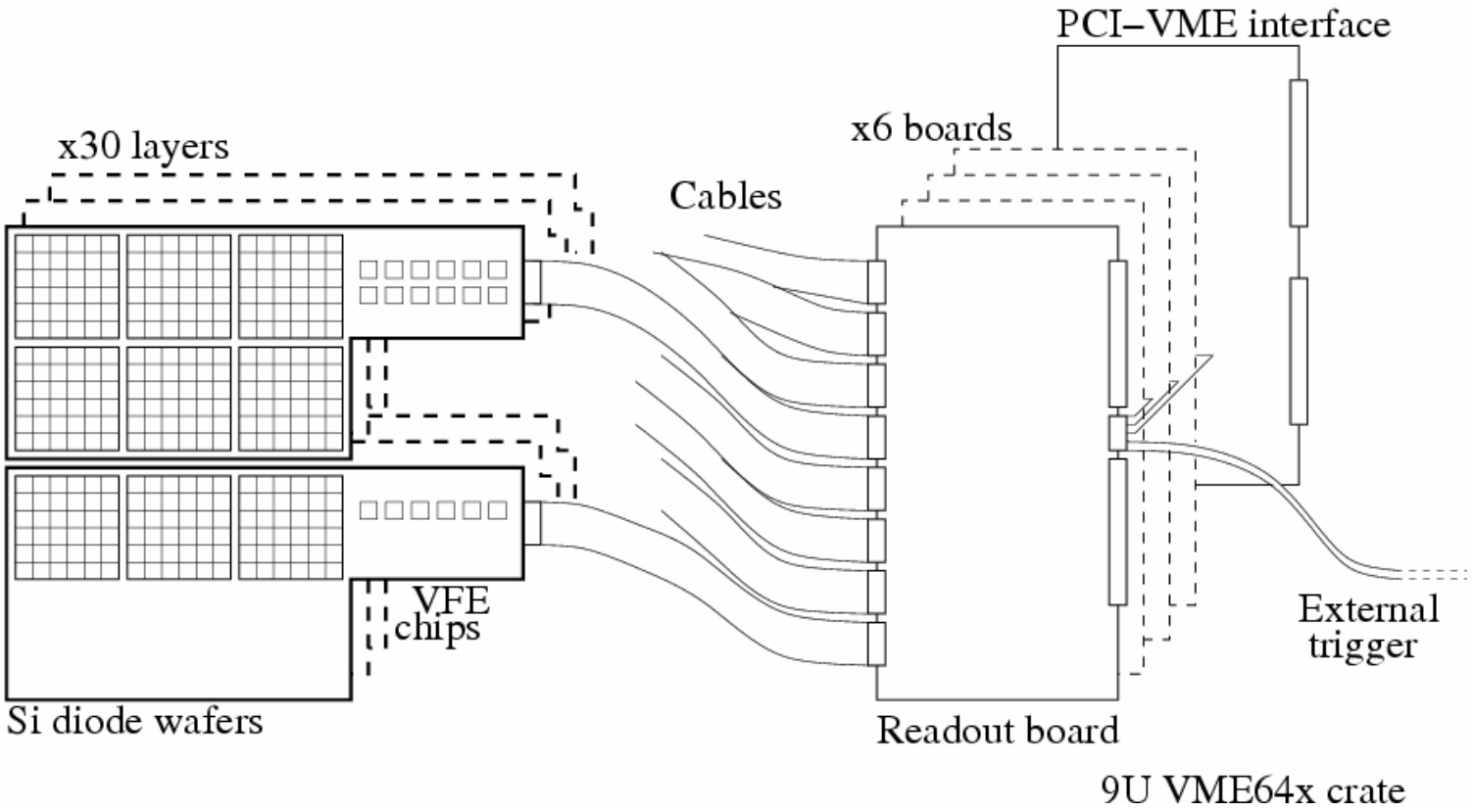
DAQ hardware layout

- DAQ CPU
  - Trigger/spill handling
  - VME and slow access
  - Data formatting
  - Send data via dedicated link to offline CPU
  - Redundant copy to local disk?
- HCAL PC
  - Partitioning
- Offline CPU
  - Write to disk array
  - Send to permanent storage
  - Online monitoring
  - Book-keeping



DAQ trigger distribution

- Trigger information sent to one CRC
- Trigger distributed on custom backplane to other CRCs in ECAL
- AHCAL/TC crate similar; cable connecting backplanes
  - More latency; keep short



DAQ hardware status

- Cables: ECAL needs 60, AHCAL needs 80, tail catcher needs 4
  - ECAL: 70 purchased (DESY and RAL); 5m not 3m!
  - AHCAL, tail catcher: need to decide on length; this summer(?)
- CRCs: ECAL needs 6 (7 if trigger in separate CRC), AHCAL needs 5, tail catcher needs 1
  - ECAL: 2 prototype Nov 2003, 2 preproduction Nov 2004, 7 production Feb 2005; preproduction identical to production
  - AHCAL and tail catcher: 7 about to be ordered from RAL, due Jun 2005
- VME crates: ECAL needs 1, AHCAL and tailcatcher need 1
  - All purchased
- VME-PCI interfaces; SBS620, one per VME crate
  - ECAL: 1 purchased but old PCI format: will buy two more in Mar 2005
  - AHCAL and tail catcher: 2 purchased (one for other use)
- PCs: Need two DAQ, one AHCAL, and disk array
  - Will buy DAQ ones in Mar 2005, AHCAL already purchased

DAQ firmware status

- FE: completely new design
  - Some FPGAs die: SER003/FE0 within minutes, SER004/FE1 after hours but always revive after reset
  - Try to double clock speed used for programmable HOLD offset count
- BE: mostly from CMS but some modifications
  - Expand use of QDR memory from 2MBytes to 8 Mbytes
  - Expand use of control FIFOs from 512 events to 2k events; needs reduction in amount of FIFO data stored
  - Fix bug causing occasional trigger loss
  - Issues to stay in synch with CMS design and tools
- BE-Trg: completely new design
  - Need trigger data to be buffered (in QDR): CRC for trigger only?
  - More trigger functionality needs to be added
- VME: same firmware as CMS
  - No interrupts: need to poll for trigger and spill change

DAQ software status

- Trigger handling, spill detection
  - Within CRC using BE-Trg; no interrupts so polling
  - Use external interrupt generator? HAL VME software does not support them
- CRC readout
  - Good shape, well tested; needs some tuning; event rate limit
- Data formatting
  - Good shape, well tested; will need new formats for new data at FNAL
- Data transport
  - Well tested for file I/O, some tests with socket I/O done, more needed
- Online monitoring
  - Very basic, lots of room for new plots
- Slow data readout (see later)
- Book-keeping
  - Effectively nothing in place

Development schedule

- Continuous running until yesterday (!)
  - No DAQ improvements during this period
- Mar/Apr/May: major upgrades
  - Final PCs, PCI cards, etc, purchased and shipped to DESY
  - Remaining ECAL CRCs tested and shipped to DESY
- Tests in Mar/Apr/May
  - Commission and test hardware (CRCs only arrived 1 month before cosmics)
  - ECAL full system tests; event readout speed tuning
  - ECAL/ACHAL crate integration tests; hope for no firmware changes
  - Slow data readout tests
  - Firmware development
  - Software development, particularly data transport and online monitoring
- Second DESY run, Jun/Jul
  - Complete(?) ECAL

Slow DAQ

- Separate developments of slow control and readout
  - ECAL: movable stage
  - ECAL: VFE power supplies and temperatures
  - CRC: power supplies and temperatures
  - AHCAL: power supplies, LEDs and temperatures
- Current plan
  - Only CRC slow data read out to data files at present
    - Movable stage data only within stage control PC
  - Each will have dedicated control/readout PC
    - Software independently developed, any format internally
  - All passive (read-only) from DAQ side
    - Settings only changed from dedicated PC
    - DAQ data contains uniform access to all slow data
    - Communication via sockets

Event rate status

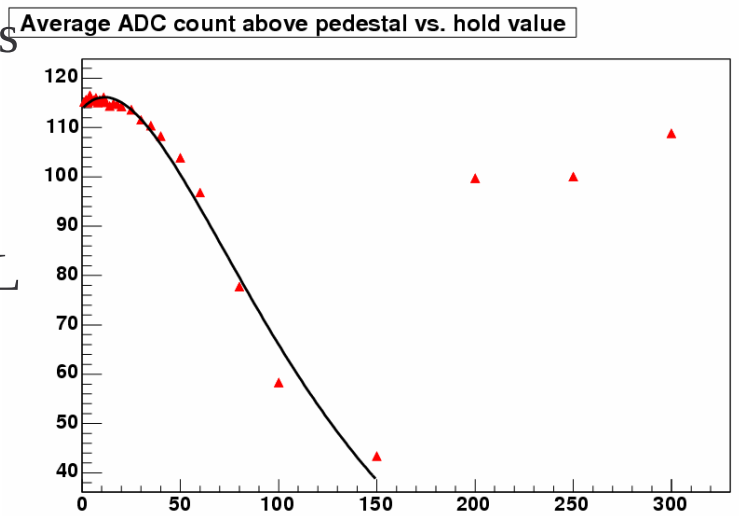
- DESY beam test (using faster AHCAL PC!)
  - Event rate ~ 40Hz ~ 40% of requirement
  - Data rate ~ 400kBytes/s ~ 8% of requirement
- BUT
  - Not CPU limited (factor of 2 faster than with ECAL, but CPU ratio > 5)
  - Lots of slow “configuration” path data (~1kByte/event) read out
- Other measure
  - One board, only QDR data using BDT ~ 330Hz ~ 1.6MBytes/s
  - Six boards ~ 50Hz ~ 50% of requirement
- Issues for study
  - Gains from code streamlining, inlining, compiler optimisation, faster PC
  - VME rate for two PCI cards in dual processor PC with threading

FNAL spill structure

- Original numbers were 0.6 sec spill/min; 1% duty cycle
  - Maximum rate ~ 3kHz to get ~ 2k events/spill ~ 30Hz
- Lengthening spills ~ 5 sec?
  - Only reduces maximum rate needed during spill to ~ 300Hz
  - Average event rate unchanged
  - (Useful for DHCAL as RPCs will be rate limited)
- Now hear only have one spill per two mins!
  - Average rate down to ~ 16Hz
  - Would need to be very organised to average 10Hz overall
- At DESY beam test
  - DAQ average rate ~40Hz with good beam
  - Average ~19Hz overall during last week of running
  - Average ~9Hz overall during previous week

Trigger latency

- Trigger latency remains a worry
  - Must send sample-and-hold to VFE boards at peak of shaped signal
  - Peaking time is ~190ns in ECAL, ~160ns in AHCAL
- Estimated delays at DESY beam test
  - NIM-LVDS module and 1m cable ~15ns
  - Trigger section on CRC board ~20ns
  - Trigger input from backplane to minimum HOLD edge ~40ns
  - Cable and level converter on VFE PCB ~40ns
  - Trigger scintillators, discriminators logic ~15ns
  - Software offset ~ 60ns
- Future uncertainties
  - AHCAL cables; 10m ~ 25ns longer than ECAL
  - Trigger signal timing at FNAL



DHCAL issues

- Many uncertainties here in DAQ hardware and software
  - Also need to make sure trigger and timing compatible with rest of CALICE
  - Move tailcatcher board into ECAL crate (beware for cable lengths)
- Basic statement
  - If data can be read into Linux PC between spills…
  - … DAQ can pull it out and merge with rest of event
- Clearly easiest if similar to AHCAL
  - VME system; two (?) crates with two PCI-VME interfaces
  - Central DAQ PC can have up to 6 PCI cards
- Data volumes
  - 400,000bits = 50kBytes of raw data
  - With NO suppression, event data volume from ~50kBytes to ~80kBytes
  - Only 60% increase and probably rate limited from RPCs
  - Zero suppression would make life even easier