DAQ/Online: readiness for DESY and CERN beam tests

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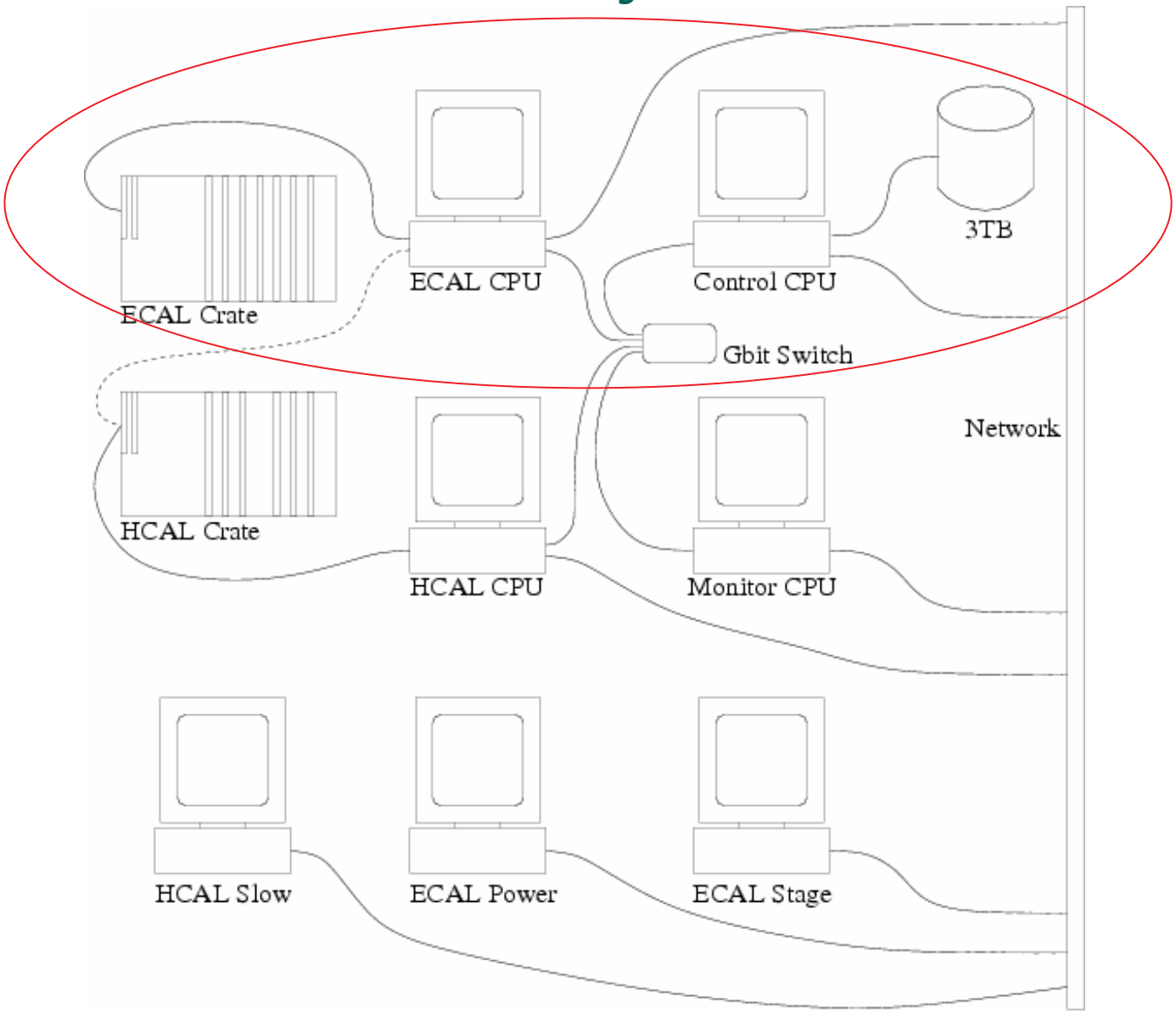
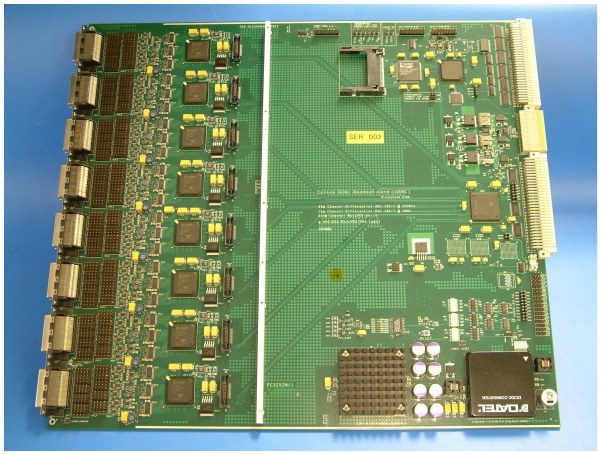
Detailed list of items for DESY and CERN

DAQ hardware layout



"Core" DAQ system

CRC status



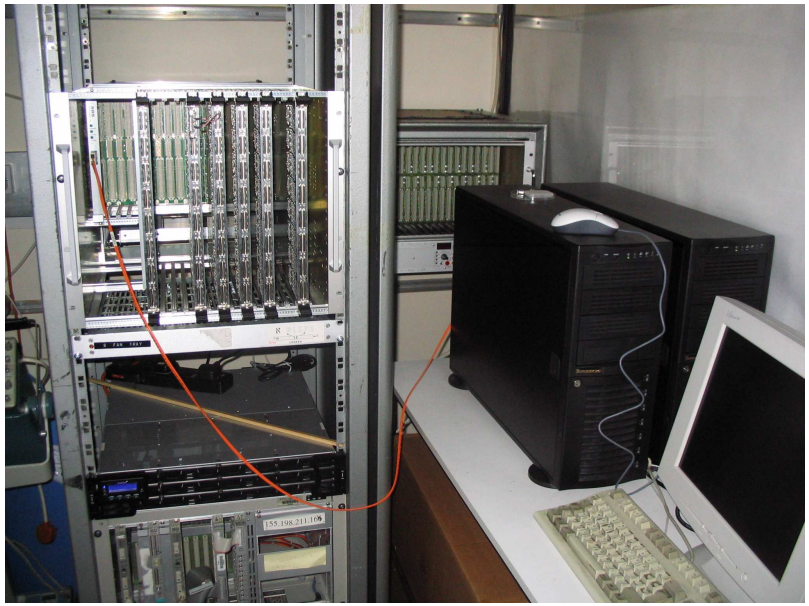
- Progress has been negative L
  - Adam Baird (RAL engineer) has not fixed any more errors on delivered boards
  - 16th board is still with manufacturer with a short
  - Several new bad channels have developed at DESY
- New bad channels are worrying
  - Two correspond to channels which had lower noise in UK tests (but did respond normally to calibration)
  - The others were (apparently) normal
  - Implies problems with this second set arose since arrival in DESY
- Must be very careful in handling
  - Cable connectors known to be a weak point; must always use screws
  - Must strain-relieve cables at crate end; cable-tie to top of crate not to side
  - Must always wear a ground strap; these could be static discharge problems
  - If static, then not fixable; connector trace breaks may be repairable

Need to plan CRC use carefully

- Need to determine exact size of the problem
  - How many bad channels now exist? Must use a VFE PCB to be sure
  - Need systematic test of every FE connector input; who will do this?
  - If problems seen, need to check alternative FE connector
  - Also check if input is connected through to first stage of ADC circuit
- Adding bridging wires for broken traces can be done
  - Probably best for Adam to do this; need to be done in the UK
  - Do we return boards to the UK? Need to be sure enough left at DESY
  - Need (realistic) schedule for ECAL/AHCAL module delivery The numbers…
  - I believe we have around 98 fully working FEs, spread over 15 CRCs
  - Most of other 22 have one or two bad channels; 8 have bad FEs
  - Total required for final system is 90 so this is not comfortable
  - Total required for ECAL run next week is 26 (plus a few for AHCAL)
  - Total required for CERN runs?

DAQ core hardware

- Core DAQ system shipped to DESY
  - Timing set by preparations for ECAL run
  - Other two DAQ PCs already at DESY
- Still need to test CRCs in the UK
  - Repairs by Adam of broken traces
  - Debugging last CRC when short fixed



- Set up test system in borrowed crate and VME interface at UCL
  - Not SBS bus adaptor so completely different driver/VME access underneath
  - Hacked HAL DummyBusAdapter to interface DAQ code to hardware
- Allows some level of checks and code development…

  …but many things can now only be done at DESY
  - SBS driver issues, speed-ups, inter-PC communication tests, etc.
  - Will cause disruption to run if not scheduled carefully

Other hardware for DESY

- New custom backplane installed at DESY
  - Inter-crate trigger cable made and whole trigger path tested; worked OK
  - Following test, second (~spare) backplane being made at Imperial
- Other PCs exist and connected to local network
  - AHCAL PC installed by Marius and Roman
  - Monitoring/histogramming PC installed and running, due to Götz, George, and Roman
- Control PC nfs mount of 3TByte disk array
  - Other PCs connected to DAQ local network can see data directly
- VFE-CRC cables purchased a long time ago
  - Not halogen-free so cannot be used at CERN
- TDC for drift chamber readout revived by Michele and Erika
  - Used to measure performance of chambers with non-flammable gas
  - Results on this presented during meeting (?)

Slow controls/readout

- ECAL power supply control (Simon)
  - Read out via stand-alone PC; will need to interface to DAQ
  - I have no replies to emails on this
  - It will presumably not be read out for ECAL run L
- ECAL stage position (Bernard/Didier)
  - Stage controlled by stand-alone PC
  - Readout interface to DAQ tested and working a year ago
  - PC OS was patched and registered at DESY yesterday
  - Currently checking interface still works
- AHCAL slow data and stage position (Sven)
  - All centralised in stand-alone PC (running H1 slow control program)
  - Readout and control interface to DAQ tested; stage position controllable
  - Finalising definition of other data this week; needs more work to complete
  - Must add beam line settings data when we get to CERN

CERN tracking

- We can borrow CERN delay wire chambers
  - Finally got information at CERN meeting last week!
  - Each chamber is $10 \times 10 cm^2$ and has x and y readout
  - Each x and y readout by lumped delay line in both directions
  - Delay timing gives 0.2mm/ns, resolution is 200μm
  - CERN provide gas, we need to provide HV and readout
- We requested four chambers but may only get three (or even two)
  - Investigate shipping Japanese chambers from DESY
  - Then need to provide gas also, safety issue with flammable gas again
- Need to have a TDC which can buffer data during spill
  - Needs up to 16 channels, range > 500ns, LSB < 1ns, buffer > 2k events
  - DESY LeCroy 1176 TDC has only 32 event buffer L
  - Got a CAEN V767 TDC out from CERN loan pool (yesterday)
  - 128 (!) channels, 800μs range, 0.8ns LSB, 32kword buffer J
  - Needs to be tested to be sure will do the job; use for ECAL run?

CERN tracking fallback

- Use DESY TDC (assuming OK to take it; it belongs to Zeus!)
  - Can only buffer 32 events so must read out during a spill
- Only read TDC but not CRCs during spill
  - Will severely limit 1kHz trigger rate during spill
- Several tricks to try
  - Reduce data volume by turning off falling edge readout
  - Buffer for 32 triggers and read all 32 at once by block transfer
  - Parallel read ahead while rest of DAQ does other processing
  - Would make offline access different (and more complicated)
- Never been tried; if managed to get 150Hz (random guess)
  - During 4.8sec spill, would take ~700 events
  - Average rate over 16.8sec machine cycle then ~40Hz
- Can test rates at DESY but need realistic occupancy, i.e. beam
  - Again may disrupt ECAL run

CERN PID

- Cherenkov detector, ~50m upstream
  - Mainly for e/π separation
  - Threshold Cherenkov; threshold must be adjusted for each beam energy
- Beam control software being upgraded for LHC
  - Same software does threshold adjustment
  - Not clear if it will be ready in time for first CERN run
  - Fallback would be adjust by hand; limits ease of changing beam energy
- If usable, readout is trivial
  - Single discriminated logic signal fixed in time relative to the trigger
  - Simply convert to LVDS and input to trigger CRC
  - CRC trigger data records history of all inputs
- In principle, could also be included in the trigger
  - In practise, arrival time is probably too late given our latency
  - Must select events offline which have this bit set

Other hardware for CERN

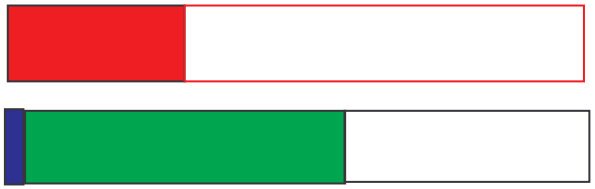
- Halogen-free cables for VFE-CRC not yet in hand
  - A few ordered by Felix for test but not yet delivered
- Cables for ~30m run from barracks to experimental area
  - VME readout; one 100m FO cable per crate. Only one purchased, other ordered by Erika but not yet delivered
  - ECAL slow data; 30m (?) copper cable but may be marginal in length. Jean-Charles may convert to fibre optic?
  - ECAL stage; Didier extended to 60m copper RS232 cable, exists
  - AHCAL slow data; two 100m FO cables, Sven ordered but not yet delivered
  - Cable to take beam spill signals from barrack to experimental area; two TTL 60m lemo cables, do not exist; who can provide?
- Can take both existing VME crates to CERN
  - Erika borrowed addition equipment for AHCAL module test stand at DESY
  - Extra VME crate, SBS card set in hand
  - Allows new module testing to continue at DESY during CERN run

Firmware status

- Main issue is buffering event data during spill
  - Firmware currently used on CRCs at DESY is limited
  - Can only buffer up to 500 events, but need 2000
  - Can only buffer in 2MBytes of memory, but need 8MBytes
  - Irrelevant for DESY; read event by event
- New version under development in UK
  - Using full 8MBytes of memory now possible J
- Remaining problem is event counters/memory control
  - 1000 event FIFOs hit FPGA gate limit L
  - Need to rewrite firmware for FIFOs to get around limit
- Will fully debug a 1000 event/8MByte version
  - This will be the fallback for CERN
  - But will push to covert the FIFOs to handle 2000 events also
  - Impossible to predict when this will be completed

Firmware fallback

- What could we do with only 1000 event buffer at CERN?
  - Spill structure is 4.8sec beam, 12.0sec deadtime
  - Assume trigger rate of 1kHz, readout rate of 100Hz
- Simple approach
  - Take 1000 triggers to fill 1000 buffer in ~1sec
  - Read out 1000 events from buffer in ~10sec
  - Wait for next spill for ~5.8sec
  - Averaged event rate ~ 1000/17 ~ 60Hz



- More complicated approach
  - Take 350 triggers in ~0.3sec
  - Read out 350 events from buffer in ~3.5sec
  - Take 1000 triggers in ~1sec
  - Read out 1000 events in ~10sec
  - Wait for next spill for ~2.0sec
  - Averaged event rate ~ 1350/17 ~ 80Hz

Would require careful tuning with exact rates to optimise

Integration tests

- Have been doing ECAL/AHCAL combined runs for months
  - Using single crate with software cludged to make it look like two crates
  - Appears to all other software as if two separate crates
- DAQ core system at DESY finally allowed true dual-crate test
  - All PCs connected via local Gbit switch
  - Guarantees bandwidth independent of external network
- Tested two crate read using two PCI cards in same PC
  - Disappointing result; parallel read no faster than serial read L
  - Looks like SBS driver blocks more than one process
  - Only one VME access at once, even if to two different crates
- Tested two crate read using two PCI cards in two PCs
  - Coordinated by sockets; worked well and gave almost double rate J
  - 12 full CRCS (approx full load) were read at 120Hz flat out
  - Realistic rate in non-optimal conditions plus TDC; might be a little slower?

Data integrity

- Workaround for VME bus error causing exception
  - Catch exception immediately and retry read; never seems to fail twice
  - Has been stress tested and does not cause problems
  - Fundamental cause not yet understood; still monitoring frequency
- Some events missing trigger
  - Due to trigger occurring at same time as trigger BUSY reset
  - BUSY is never lowered, so next trigger does not happen
  - Now detected in software; retry reset when this occurs
  - Has been stress tested and does not cause problems
- VME driver cannot handle signals (Ctrl-C, etc) correctly
  - Signals were used to start runs, end runs, end program, etc.
  - Sometimes get corrupted data if reading when signal arrives
  - Have rewritten control to avoid use of signals; now uses shared memory
  - This has been installed and is running without problems

Upcoming software improvements

- Trigger handling not flexible enough given all ongoing activities
  - Needs recompile or rewiring to go from ECAL-only to AHCAL-only
  - Solution straightforward; would also fix a few other issues
  - Would require significant testing to ensure each run type has the right trigger
- Run sequences requested
  - Predefined lists of runs which can be executed sequentially
  - No intrinsic obstacle, but quite a lot of infrastructure; under development
- Speed up for online monitoring histograms
  - ROOT very general but memory management makes it slow here
  - Could replace data storage with much simpler (faster) system
  - Display would still be done using ROOT so would appear identical
  - Also, whole histogram filling code could run in parallel process
- Speed up for data readout
  - Read-ahead for event data when otherwise hanging for next record

Non-technical issues

- DAQ is critically short on effort
  - I've been on about this for ages
  - Flagged up in the last Technical Review
- Expert coverage for DESY and CERN currently two people
  - Core code is me, Marius is now AHCAL expert
  - Nobody yet identified as equivalent for ECAL
  - No other volunteers have stepped forward
  - Lots of things to do before/during CERN run; let me know if you can help
- Started running shifts at DESY with non-experts
  - Not very smooth; some bugs/features found
  - Main errors were operator mistakes due to lack of documentation, clear rules and communication problems
  - Anne-Marie and Erika have since produced much better instructions:

    http://www.hep.ph.imperial.ac.uk/calice/testBeam/testBeam.html

Summary

- DESY ECAL run
  - Hardware mainly in place or on order
  - Firmware is functional
  - Software is functional but needs further documentation
  - Slow controls needs some work
- CERN runs
  - Still several hardware pieces missing but most on order
  - Firmware not fully functional but fallback is not a disaster
  - Software will have to be flexible as running mode not yet known
  - Extra slow controls work for beam line settings
- Have functioning independent UK test system
  - Required for CRC repairs
- Will have independent DESY test system
  - Required for testing AHCAL new modules before being sent to CERN