# Progress on the future DAQ

**Matthew Wing - UCL**
**(on behalf of the CALICE-UK DAQ groups)**

**Cambridge, Imperial, Manchester, RHUL, UCL**

- **Preamble**
- **ASICs and data transportation on the PCBs**
- **Networking and on/off-detector communication**
- **Off-detector receiver**
- **A (paper) model DAQ**

# Preamble

**Thinking of a future DAQ system, have a conceptual design: commercial, back-planeless, etc.**

**Basic R&D to investigate issues with this concept. Keep on top of technology.**

**Idea that it could be used for future detectors (calorimeter) and prototypes.**

**As well as bench-testing and “generic” R&D, committed to provide DAQ for EUDET module.**

**Report on progress: model slab and PCI card.**

# ASIC testing

**To test new rounds of ASIC chips for noise, pedestals, etc. and feed back for the next production.**

**Will do tests of single chips and also many chips.**

**Expect chip to be fabricated by February 2007.**

**Continue process for expected rounds of production.**

# Model slab

**Plan**

- **emulate multiple VFE chips on long PCBs**
- **study transmission behaviour: noise, cross-talk, etc.**
- **optimise VFE PCB with respect to data-rate requirements**

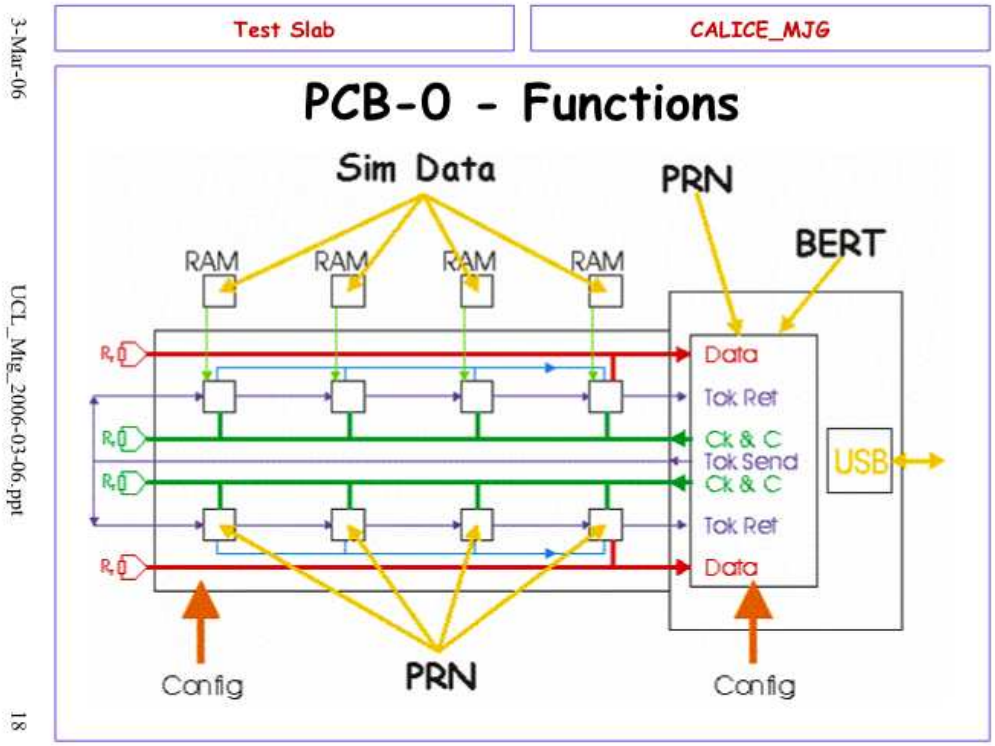
**Needs**

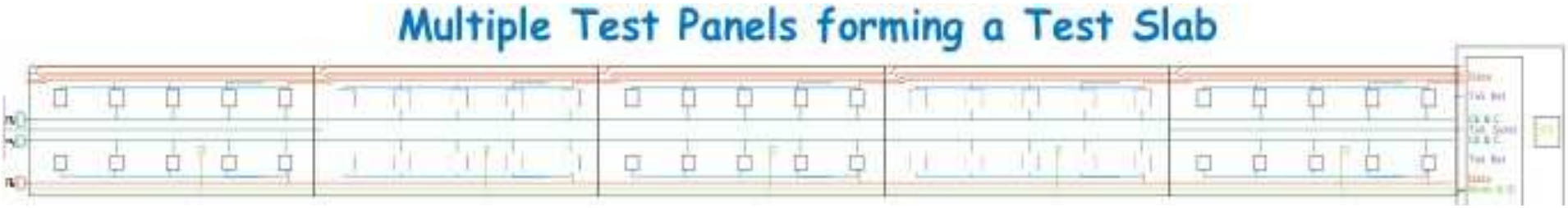
- **segmented test slab PCBs**
- **FPGAs emulating VFE chips, “pVFEs”**
- **FE boards for distribution and reception of clock, controls, data, etc.**

**Will feed into ASIC and PCB design for EUDET (and final) modules**

**Will have designed and constructed FE board - feed into future real modules**

# Model slab layout



# Board design and layout

**Assumed:**

**5 $\times$ 5 mm$^2$ pads, 72 channels/ASIC $\rightarrow$ 1 ASIC covers 6 $\times$ 12 pads, or 3 $\times$ 6 cm$^2$**

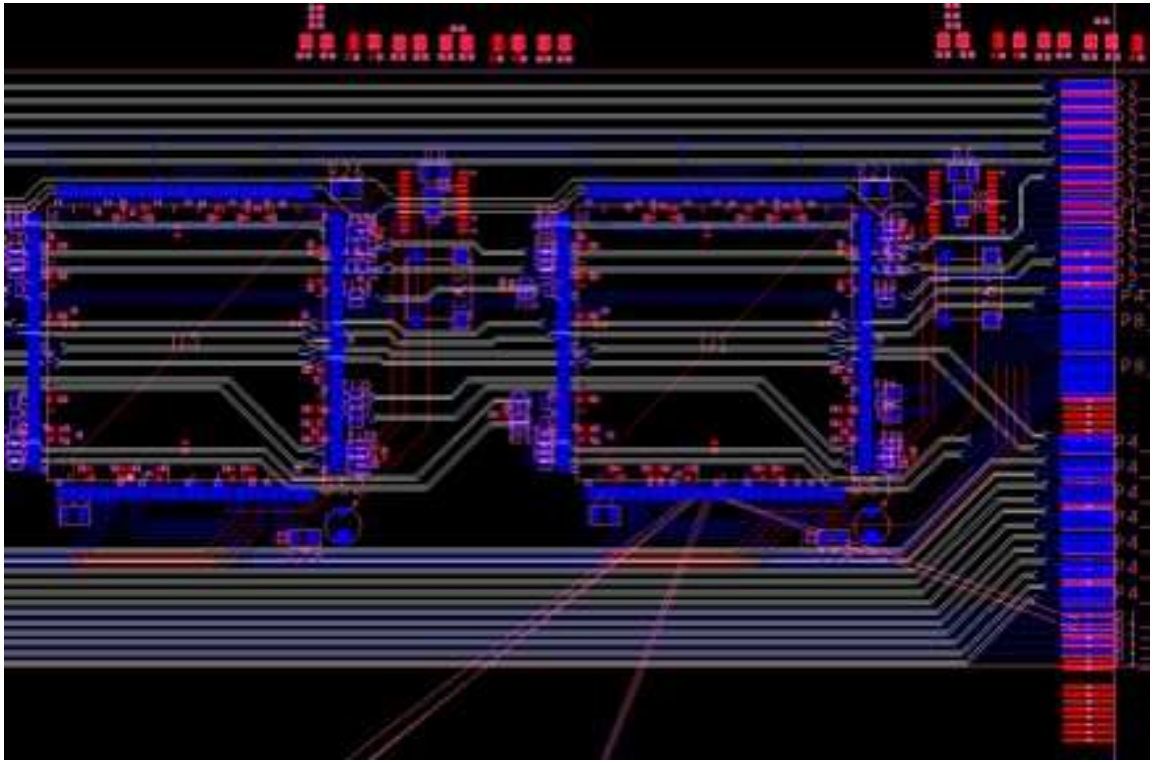
**Thin 64 $\mu$m layers and narrow 75 $\mu$m traces**

**Traces for various clock distribution and/or readout architectures incorporated**

**Row of 4 FPGAs per board**

**Every FPGA mimics 2 VFE chips**

**A row of FPGAs is equivalent to VFE covering 24 $\times$ 6 cm$^2$**



**Schematics finished, layout almost finished.**

# pVFE FPGA progress

**Simulation of actual VFE VHDL code using VFE technology specific SRAM**

**Modification of VFE code and simulation using FPGA SRAM**

**VFE chips incorporated in VHDL test-bench**

**Suggestions incorporated into VFE VHDL code**

**VFE chip plus test-bench running on Xilinx Spartan3E FPGA**

**Two chips plus test-benches fitted into single FPGA**

- **25% of logic used**
- **83% of block RAM used**

**Preliminary code for alternative pVFE implementation**

**Model slab to be finished soon and ready for tests**

# Networking and on/off-detector communication

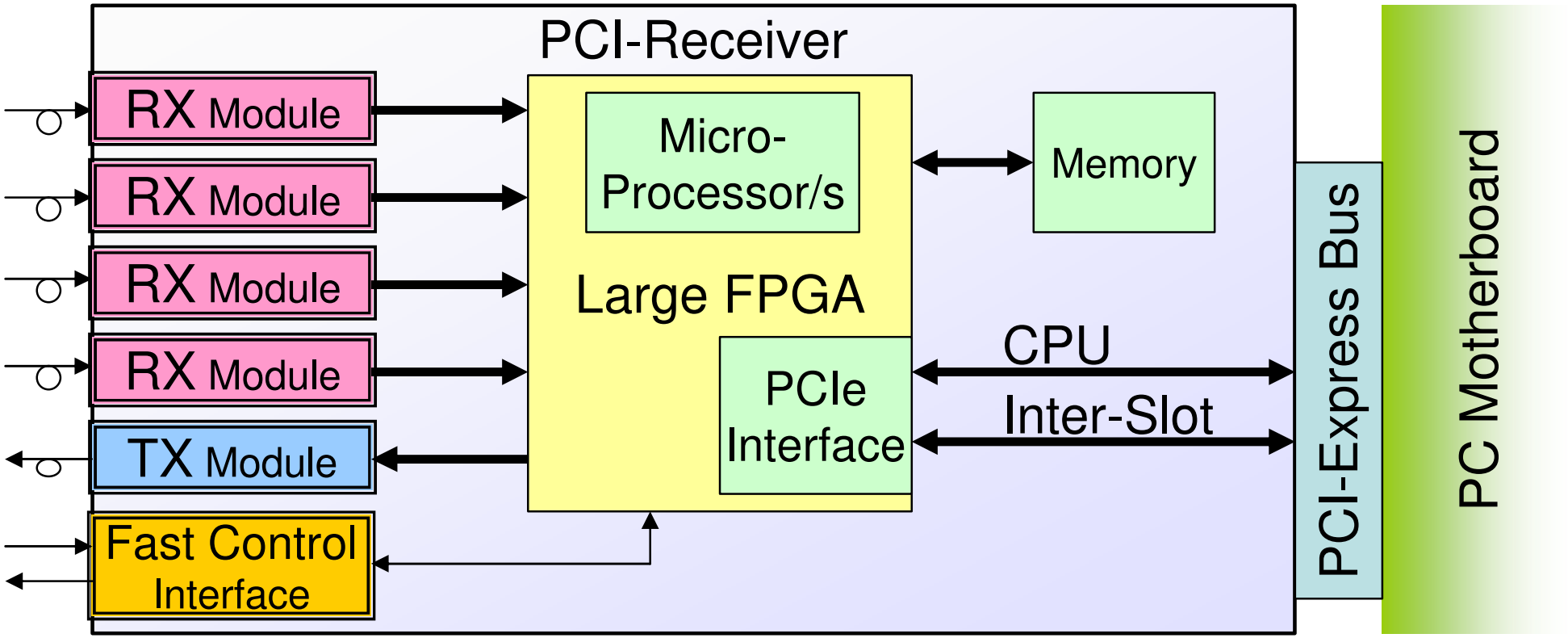
**Conventional network switches:**

- **testing ultimate performance of PCI Express - cope with high data rates, bundle system into fewer components.**
- **use PCI card: set-up so measurements can be made.**
- **series of tests done for other systems, PCI-X, ethernet, to be repeated.**

**Off- to on-detector communication:**

- **Monte Carlo simulation of radiation environment around FE electronics**
- **Evaluation of SEU effects on FPGAs**

# Off-detector receiver design




**Custom design (using commercial components) and fabricate**

**Couple of rounds of iterations and final board ready**

# Off-detector receiver PCI card

**Simpler to just buy(!) the cards**

# PCI cards - specs

**Bought PCIe cards from PLD applications (http://www.plda.com/):**

- **model: XpressFX100**
- **FPGA: Xilinx Virtex-4 FX100**
- **bus: PCIexpress x8 lane.**
- **Gbit optical and copper transceivers**

**Hosted in computers in our labs.**

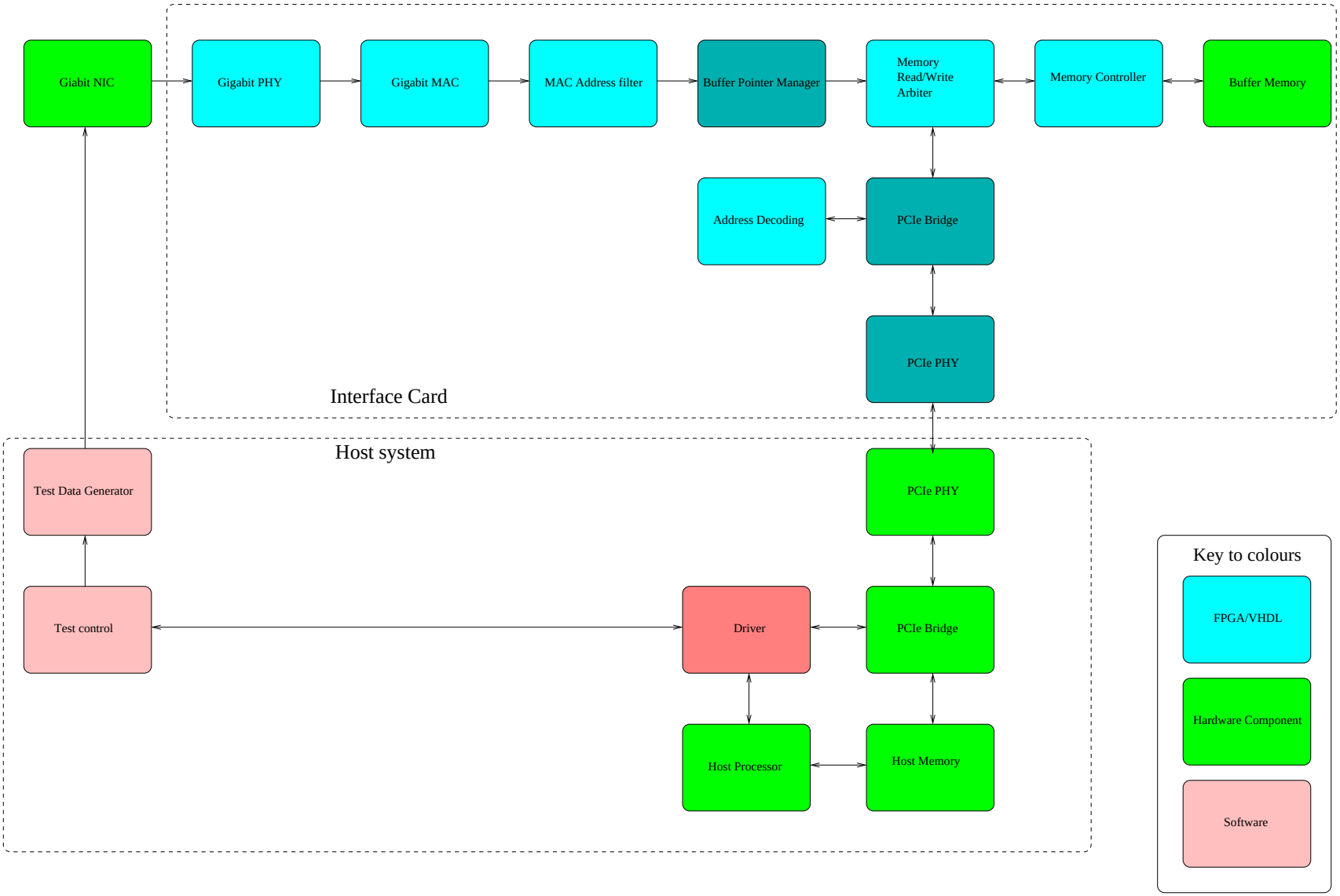
**Working on firmware and test software**

# PCI cards - tasks

**Have a box diagram of a structure for passing data in such a system.**

- **writing firmware for each box (several people: one person per box)**
- **collected in central repository**
- **first goal is to get data to be read into (and out) the host memory and measure the speed of throughput.**

# PCI cards - box diagram of Stage 1



# A (paper) model DAQ

**Gives (order of magnitude?!) idea of scale of system. Useful for C/TDRs, can highlight problems.**

- **Assume ADC and thresholding done in 32-channel VFE, buffering in FE.**
- **Calorimeter/accelerator**
  - **Tesla 800 GeV bunch structure**
  - **$24\times10^6$ Si pads; 6000 slabs; 40 layers,**
- **Data size and rate:**
  - **Raw data 2 Bytes/channel, additional 4 Bytes/channel for a timing label**
  - **Threshold $\rightarrow$ 100$\times$ reduction $\Rightarrow$ ($24\times10^6 \times 4886 \times 6$)/100 = 7.0 GBytes or 1.2 MBytes/slab.**
  - **Buffering in FE $\Rightarrow$ rate = 4.7 MBytes/s/slab.**
  - **Bundle half a tower, 20 slabs together, for a rate of 0.75 Gbit/s per fibre.**

- **Components off the detector:**
  - **300 fibres.**
  - **assume a PCI card can receive 8 fibres $\Rightarrow$ 38 PCI cards.**
  - **assume a PC holds 2 PCI cards $\Rightarrow$ 19 PCs.**
  - **allowing 20% contingency (redundancy, faulty PCs) $\Rightarrow$ 50 PCI cards and 25 PCs.**

**A manageable system.**