General work on the DAQ system - From the slab backwards …

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Overview

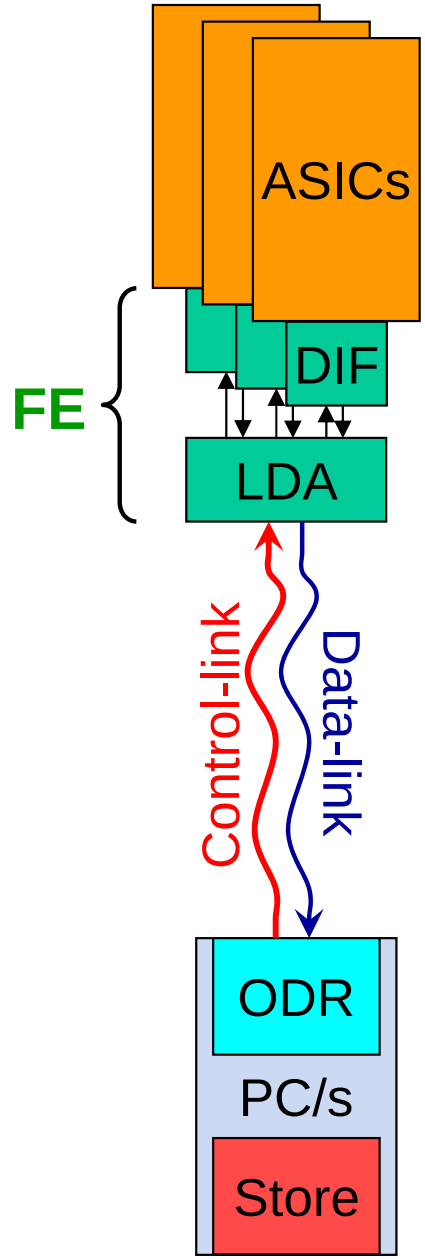
1. CALICE-DAQ

2. Optical Switch

3. Single Event Upsets

DAQ Structural Overview

- ASICs
- Front-End (FE)
  - -FE-Interface (DIF): Detector specific
  - -FE Link/Data Aggregator (LDA): Generic
- Data-link (FE to Off-Detector Receiver)
- Control-link (C+C to FE)
- DAQ PC
  - -Off-Detector Receiver (ODR)
  - -Control data-link (Clock, Control to FE)
  - -Data Store

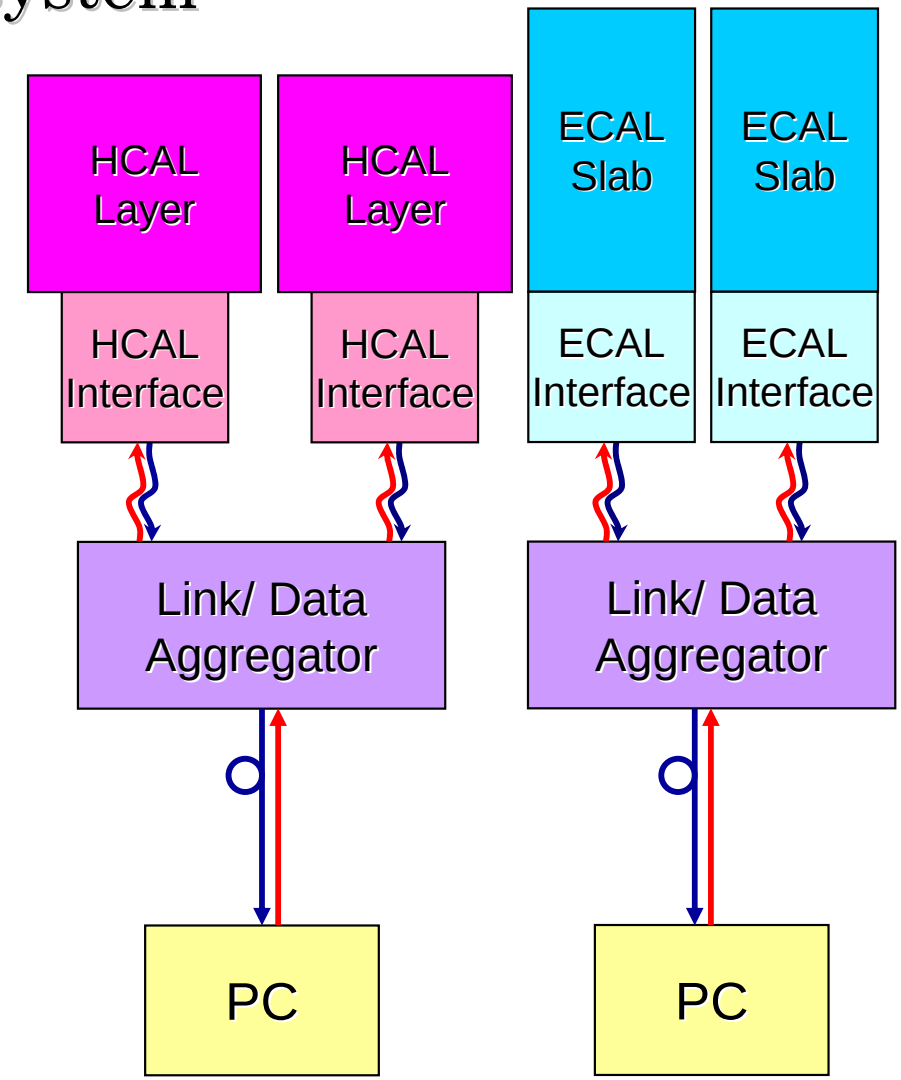


FE Structure Detail

We have 2+ types of detector to readout.
Divide the FE into a 2 part, tiered system

1) Detector Interface module (DIF)
   - -Detector specific interface
   - -Includes power connectors
   - -'Local' systems (e.g. clock)
   - -Debug connectors

2) Link/Data Aggregator module (LDA)
   - -Collects data from many 'DIF's
   - -Drives data Off detector link
   - -Receives and distributes C+C



BUT:

We would probably like to read-out slabs individually first…

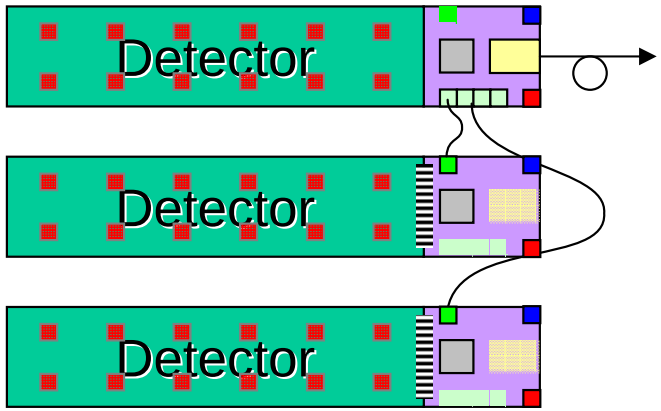
FE – More thoughts

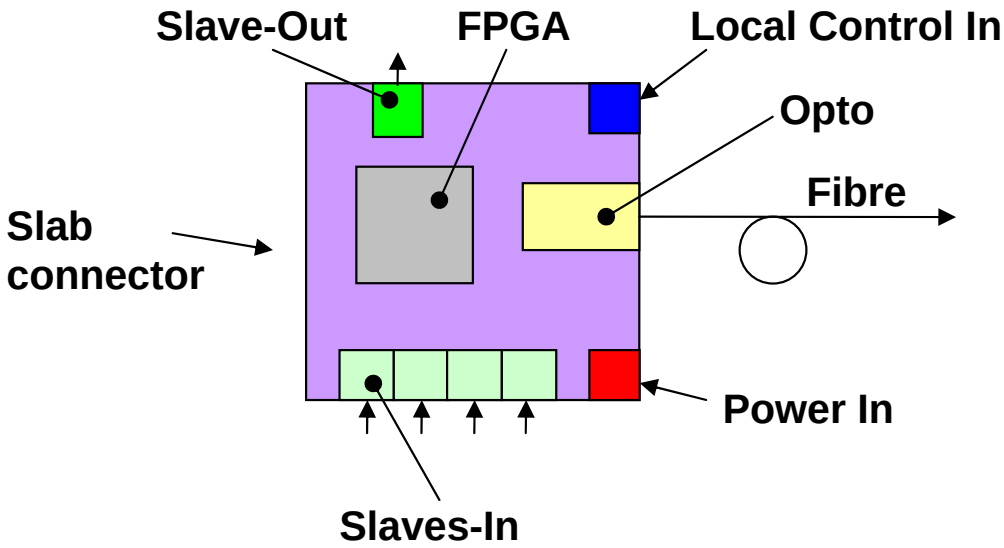
- Each DIF can connect directly to an LDA for stand-alone operation

OR

- Combine on single PCB, with single FPGA
  - -Capabilities depend on PCB loading
  - -Operate as stand-alone, or as master-slave (aggregator)
  - -Firmware development 2 tiered

Eg: ECAL:





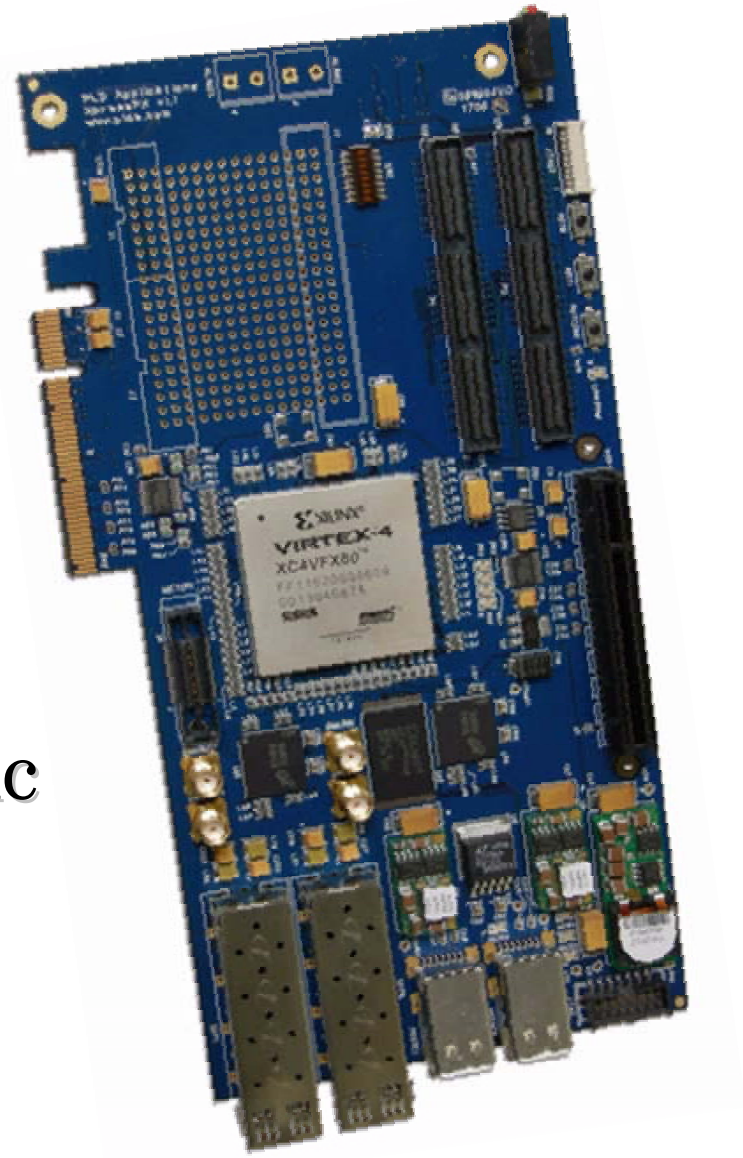
Data-link (+Control)

- Plan to use most common networking fibre-optics:
  - -Multimode with LC connectors
  - -SFP (mini-GBIC) interfaces
  - -1Gbit rate
  - -Ethernet

- Control up-link NOT via fibre, ***initially***.

Off-Detector Receiver (ODR)

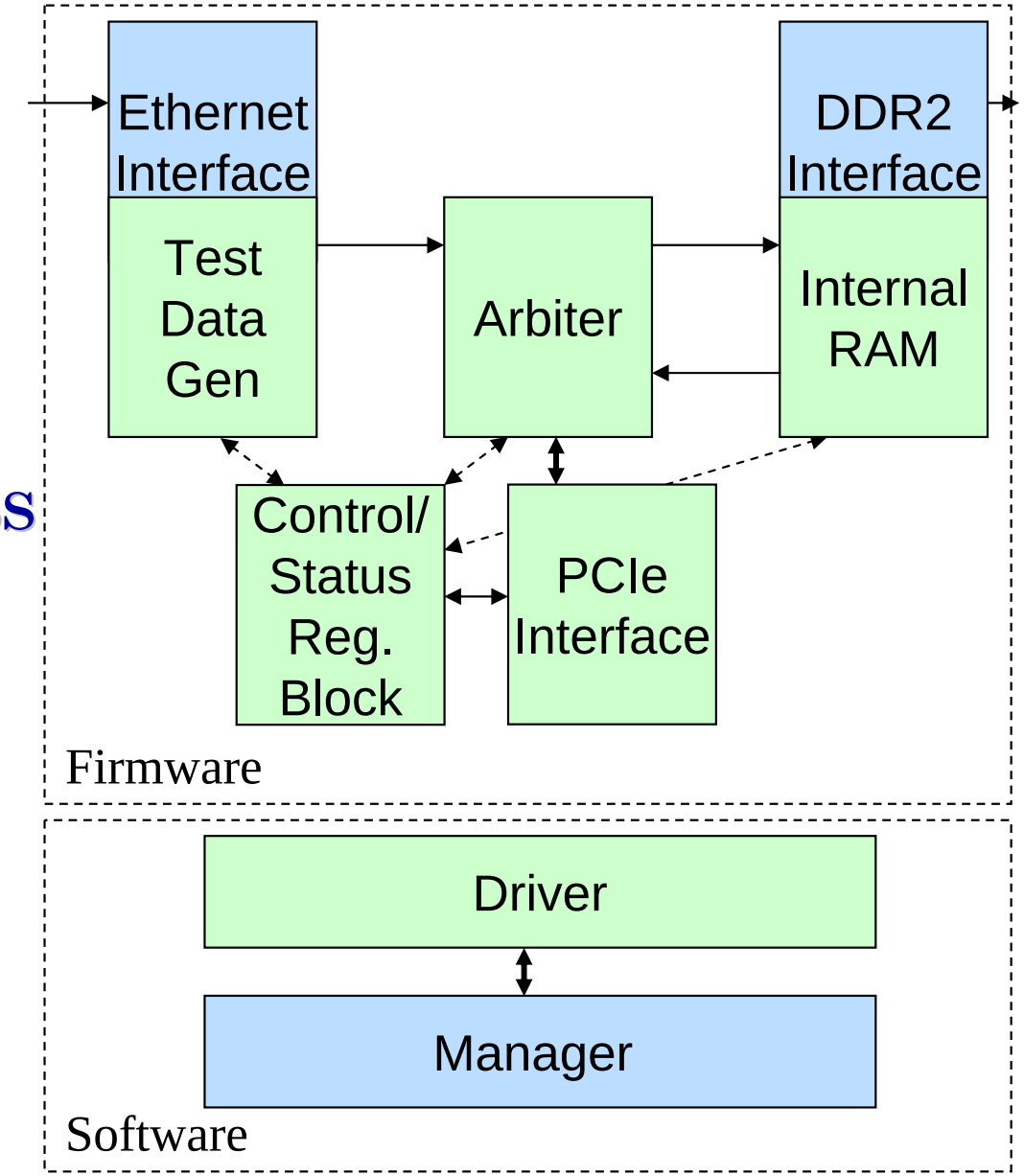
- PCI Express Card
- Virtex 4, FX100 FPGA (big!)
- Hosts opto-links
  -2xSFP, 2xHSSDC2 on board
- Source of C+C (Control link)
  -Initially copper (SMA connectors?)
  -Later fibre
- Will use external clock and sync signals for multi-PC operation



ODR(2) - Status

Firmware AND software well underway:

- PCIe interface **DONE**
- Register read/write **DONE**
- DMA access **DONE**
- Ethernet Interface
  IN-PROGRESS
- DDR2 Interface **IN-PROGRESS**
- Linux driver **DONE**
- Manager Software
  IN-PROGRESS
- Performance profiling
  IN-PROGRESS
- Clock and Control Uplink
  NOT-STARTED



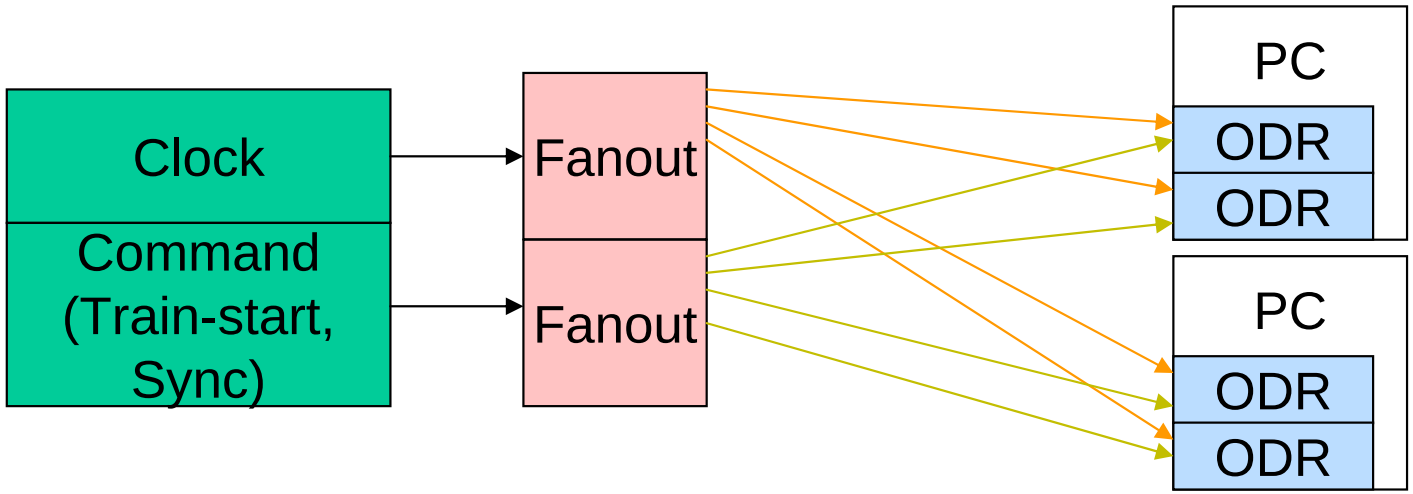
Datastore and Integration

Keep it simple!

Event files written to local disk

System synchronising signals distributed

-All data tagged with common ‘timestamp’



UK Read-out work (ECAL FE)

Detector Interface (Cam)
- Spec + hardware

DIF to Link/Data Aggregator (Cam/Man)
- Spec + hardware

Data aggregate, format (Man)
- Hardware + firmware

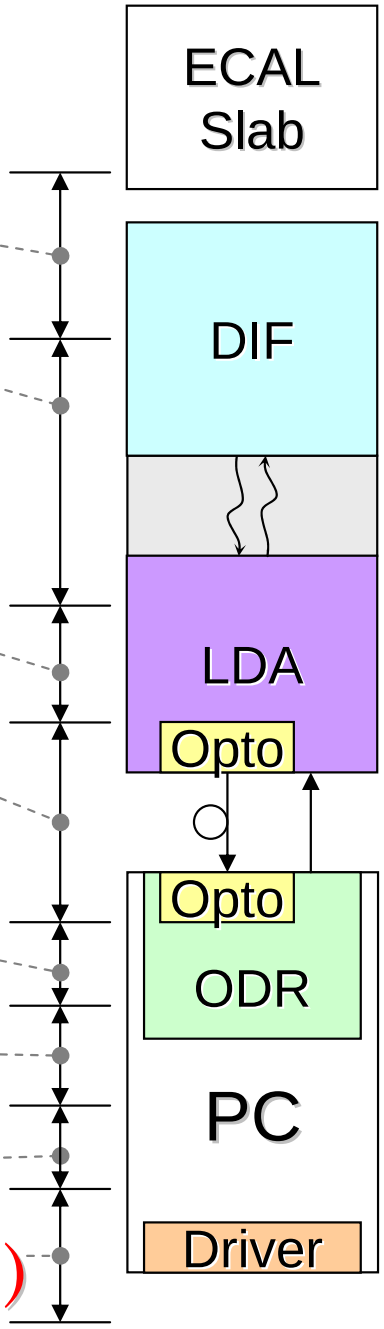
LDA to ODR opto-link (Man, UCL)
- Hardware + firmware

ODR (RHUL, UCL, Cam)
- firmware

ODR to disk (RHUL)
- Driver software

Local Software DAQ (RHUL)

Full blown Software DAQ (RHUL, UCL, [IC])



DAQ Summary

UK proposes to do large part of readout chain

[we can fight independently!]

Key areas for development identified:

- Baseline structure
- Work segmented

ECAL will be looked after entirely by UK

- HCAL may need to manufacture own FE PCB

Optical Switch

Optical (Layer-1) Switching

Part of the UK project is to evaluate the use of a "layer-1" switch.

This switch physically (re)connects fibres

It can be used in various ways:

1) DAQ PC failover

   Redirect data to spare unused DAQ PC on the fly

2) "Router" (able to switch at >10Hz for many years)
   - Can change data destination per bunch-train.
   - Regulate load by sending data directly to free resources

3) Programmable optical patch panel (large installation)
   - Easily switch to redundant fibres remotely
   - Useful for grouping fibres from physics region (e.g. logical grouping)

Switch Unit Purchased

- Manufacturers offering similar products, in same price range e.g. Glimmerglass, Polatis - difficult to differentiate between them
- Decided on Polatis
  - -can switch dark fibre (i.e. not MEMS based)
  - -Multimode fibre capable
  - -Fastest switching time (20ms)
- 16x16 array with 50µm multimode LC connectors

Single Event Upset Studies

Single Event Upsets

Attempting to find out expected SEU rates in FE

- Influences choice of technology for final FE
- Influences re-configure/reset rate of FE

SEU rates very dependent on hardware, and we have none!

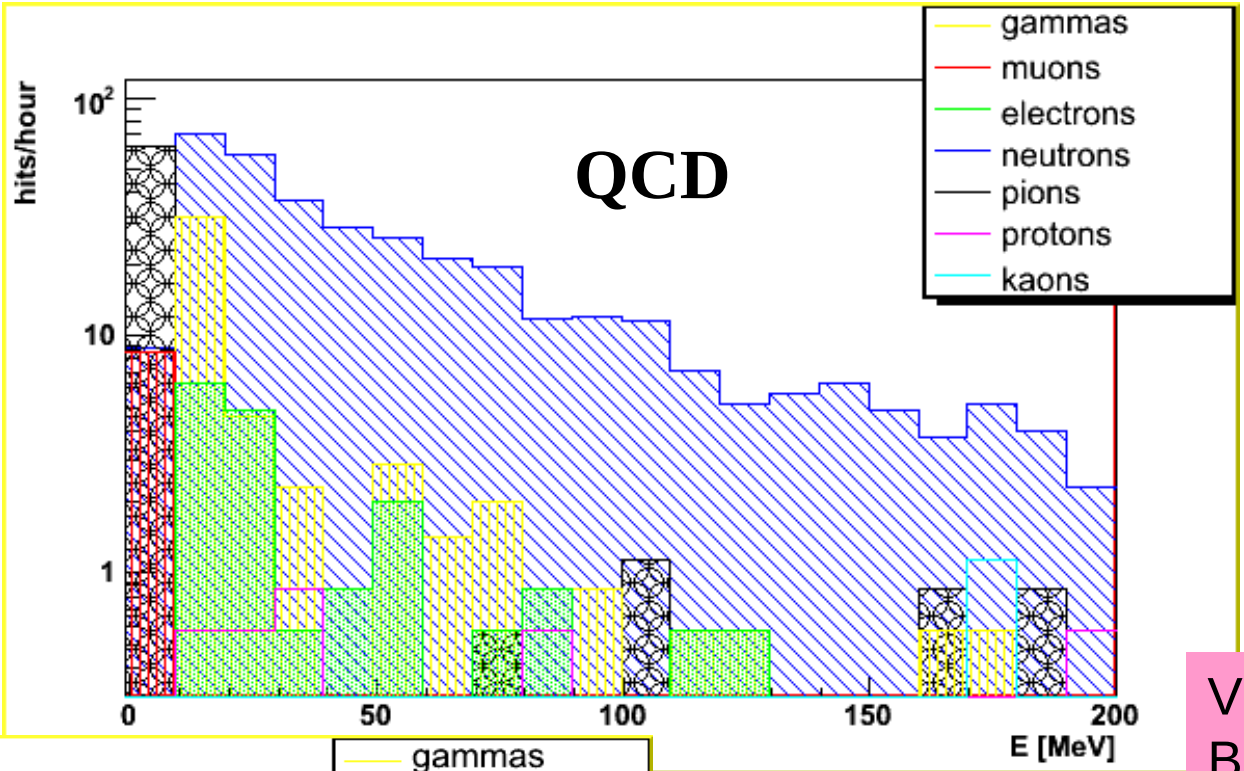
- Attempting to provide framework and data for use when making hardware decisions later

- We have simulated the expected environment at the end of ECAL slabs.
- Results are compared with existing FPGA measurements.

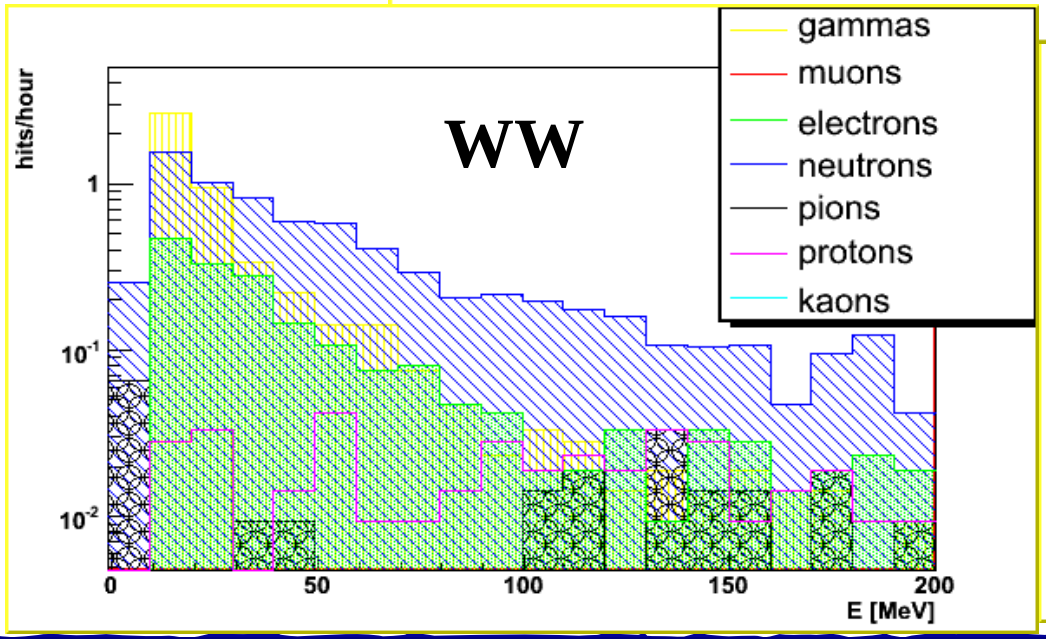
SEU: Energy Spectrum of Particles in FPGAs

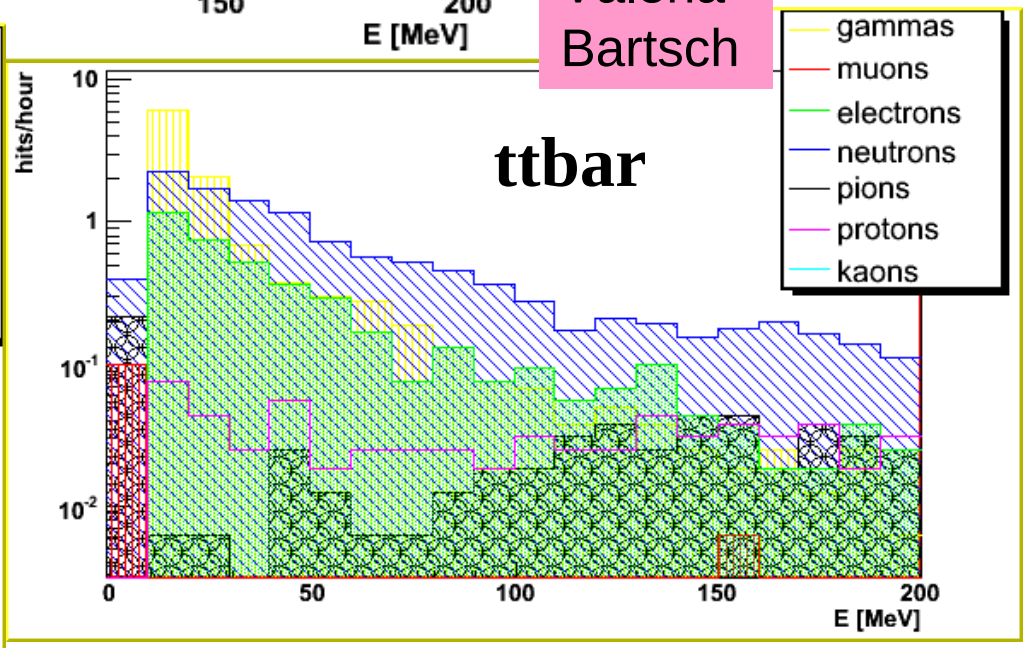
Y axis:

hits/hour



Valeria Bartsch





SEU: Weibull Fit

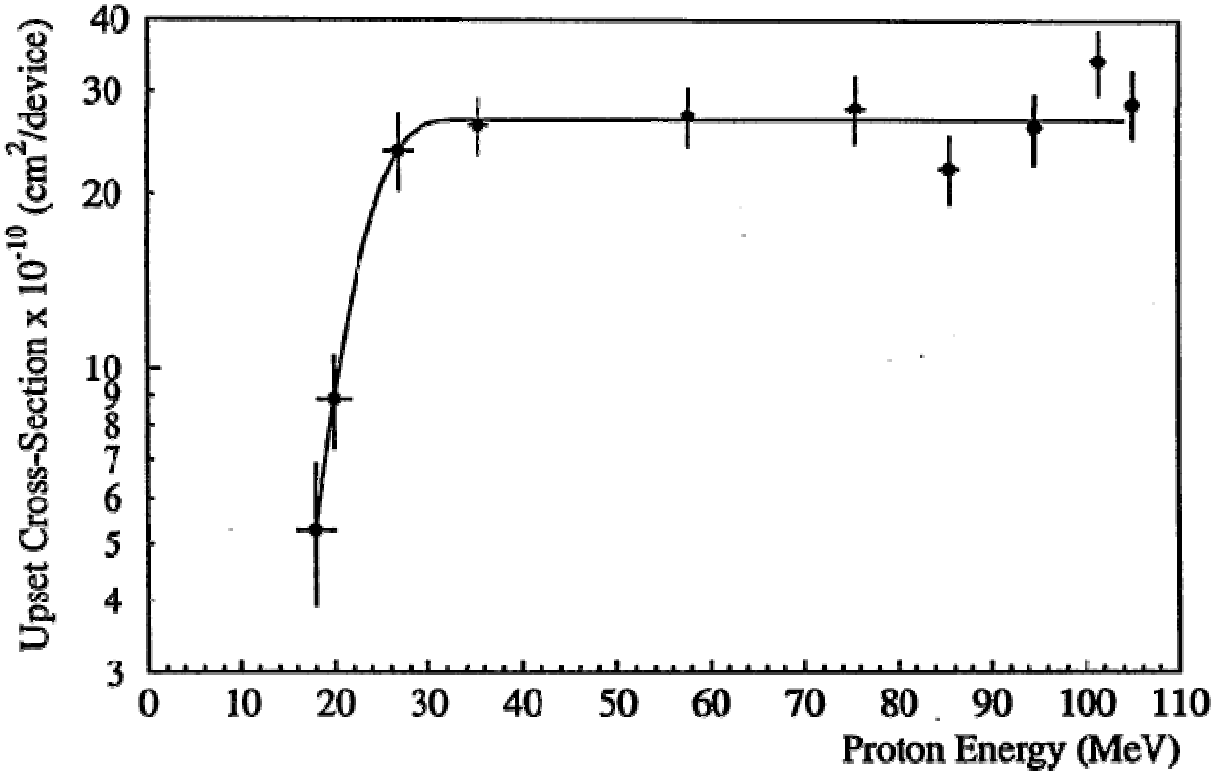


Fig. 4. Proton-induced SEU cross section for the switches and circuit in the Xilinx XC4036XLA FPGA. The curve is a fit to the data using a Weibull cumulative density function.

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Gingrich

⇒ above 20MeV neutrons start doing upsets

SEU: Rates expected with existing FPGAs

Virtex II X-2V100 Virtex II X-2V6000	0.018 SEUs/h
Altera Stratix	**0.220 SEUs/h**
Xilinx XC4036XLA	**0.005 SEUs/h**
Virtex XQVR300	0.044 SEUs/h
9804RP	0.018 SEUs/h

⇒in best case 1 SEU in 8 days for all FPGAs in the ECAL

Fin ...