Update on the Data Acquisition System development in the UK

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DAQ architecture

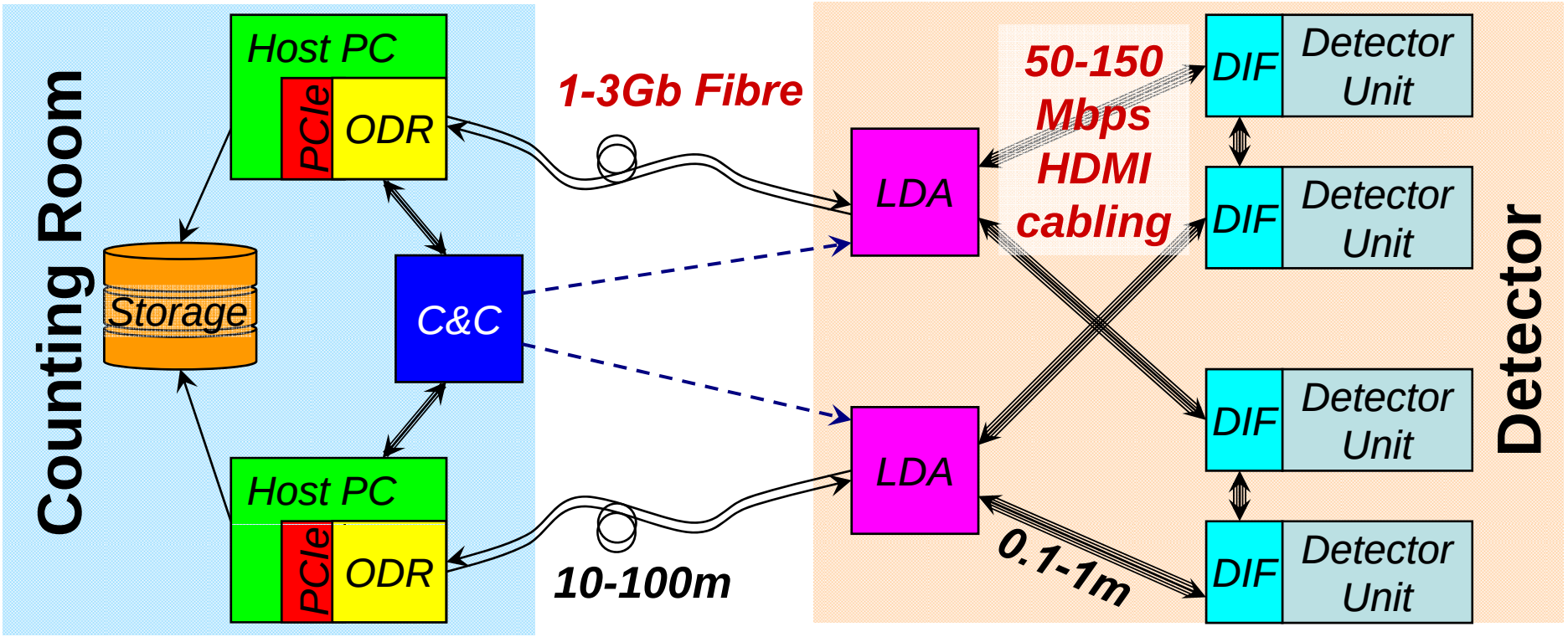
Detector Unit: Sensors & ASICs

DIF: Detector InterFace - connects generic DAQ and services

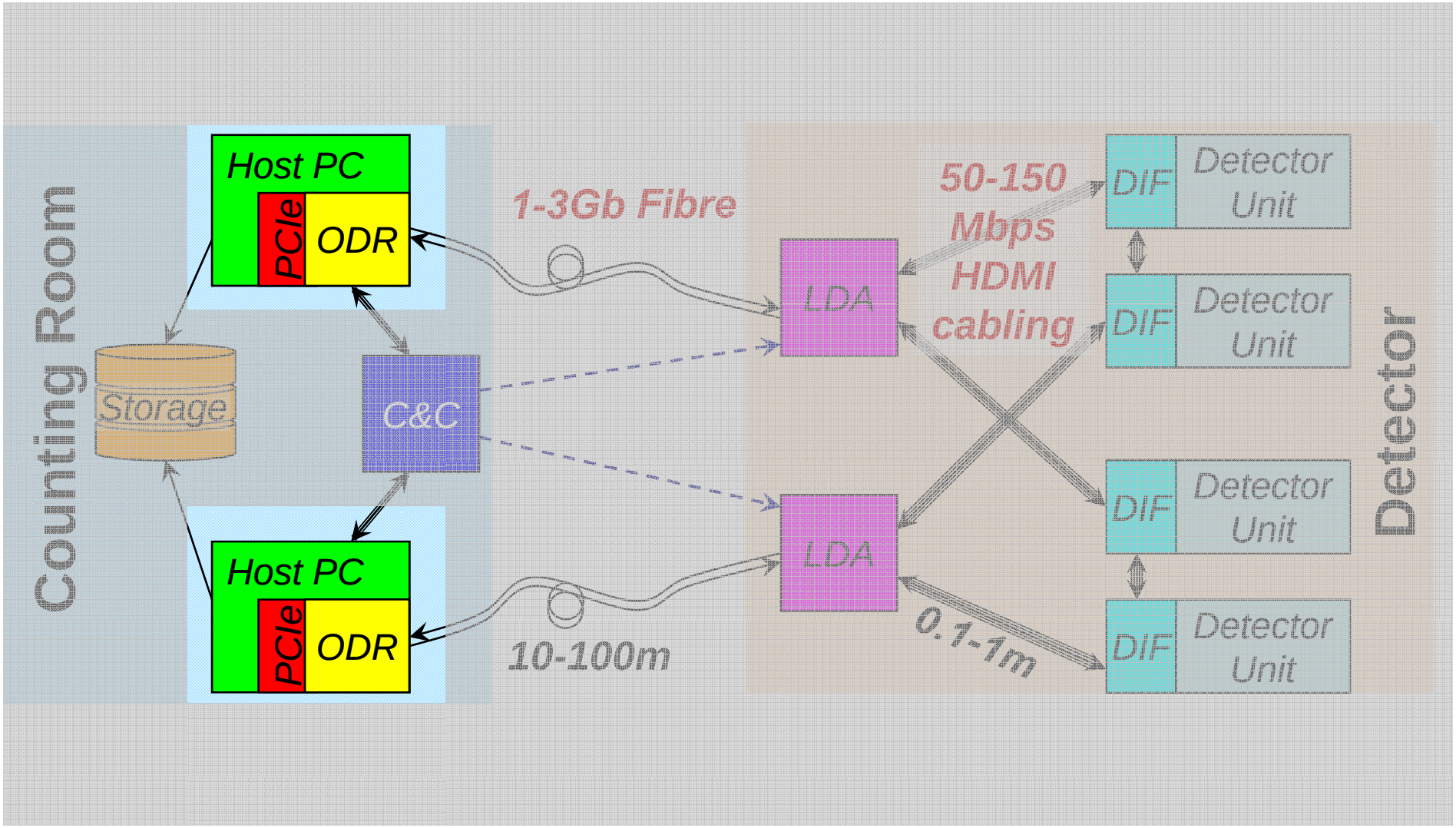
LDA: Link/Data Aggregator – fanout/in DIFs & drive link to ODR

ODR: Off Detector Receiver – PC interface for system.

C&C: Clock & Control: Fanout to ODRs (or LDAs)

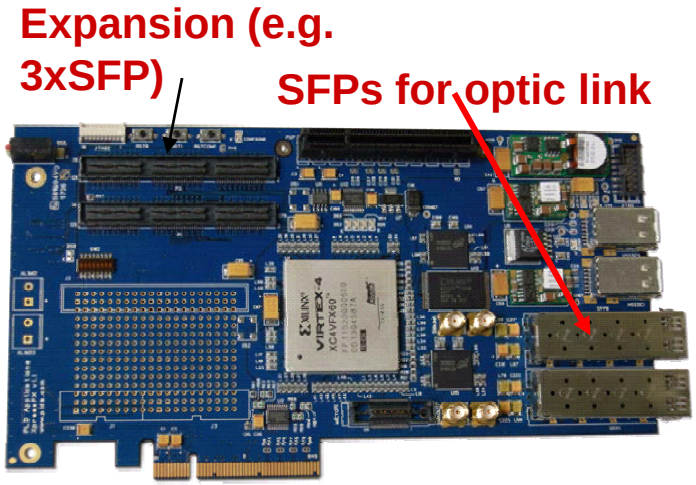


DAQ architecture



Off Detector Receiver (ODR)

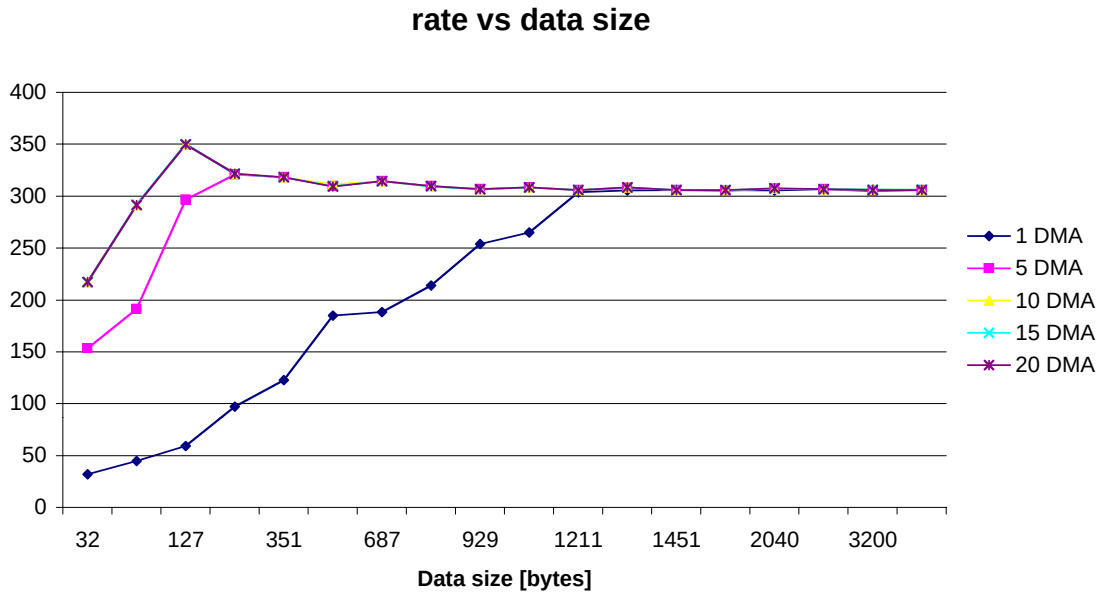
- Receives module data from LDA
  - PCI-Express card, hosted in PC.
  - 1-4 links/card (or more), 1-2 cards/PC
  - Buffers and transfers to store as fast as possible
- Sends controls and config to LDA for distribution to DIFs
- Performance studies & optimisation on-going

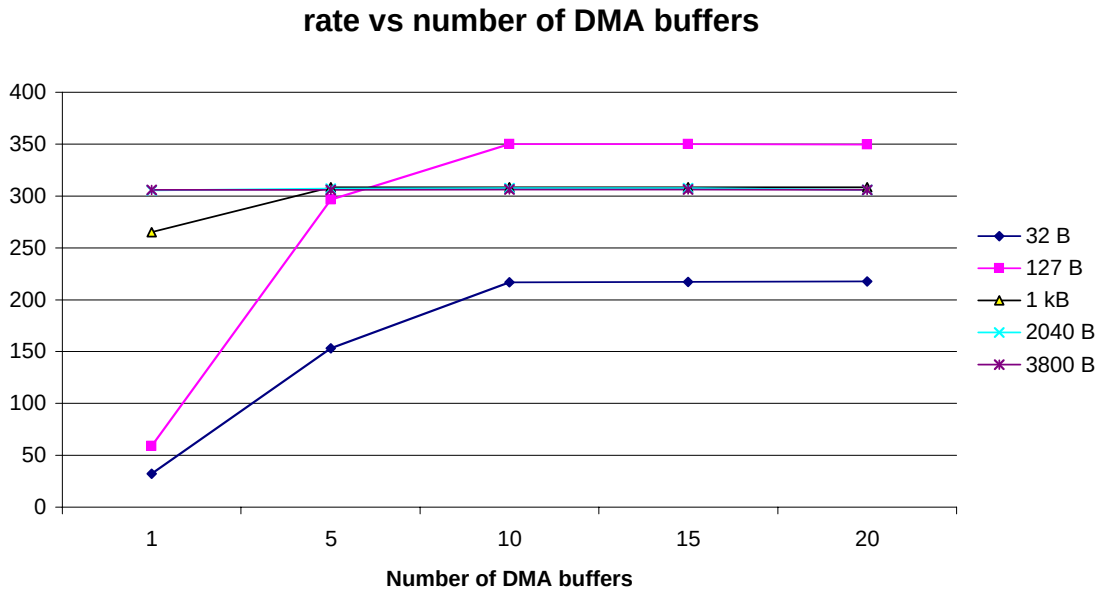


Hardware:

- Using commercial FPGA dev-board:
  - PLDA XPressFX100
  - Xilinx Virtex 4, 8xPCIe, 2x SFP (3 more with expansion board)

ODR - data access rate

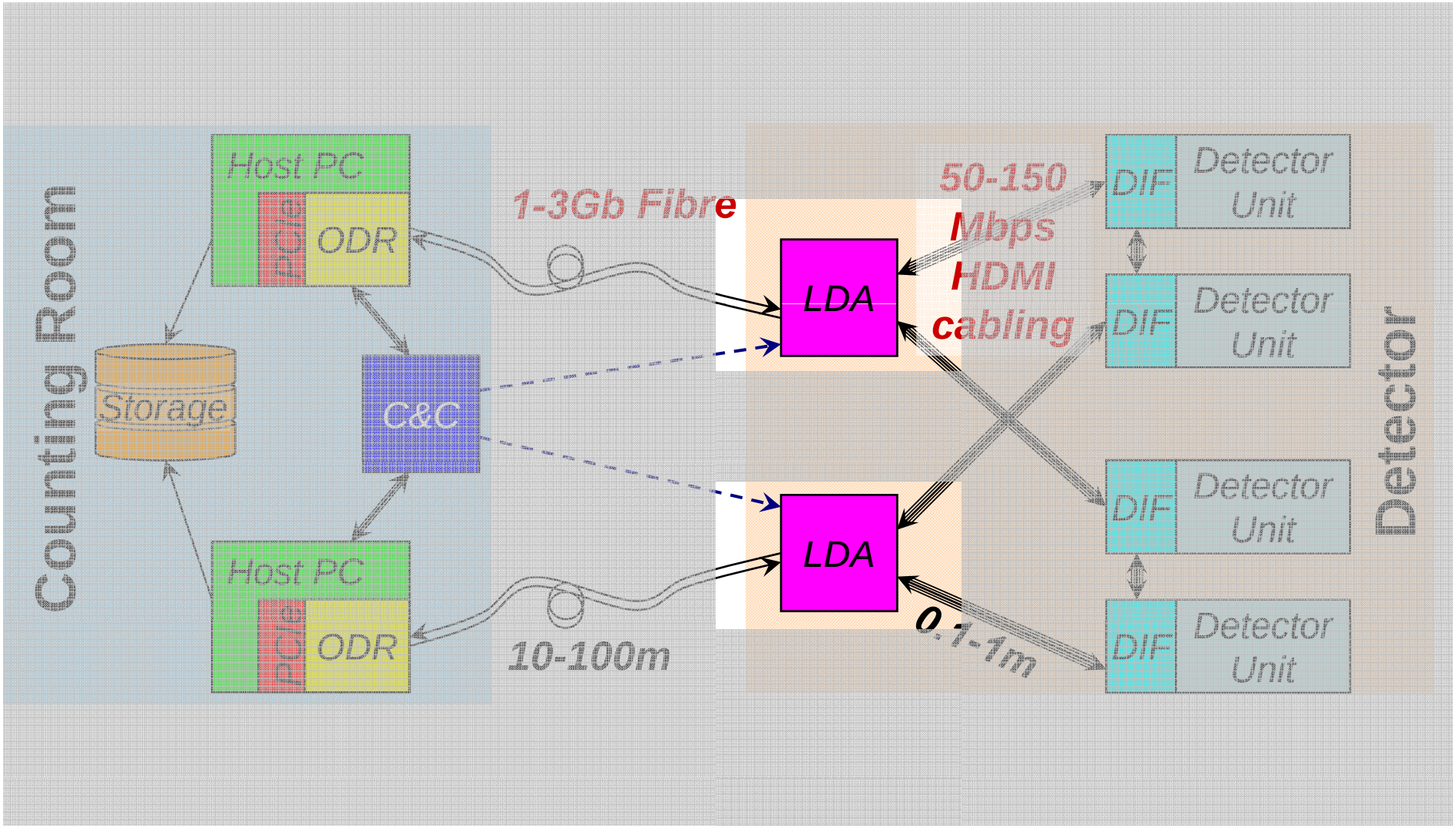




transfer of the data from ODR memory to the user-program memory

=> 220-320MByte/sec

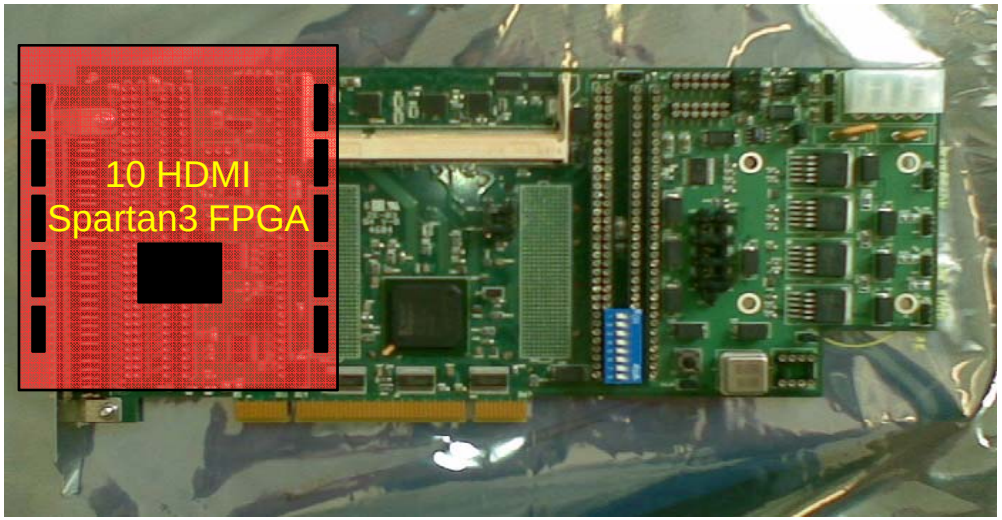
DAQ architecture

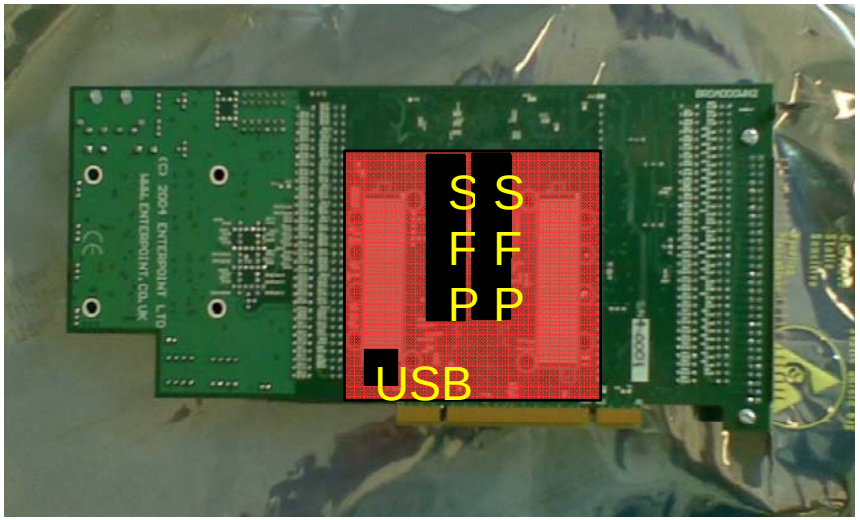


Link Data Aggregator (LDA)

Hardware:

- PCBs designed and get customized in 1week time by Enterpoint
- Carrier BD2 board likely to be constrained to at least a Spartan3 2000 model
- Gigabit links as shown below, 1 Ethernet and a TI TLK chipset
- USB used as a testbench interface when debugging





M.K., Manchester

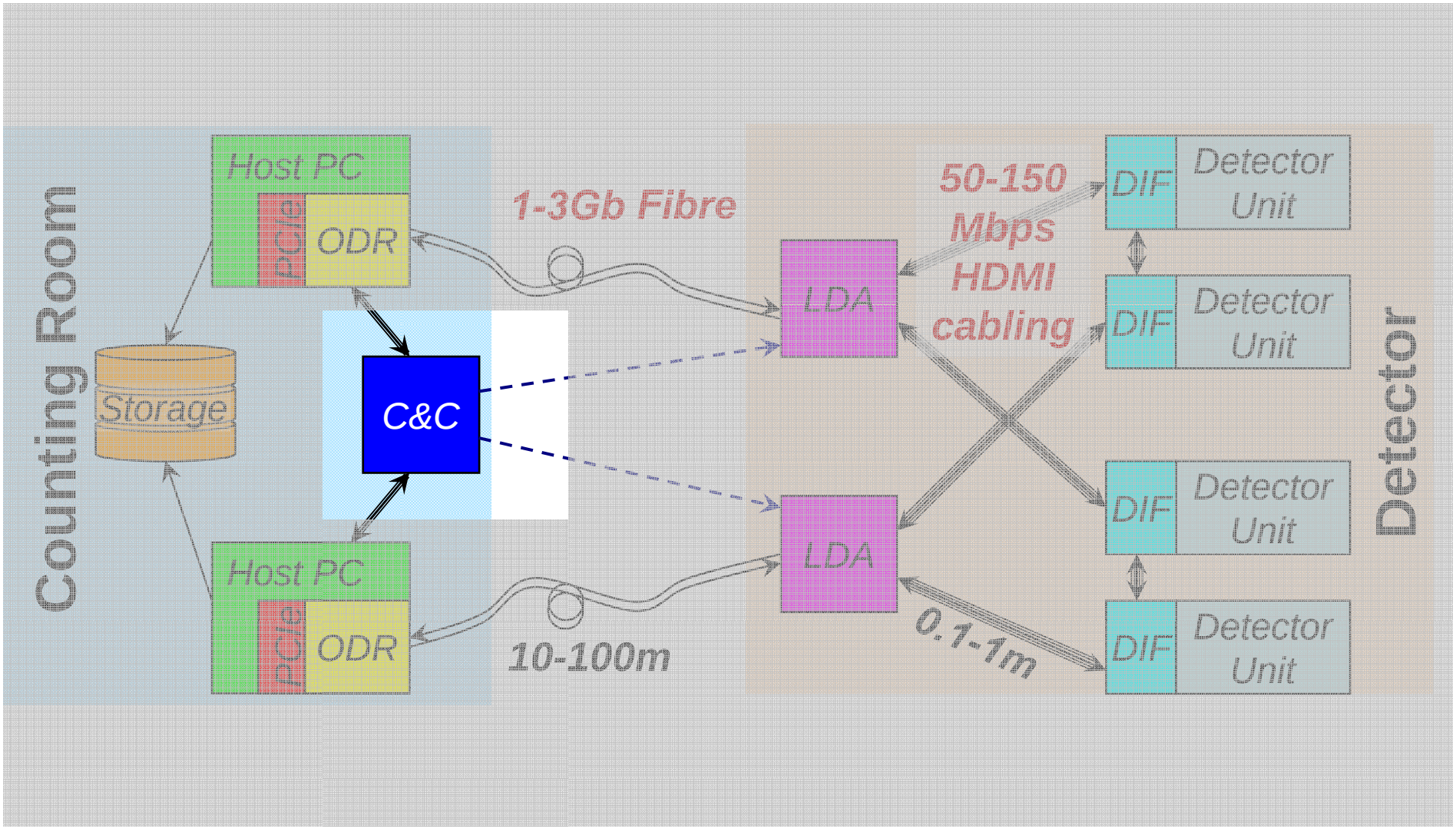
Link Data Aggregator (LDA)

Firmware:

- Ethernet interface based on Xilinx IP cores
- DIF interface based on custom SERDES with state machines for link control. Self contained, with a design for the DIF partner SERDES as well
- Possible to reuse parts from previous Virtex4 network tests
- No work done on TLK interface as of yet

1 LDA can serve 10 DIFS

DAQ architecture

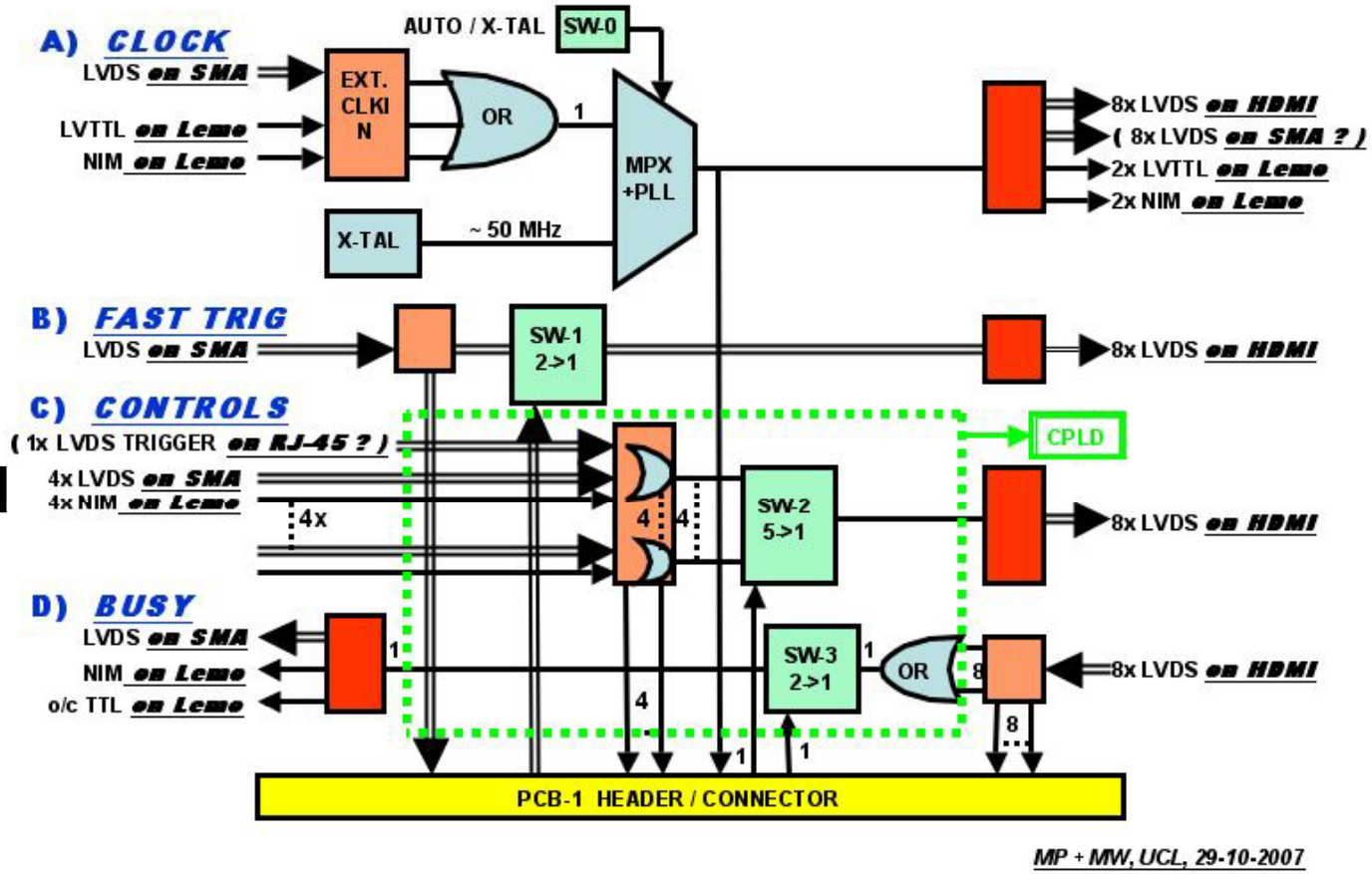


Clock and Control board

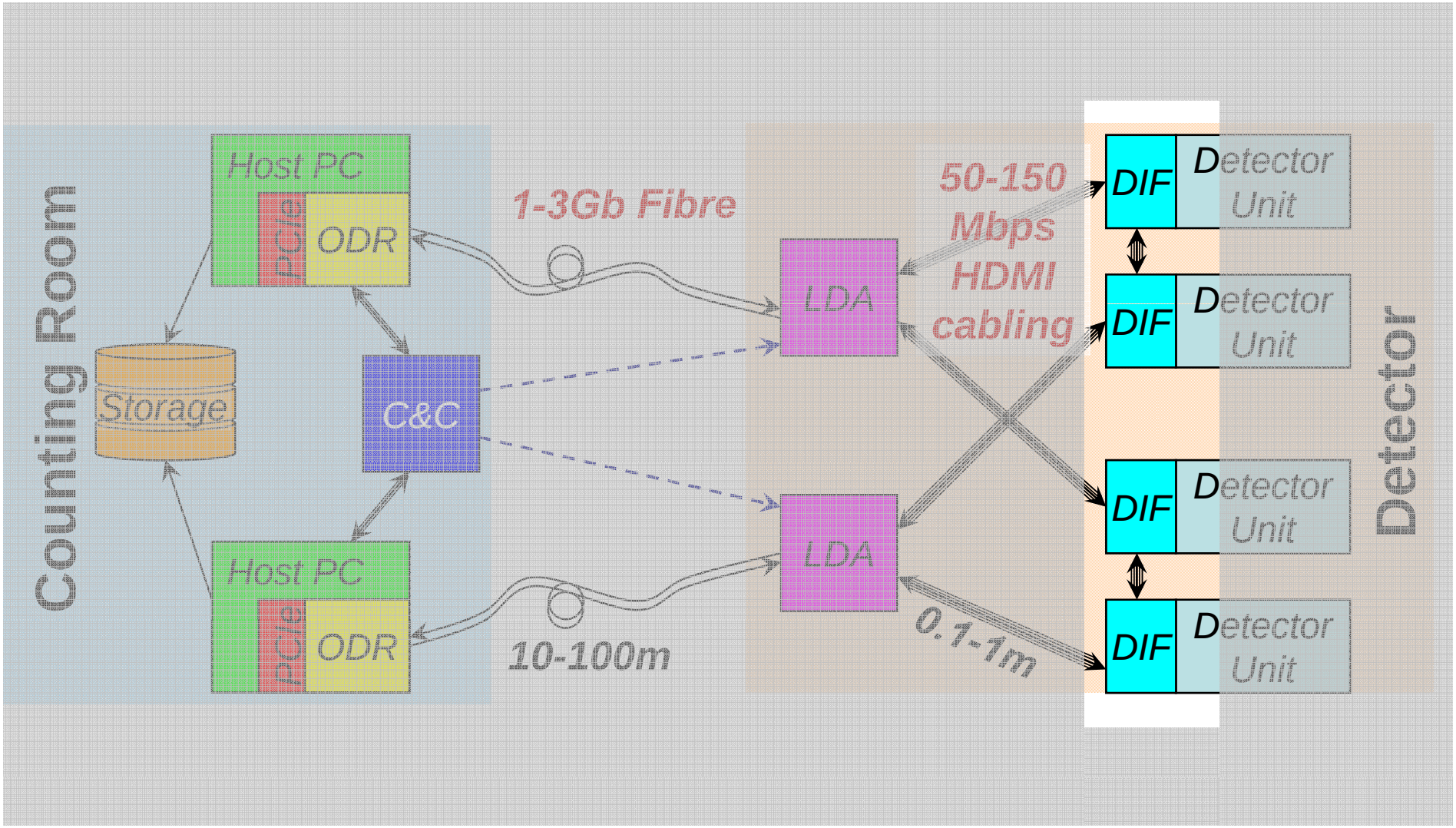
- provides an input line to an external clock and an internal clock for testing and debugging
- provides input lines for controls and fast trigger

board to be built at RAL

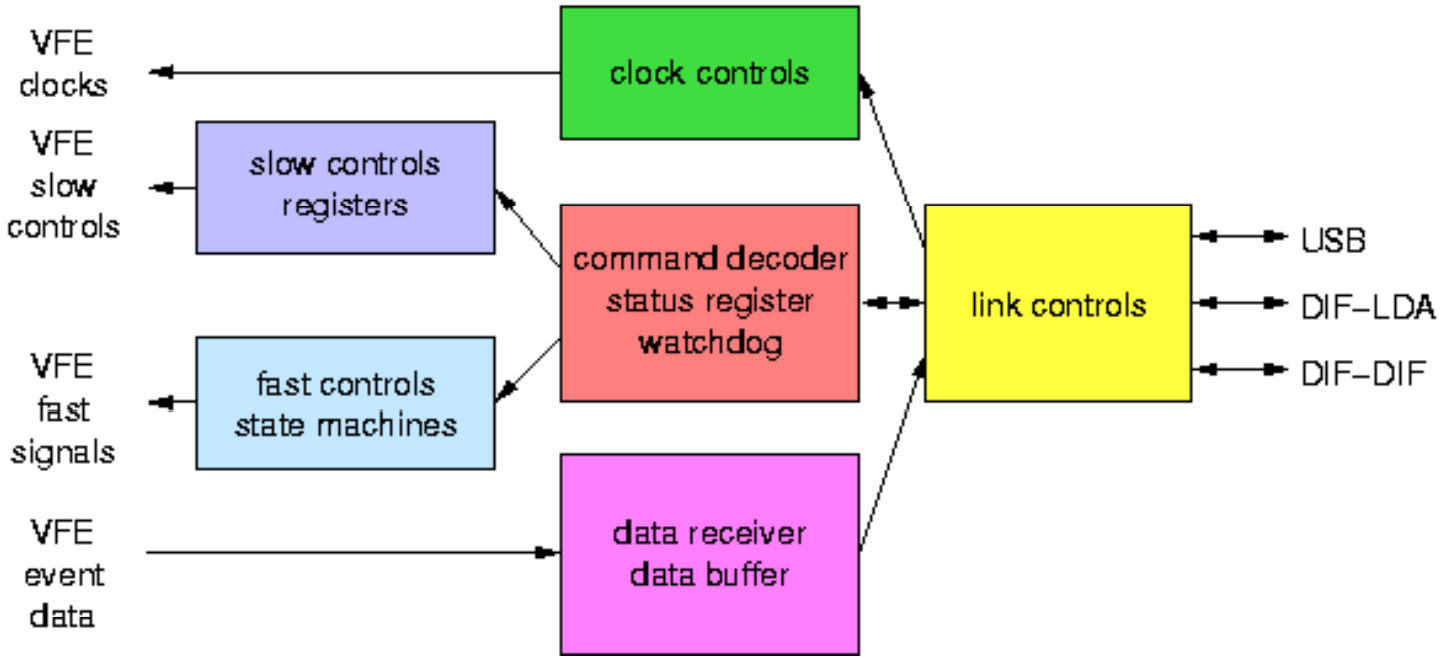
design finalised



DAQ architecture



Detector Interface (DIF) status

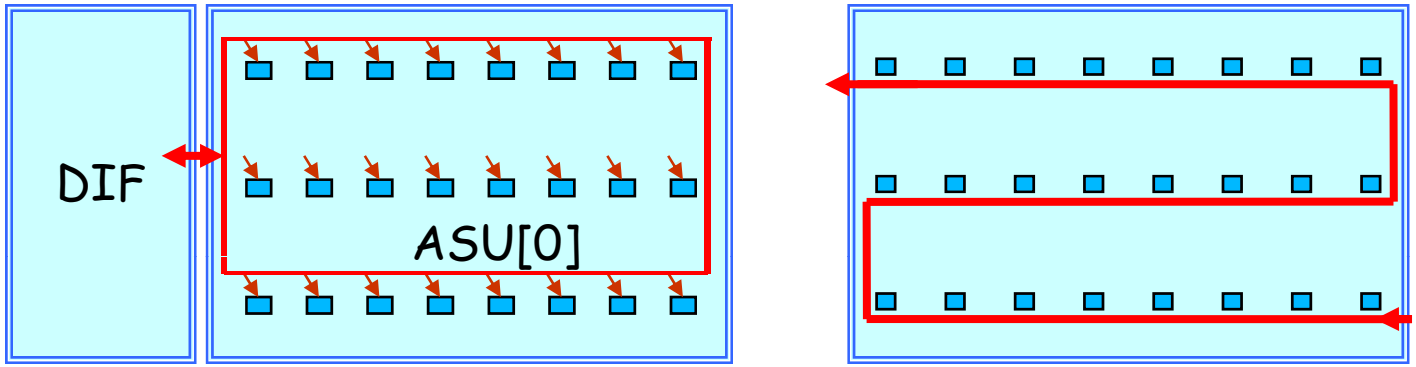


- keep DIF simple hence predictable (no local ‘memory management’, for example)
- DIF proto: large Xilinx FPGA, to be slimmed down for final DIF
- design ‘frozen’ (but not too cold), board layout well under way

M.G, B.H, Cambridge

ECAL slab interconnect

• geometry investigated (multi-rows preferred)



• technology: conductive adhesive vs. flat flexible cable (FFC), with preference to FFC

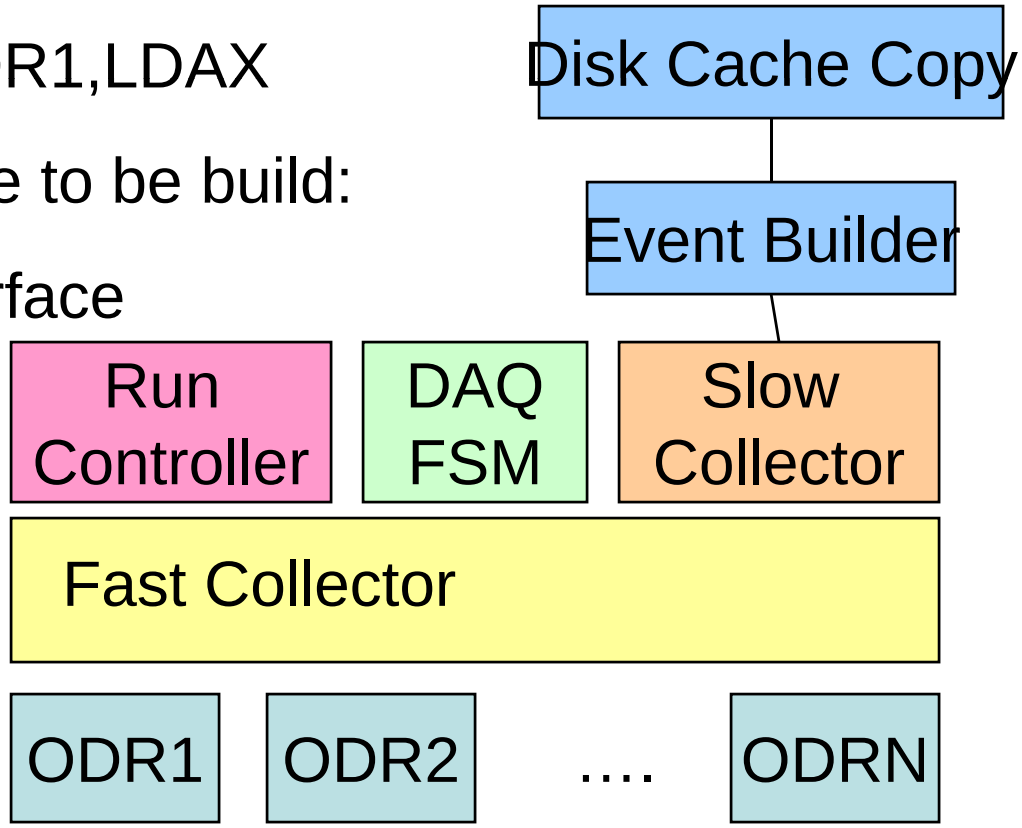
• soldering technologies are being investigated (Hot-Bar soldering, laser soldering, IR soldering)

DAQ software

- Chose DOOCS framework
- Ens naming service:

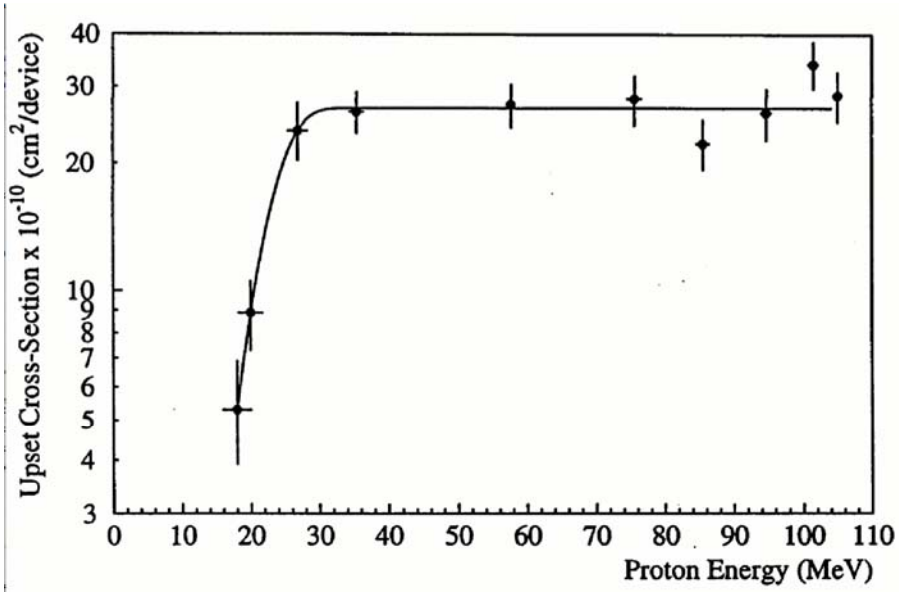
  Facility (F), device (D), location (L), property (P)

  e.g. CALICE,ODR,ODR1,LDAX
- Overview over infrastructure to be build:
  - starting point: ODR interface
  - event builder needs to be modified



Single Event Upset (SEU) Study

finalised, submitted to NIM



SEU cross section depending or

- FPGA type
- traversing particle (n,p,π)
- energy of traversing particle

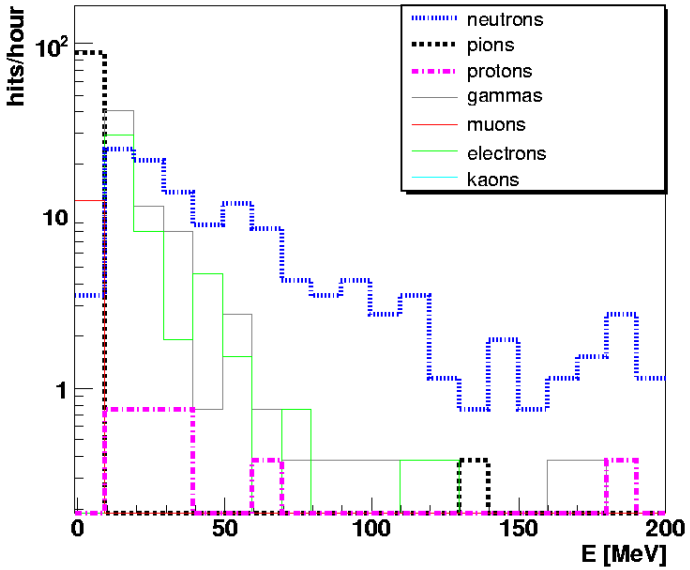
=> need to study particle spectra

V.B, M.W. UCL

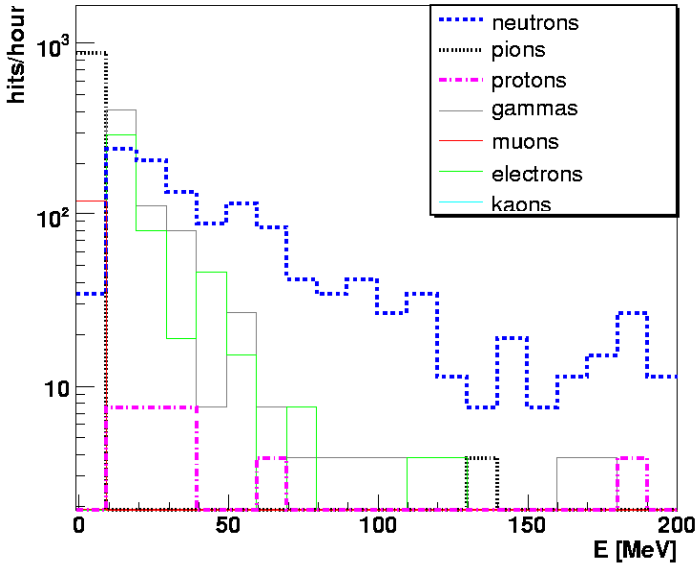
Single Event Upset (SEU) Study

Main backgrounds: (tt, WW and bhabha scattering also studied)

$\gamma\gamma$ (from beamstrahlung) -> hadrons



QCD events



$\Rightarrow$ SEU rate of 14 min-12hours depending on FPGA type for the whole ECAL, needs to be taken into account in control software

$\Rightarrow$ fluence of $2*10^6$/cm per year, not critical

$\Rightarrow$ radiation of 0.16Rad/year, not critical

$\Rightarrow$ occupancy of 0.003/bunch train (not including noise)

outlook

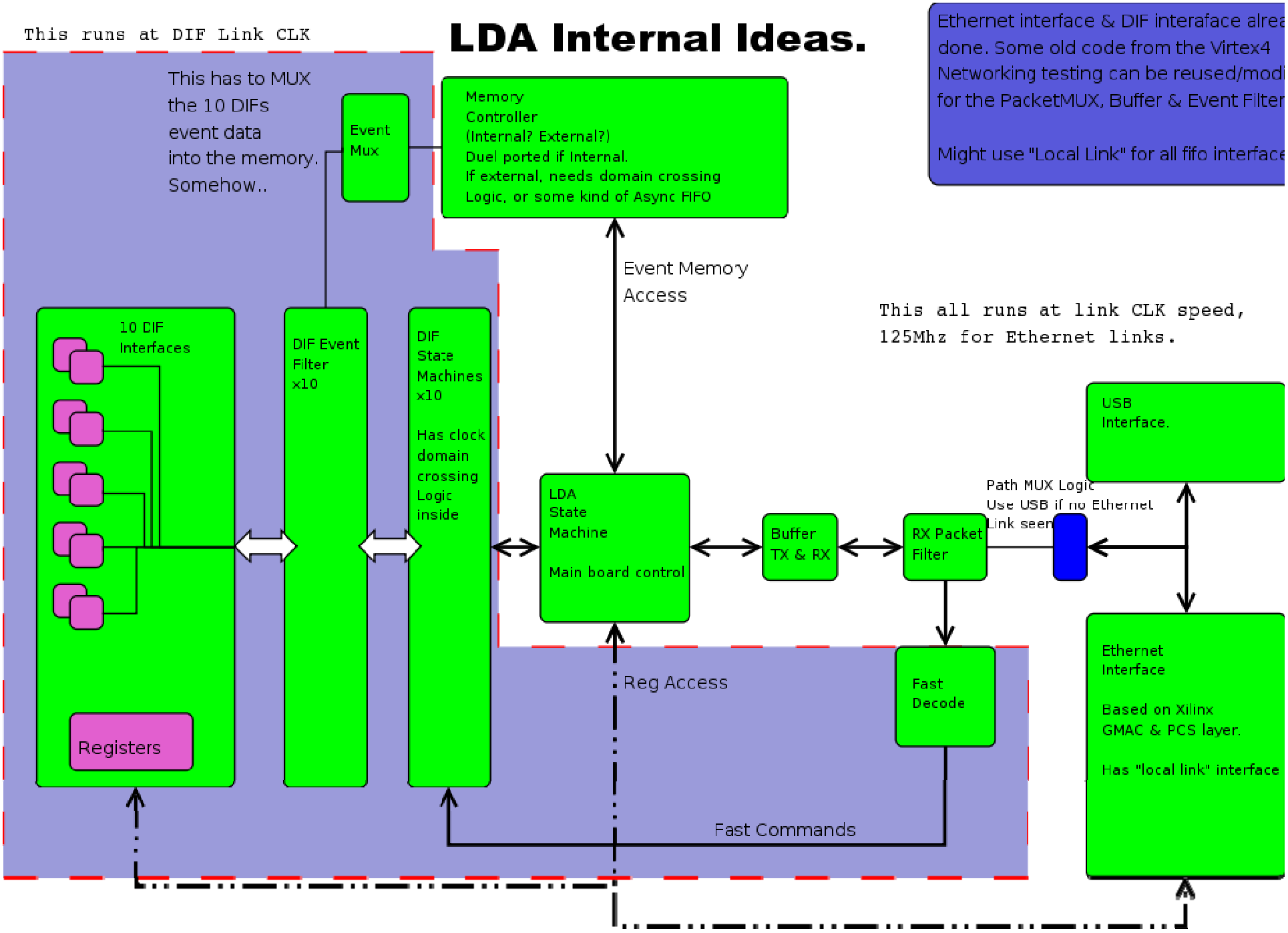
EUDET module:

- DAQtest 2008: ‘minimal DIF’ hardware & firmware
- EUDET beam test 2009

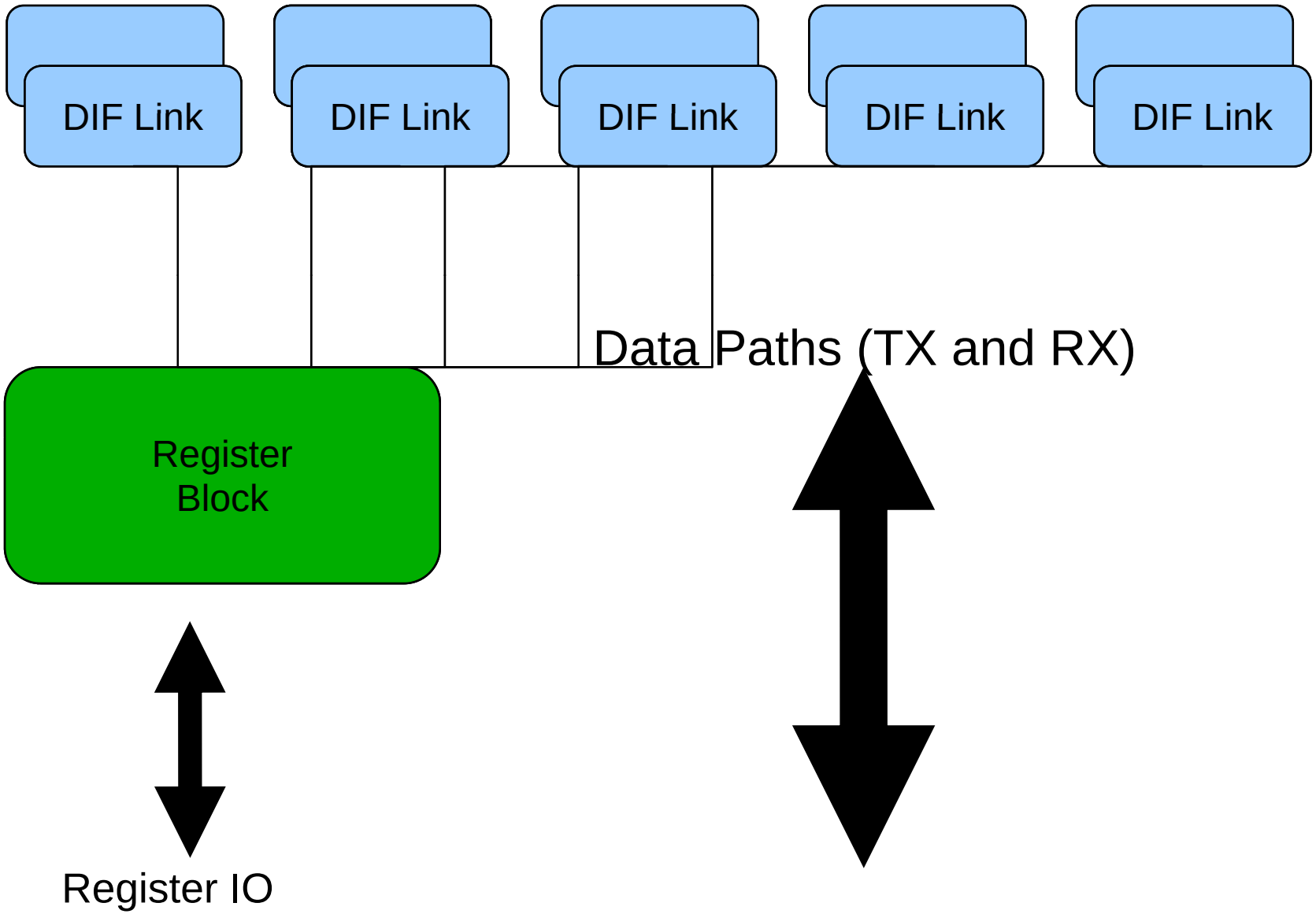
Question to the detector people:

- how many ODRs do we need?
- how many LDAs do we need?

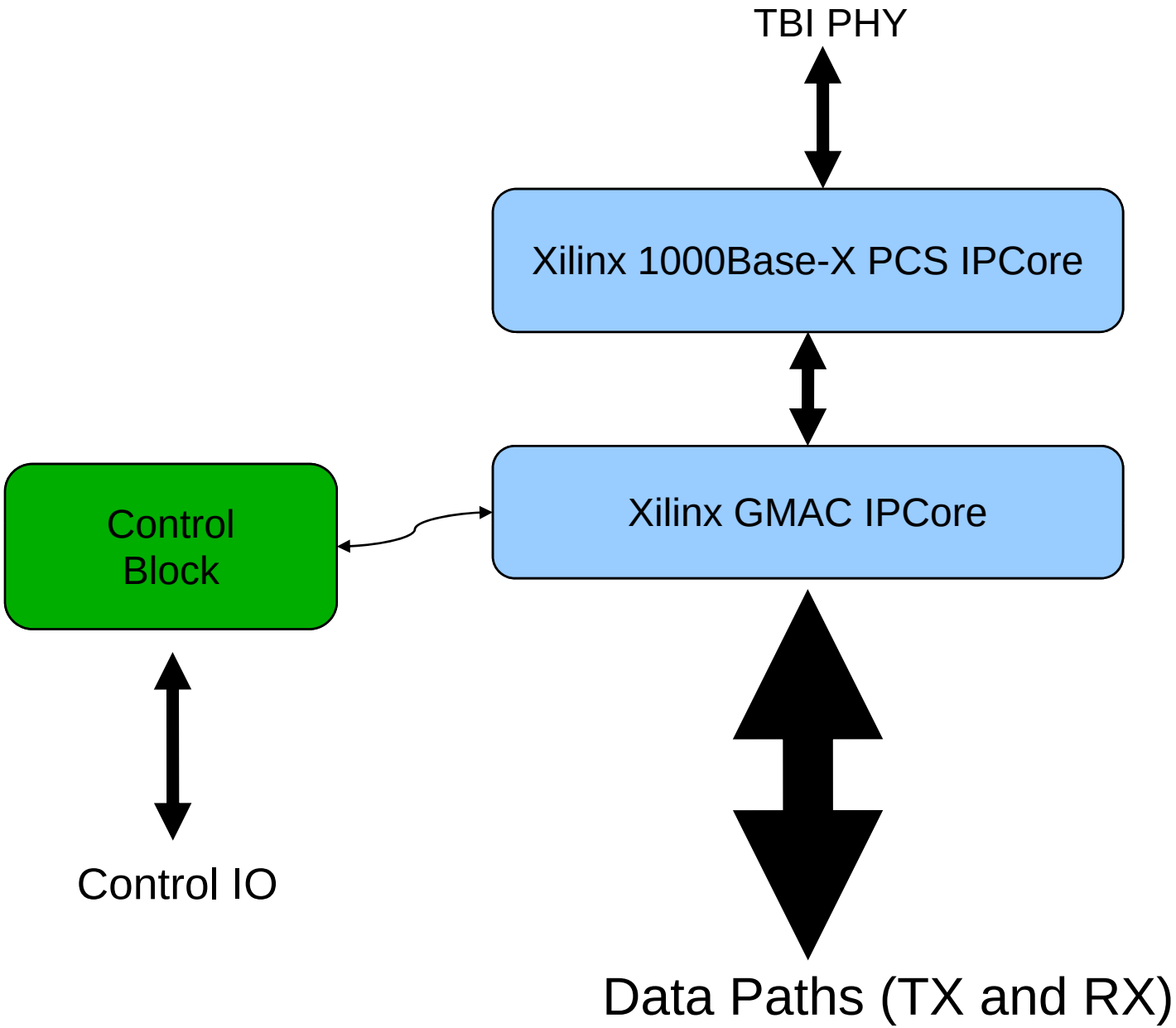
backup slides

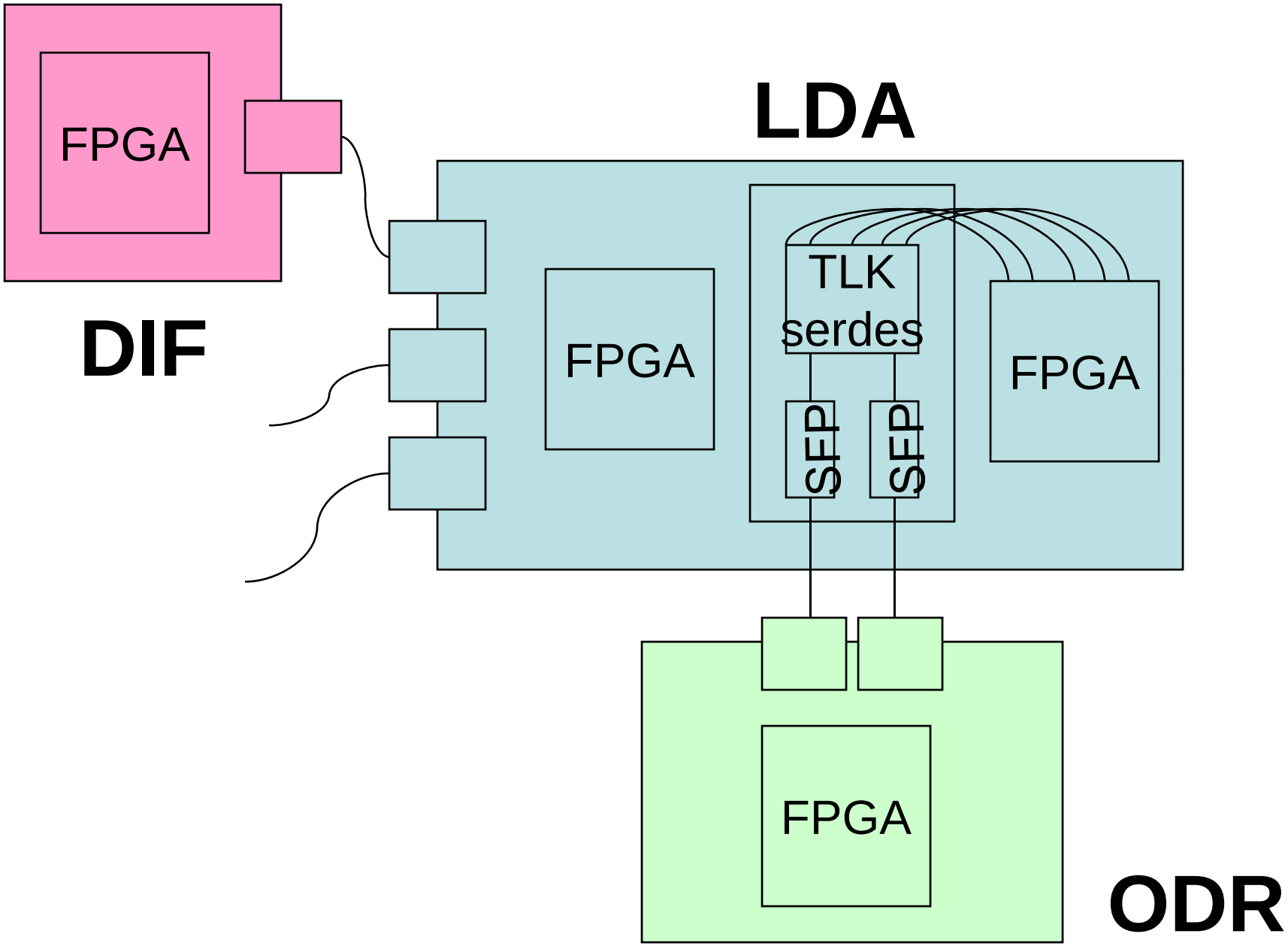

This runs at DIF Link CLK
LDA Internal Ideas.
Ethernet interface & DIF interaface alrea
done. Some old code from the Virtex4
Networking testing can be reused/modi
for the PacketMUX, Buffer & Event Filter
Might use "Local Link" for all fifo interface
This has to MUX
the 10 DIFs
event data
into the memory.
Somehow..
Event
Mux
Memory
Controller
(Internal? External?)
Duel ported if Internal.
If external, needs domain crossing
Logic, or some kind of Async FIFO
Event Memory
Access
This all runs at link CLK speed,
125Mhz for Ethernet links.
10 DIF
Interfaces
DIF Event
Filter
x10
DIF
State
Machines
x10
Has clock
domain
crossing
Logic
inside
LDA
State
Machine
Main board control
Buffer
TX & RX
RX Packet
Filter
Path MUX Logic
Use USB if no Ethernet
Link seen
USB
Interface.
Ethernet
Interface
Based on Xilinx
GMAC & PCS layer.
Has "local link" interface
Registers
Reg Access
Fast
Decode
Fast Commands

DIF Links Detail



Ethernet Link Detail




FPGA
DIF
LDA
FPGA
TLK
serdes
SFP
SFP
FPGA
FPGA
ODR