WP2.2 Slab Data Paths

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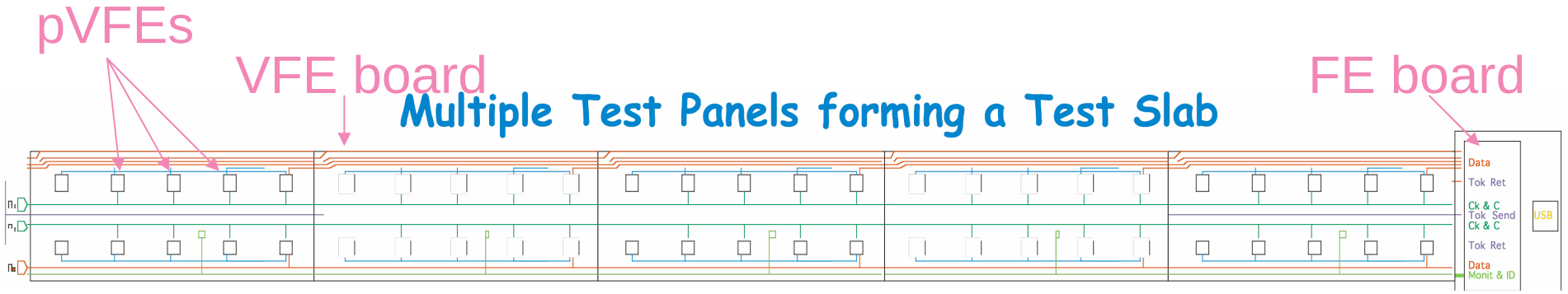
- Plan:
  - emulate multiple VFE chips on long PCBs
  - study the transmission behaviour (data, clock, controls..)
  - optimise VFE PCB for the required data rates

- Needs:
  - Segmented Test Slab PCBs
  - FPGAs emulating VFE chips: pVFEs
  - FE boards for distribution and reception of signals and services



VFE PCB progress:

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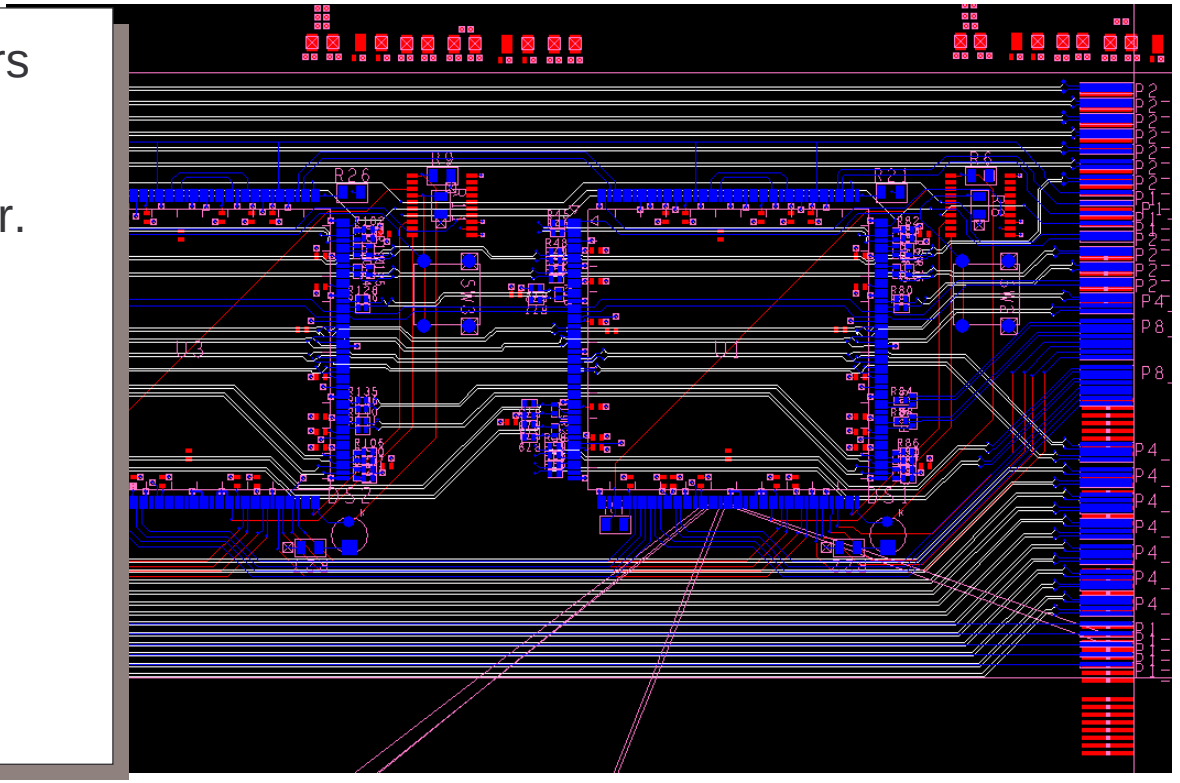
- Features thin (64mum) layers and narrow (75mum) traces
- Traces for various clock distr. schemes and/or readout architectures
- Rows of 4 FPGAs/board
- Every FPGA mimics 2 VFE chips



Ø Board schematics are ‘finished’
Ø PCB layout completed

FPGA Firmware for VFE emulation

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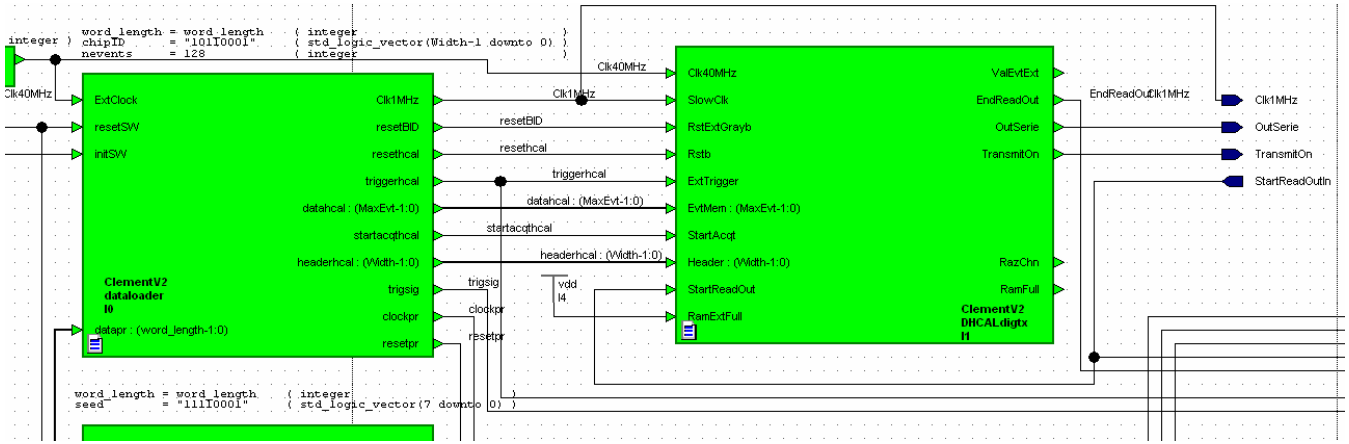
- ‘official’ VHDL code obtained from VFE chip designers at LAL (thanks!)
- VHDL code adapted for FPGA synthesis
- testbench for pVFE in VHDL



Evaluation board for tests

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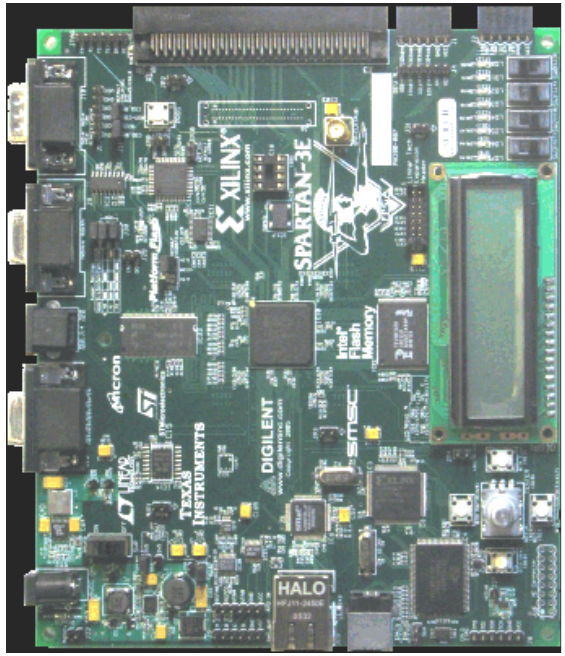
- Purchased Xilinx - Digilent evaluation board
- Spartan 3E FPGA suits our tests: many output standards and speeds supported
- Versatile test system: 32MB SRAM, RS232, USB, Ethernet 10/100, user connectors, etc.
- Excellent price/performance



pVFE simulation

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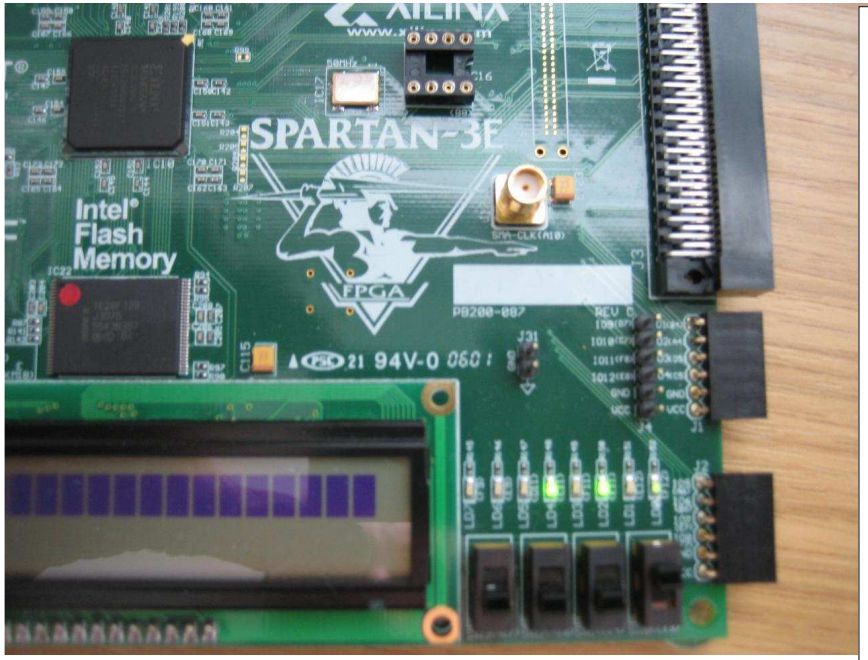

- Synthesized VFE VHDL code using Xilinx coregen RAM
- Two pVFEs+testbenches running on evaluation board (X3S500E device)
- Design fits into envisaged pVFE FPGA and yet leaves room for extras:
  - 25% of logic used
  - 83% of block RAM used.
- Preliminary code available for alternative pVFE implementation

High data rate alternative

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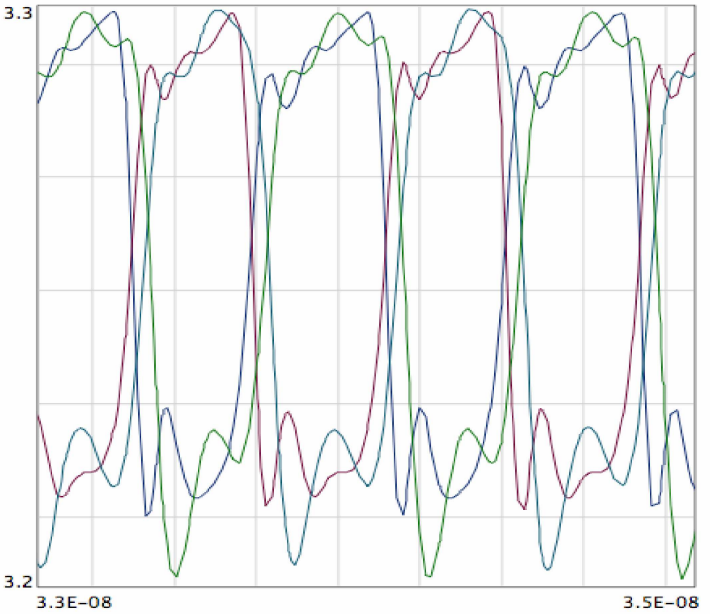
- Low output data rate relies on effective zero-suppression
- Assumed: low noise and low occupancy
- If assumptions prove wrong, much higher data rates are to be expected
- Investigate high-rate capability of slab data path



•ATLC/SPICE simulation of fast signals over PCB traces

•Spartan3E supports output rates of ~200MHz

pVFE firmware current status:

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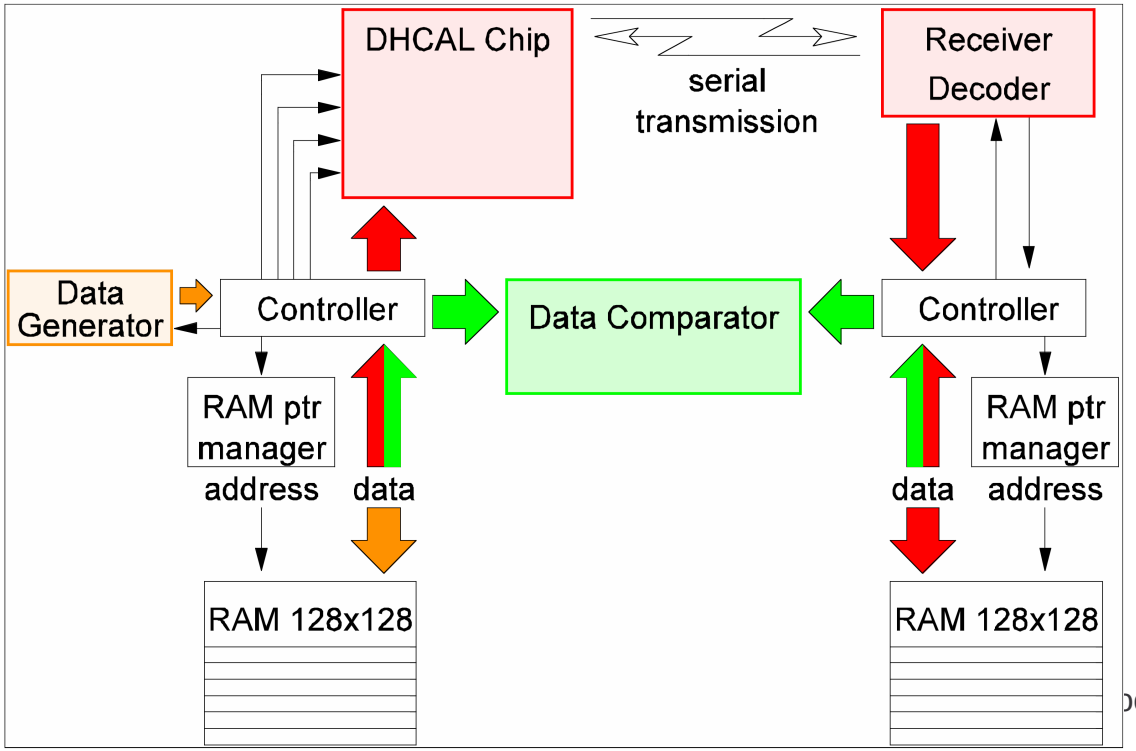
- ü Preliminary system in place,:
  - ü Data Generator
  - ü pVFE controller
  - ü Serial transmission (by DHCAL emulator)
  - ü Receiver



- q Next step:

  system capable of

  Bit Error Rate Testing:

  - q Data are stored in RAM
  - q Initial data are compared with data sent through serial transmission chain

Outlook and plans:

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- Manufacture VFE PCB panels (very) soon
- Define FE board requirements and interface
- Continue firmware development for pVFE and FE
- Think of interface with outside world…