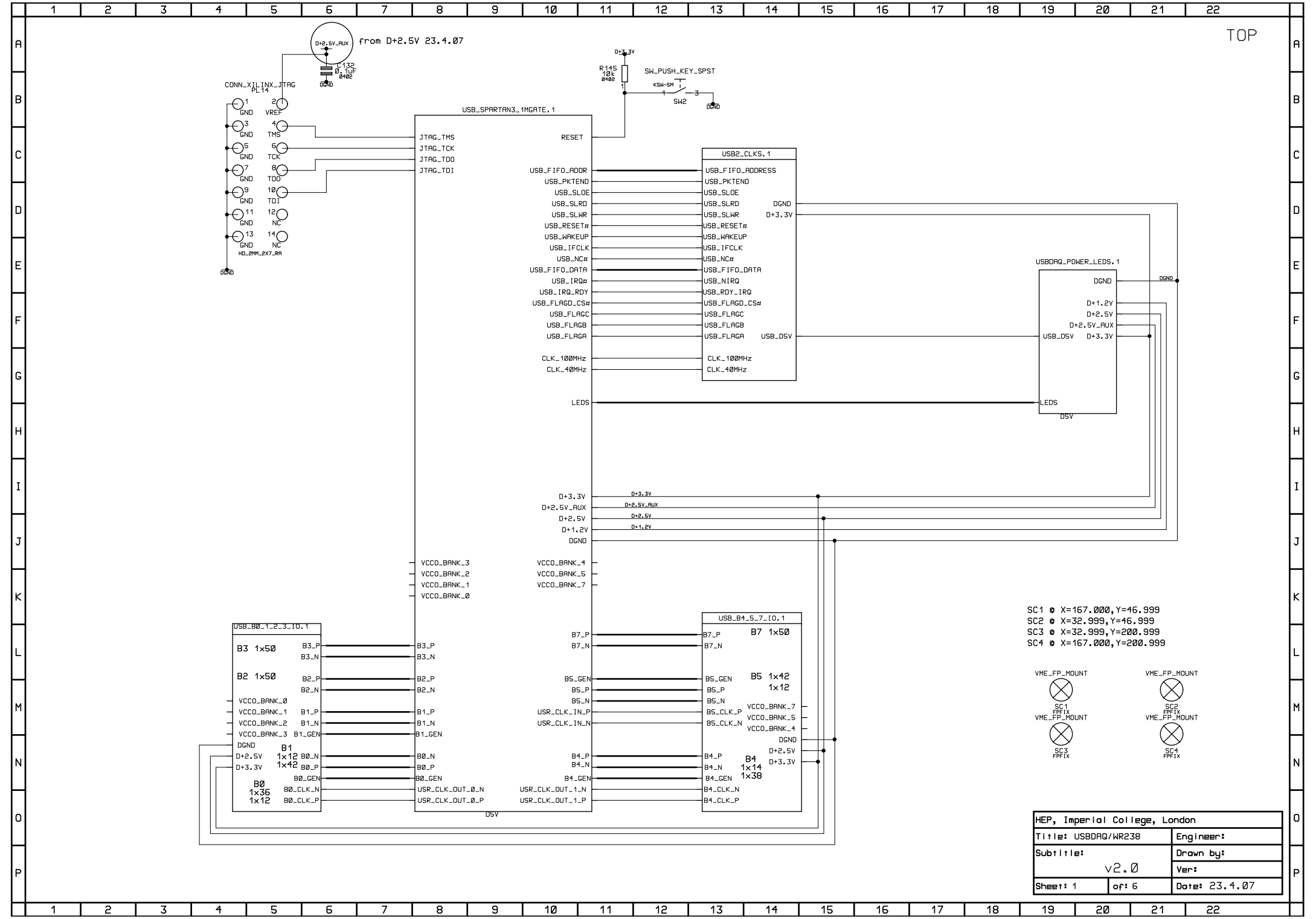
TOP
D+2.5V_AUX
from D+2.5V 23.4.07
C132
0.1UF
0402
DGND
CONN_XILINX_JTAG
PL14
HD_2MM_2X7_RA
GND
VREF
TMS
TCK
TDO
TDI
NC
D+3.3V
R145
10k
0402
SW_PUSH_KEY_SPST
KSH-SM
SW2
USB_SPARTAN3_1MGATE.1
JTAG_TMS
JTAG_TCK
JTAG_TDO
JTAG_TDI
RESET
USB_FIFO_ADDR
USB_PKTEND
USB_SLOE
USB_SLRD
USB_SLWR
USB_RESET#
USB_WAKEUP
USB_IFCLK
USB_NC#
USB_FIFO_DATA
USB_IRQ#
USB_IRQ_RDY
USB_FLAGD_CS#
USB_FLAGC
USB_FLAGB
USB_FLAGA
CLK_100MHz
CLK_40MHz
LEDS
USB2_CLKS.1
USB_FIFO_ADDRESS
USB_NIRQ
USB_RDY_IRQ
USB_D5V
USBDAQ_POWER_LEDS.1
D+1.2V
D+2.5V
D+2.5V_AUX
VCCO_BANK_3
VCCO_BANK_2
VCCO_BANK_1
VCCO_BANK_0
VCCO_BANK_4
VCCO_BANK_5
VCCO_BANK_7
USB_B0_1_2_3_IO.1
B3 1x50
B2 1x50
B1
1x12
1x42
B0
1x36
1x12
B3_P
B3_N
B2_P
B2_N
B1_P
B1_N
B1_GEN
B0_N
B0_P
B0_GEN
B0_CLK_N
B0_CLK_P
USR_CLK_OUT_0_N
USR_CLK_OUT_0_P
USB_B4_5_7_IO.1
B7 1x50
B5 1x42
1x12
B4
1x14
1x38
B7_P
B7_N
B5_GEN
B5_P
B5_N
B5_CLK_P
B5_CLK_N
USR_CLK_IN_P
USR_CLK_IN_N
B4_P
B4_N
B4_GEN
B4_CLK_N
B4_CLK_P
USR_CLK_OUT_1_N
USR_CLK_OUT_1_P
D5V
SC1 @ X=167.000,Y=46.999
SC2 @ X=32.999,Y=46.999
SC3 @ X=32.999,Y=200.999
SC4 @ X=167.000,Y=200.999
VME_FP_MOUNT
FPFIX
SC1
SC2
SC3
SC4
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Engineer:
Subtitle:
v2.0
Drawn by:
Ver:
Sheet: 1
of: 6
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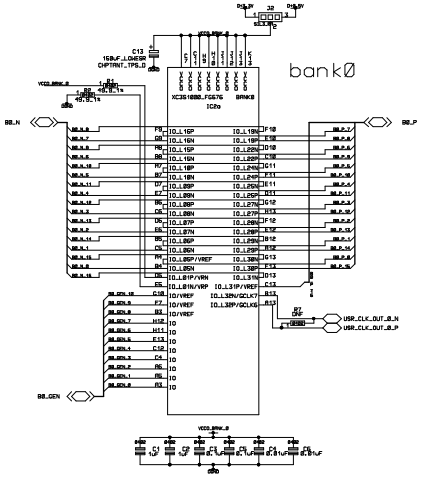
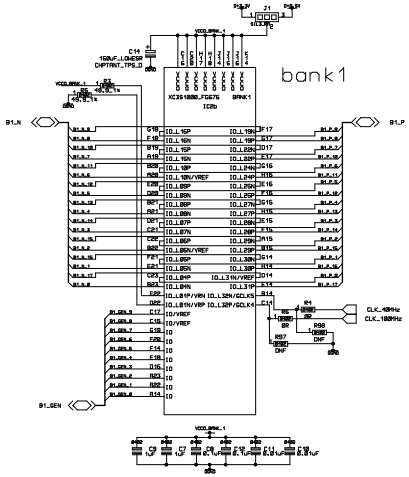
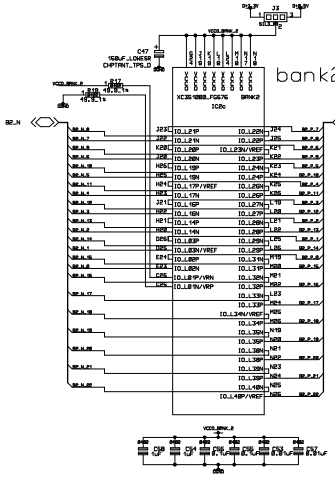
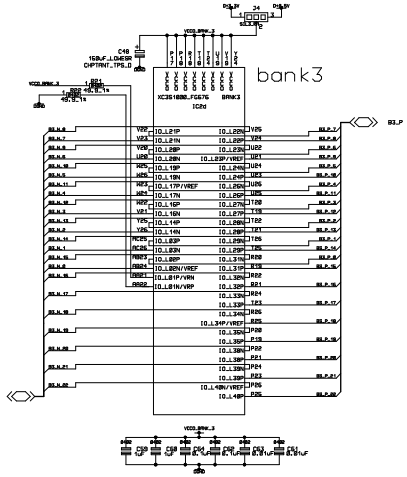
SYSTEM_FPGA

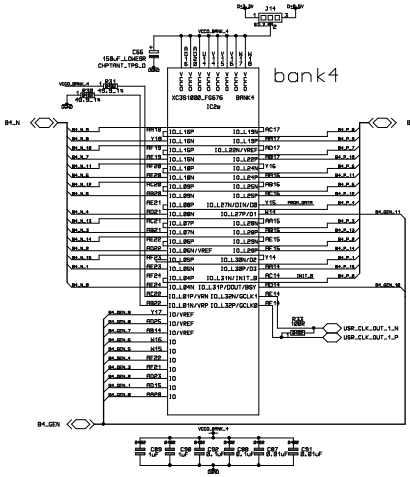
SPARTAN3_1MGATE

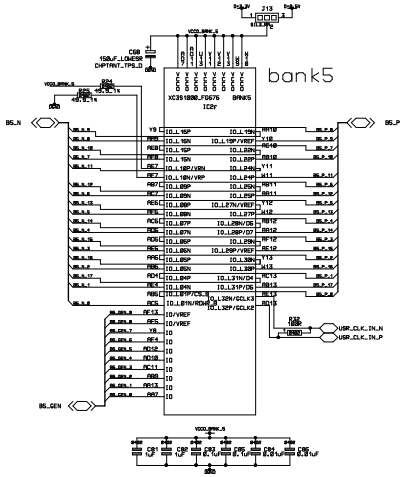


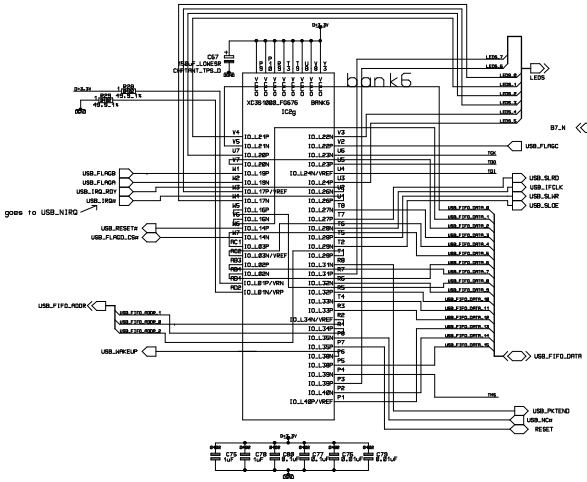


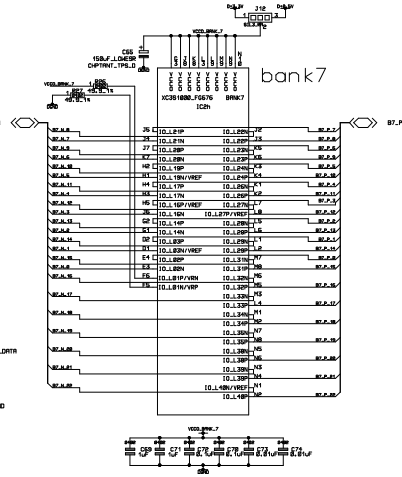




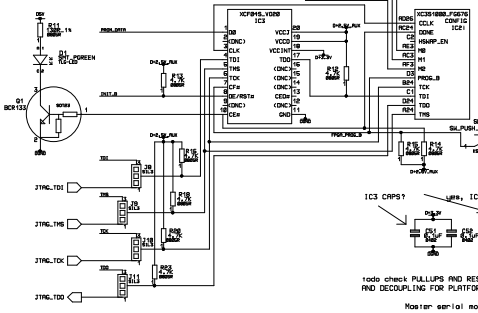


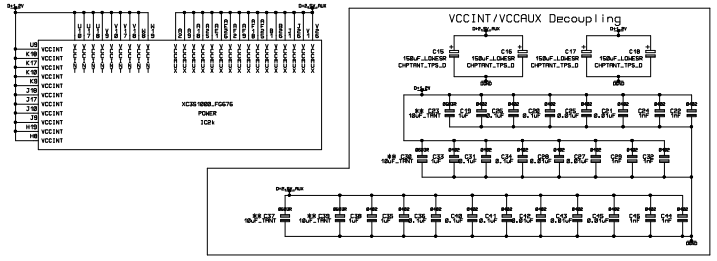






I've changed the power of the configuration circuit to D+2.5_AUX. Matt, 29.01.07



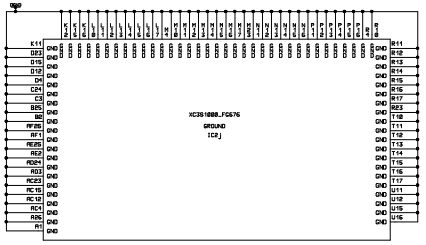


** Value reset on these caps, rather than generate new symbol 21.4.07

IC3 CAPS? Yes, IC3, please. Matt, 29.01.07

todo check PULLUPS AND RESISTORS AND DECOUPLING FOR PLATFORM FLASH

Master serial mode =0,0,0



DGND
D+1.2V
D+2.5V
D+2.5V_AUX
D+3.3V
DSV

VCCO_BANK_0
VCCO_BANK_1
VCCO_BANK_2
VCCO_BANK_3
VCCO_BANK_4
VCCO_BANK_5
VCCO_BANK_7

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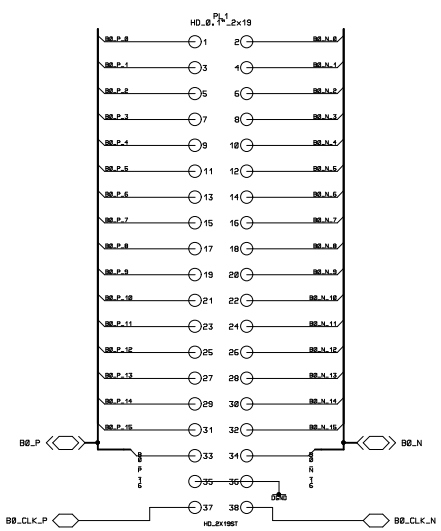
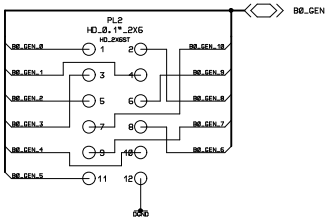
Title: USB2ORQ/HR230	Engineer:	
Subtitle: v2.0	Drawn by: Yan!	
Sheet 1 of 16	Date: 23.4.07	

BANK_0_1_2_3

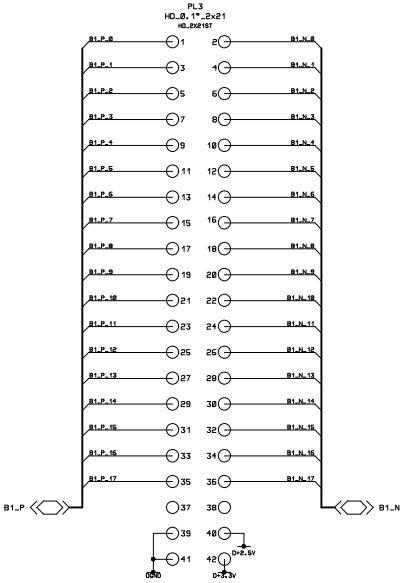
change symbol sometime...still thinks its 48way

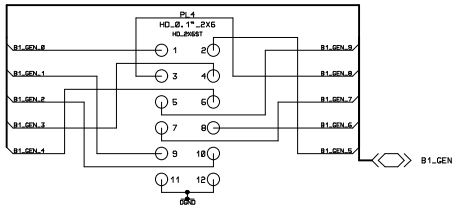
BANK 0



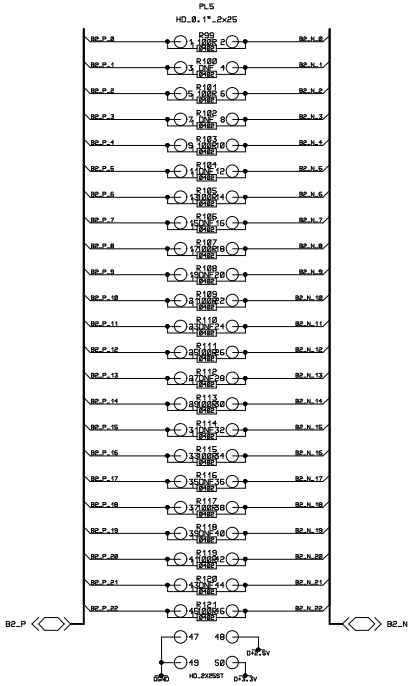


BANK 1

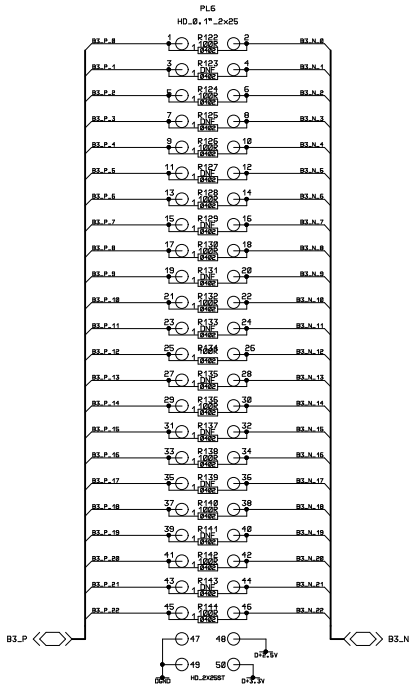




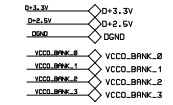
BANK 2



BANK 3



RESISTORS PLACE NEAR FPGA WITHIN 2CM MAX
CLEARER/EASIER TO PLACE ON THIS SHEET THAN ON FPGA BLOCK



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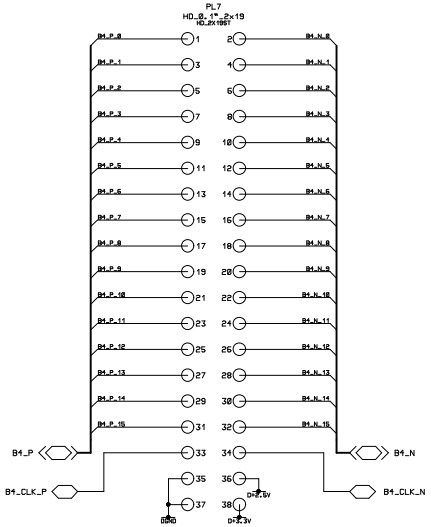
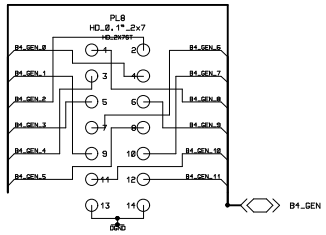
Title: USBDAQ/WR2338		Engineer:
Subtitle: v2.0		Drawn by:
		Ver:
Sheet: 5	of: 6	Date: 23.4.07

BANK_4_5_7

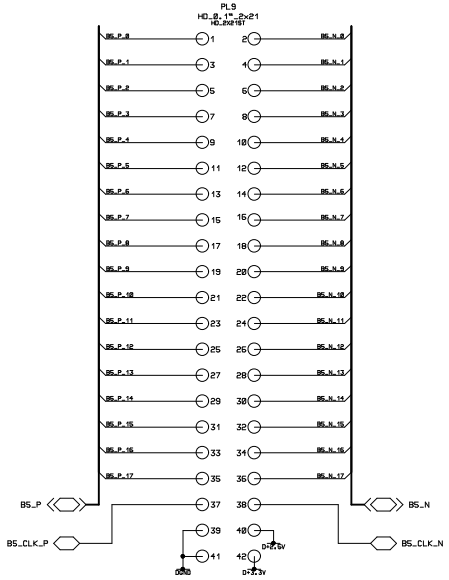
change symbol sometime...still thinks its 48way

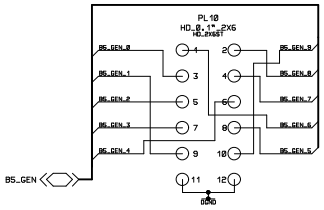
BANK 4



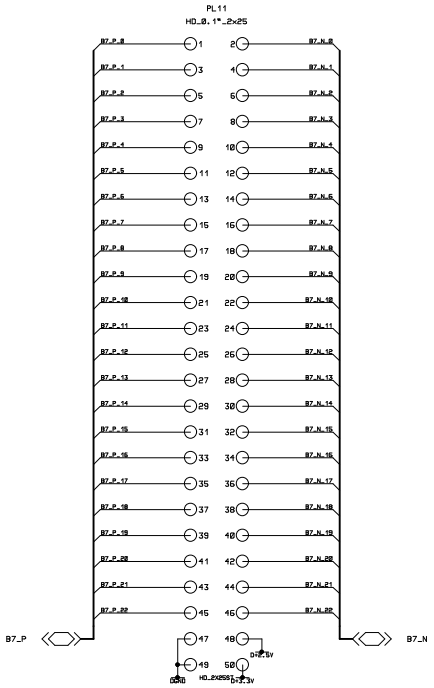


BANK 5





BANK 7



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Title: USBDAQ/WR238		Engineer:
Subtitle: v2.0		Drawn by:
		Ver:
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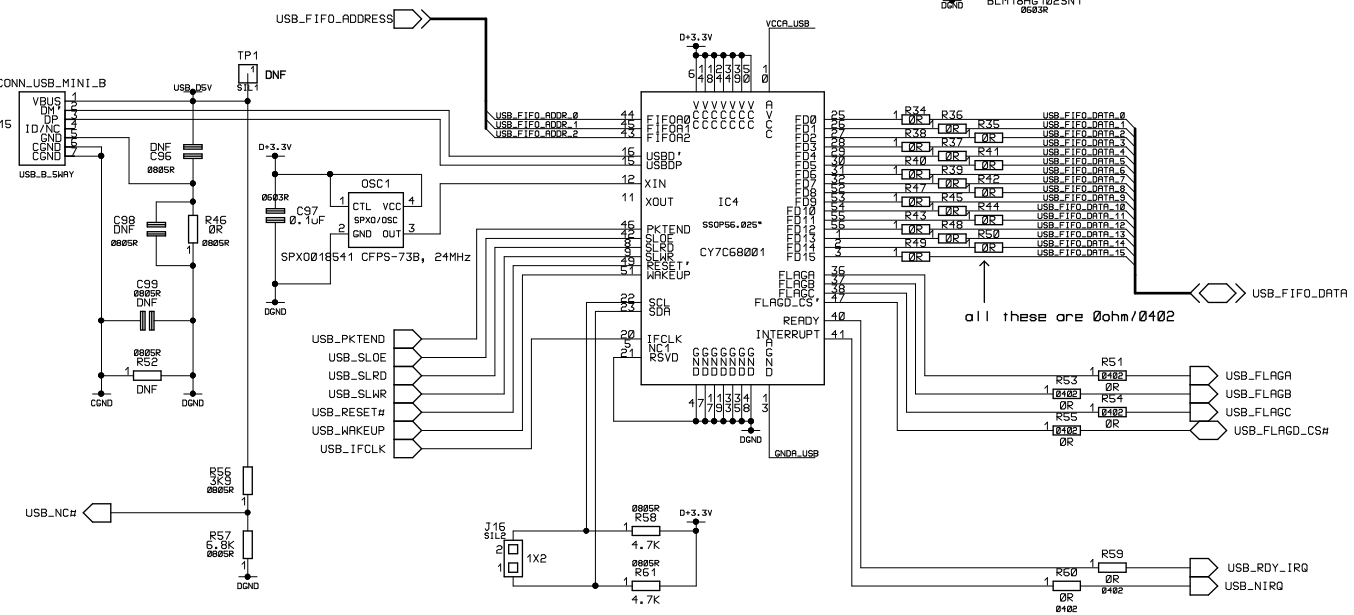
USB 2.0

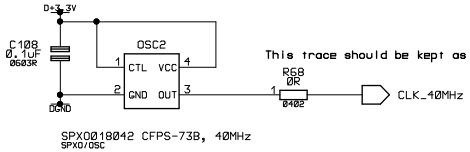
[IDAQ USB X = 1.185"]

90 Ohm +/- 10% differential trace for DP/DM

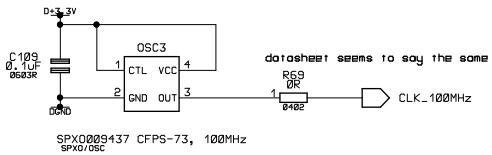
NOTE: Must read PCB layout guidelines in SX2 manual (p.49)

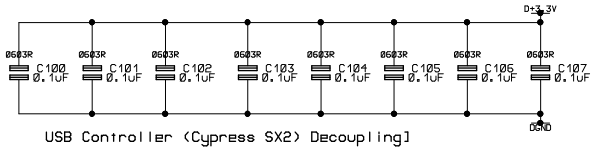


40MHz Clock



100MHz Clock





USB Controller (Cypress SX2) Decoupling

DGND
D+3.3V
USB_5V

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Title: USBDAQ/WR238		Engineer:
Subtitle: v2.0		Drawn by:
		Ver:
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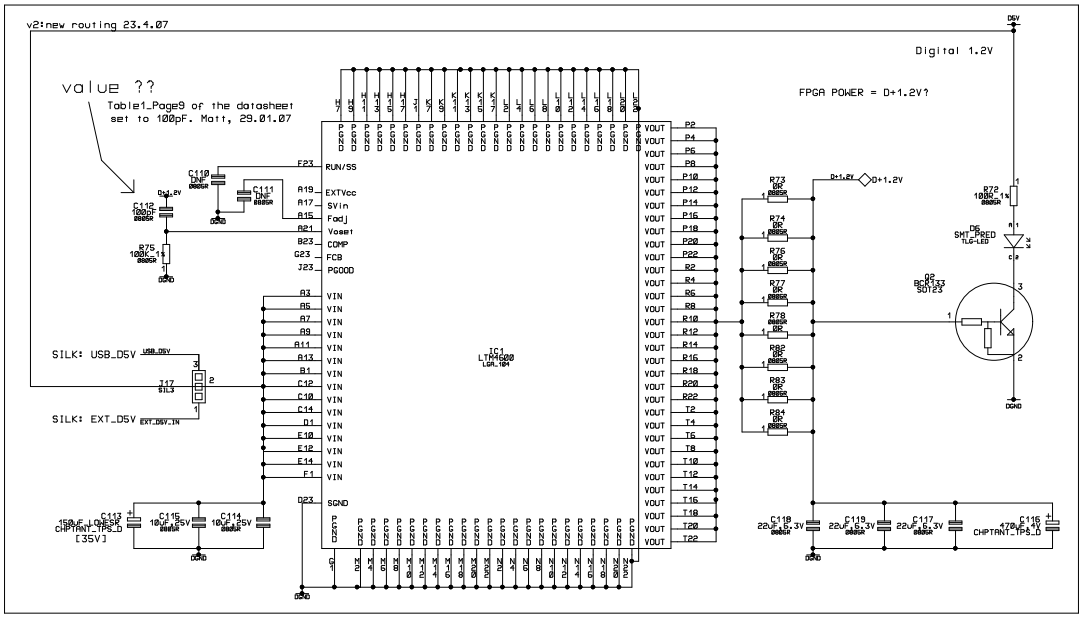
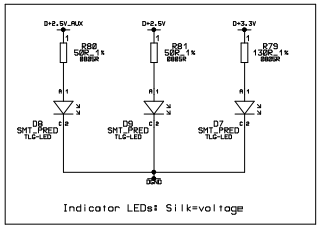
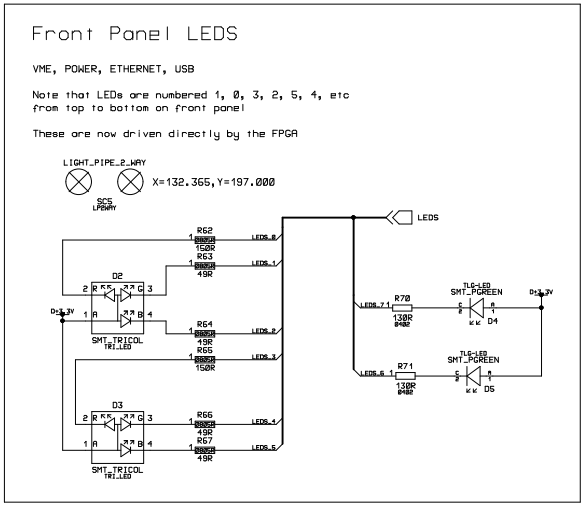
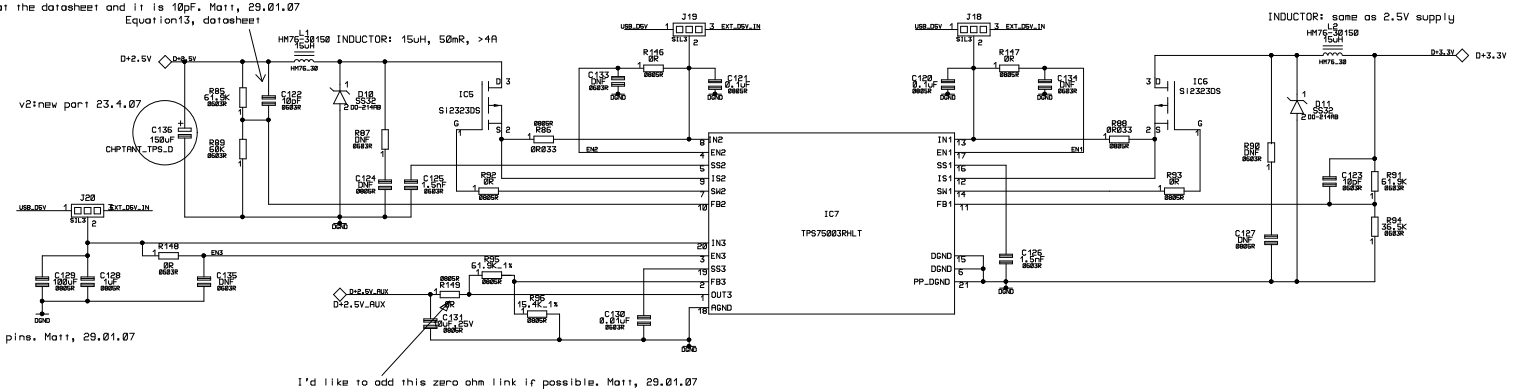


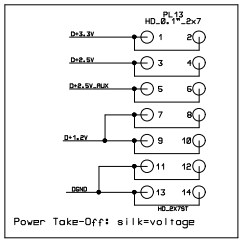


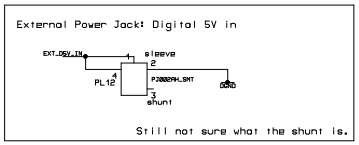


looked again at the datasheet and it is 10pF. Matt, 29.01.07
Equation13, datasheet



Added D+2.5V_AUX power connection here, doubpled pins. Matt, 29.01.07





HEP, Imperial College, London		
Title: USBDAQ/WR238		Engineer:
Subtitle: v2.0		Drawn by:
		Ver:
Sheet: 2	of: 6	Date: 23.4.07