CALICE Workpackages 2, 3 and 4

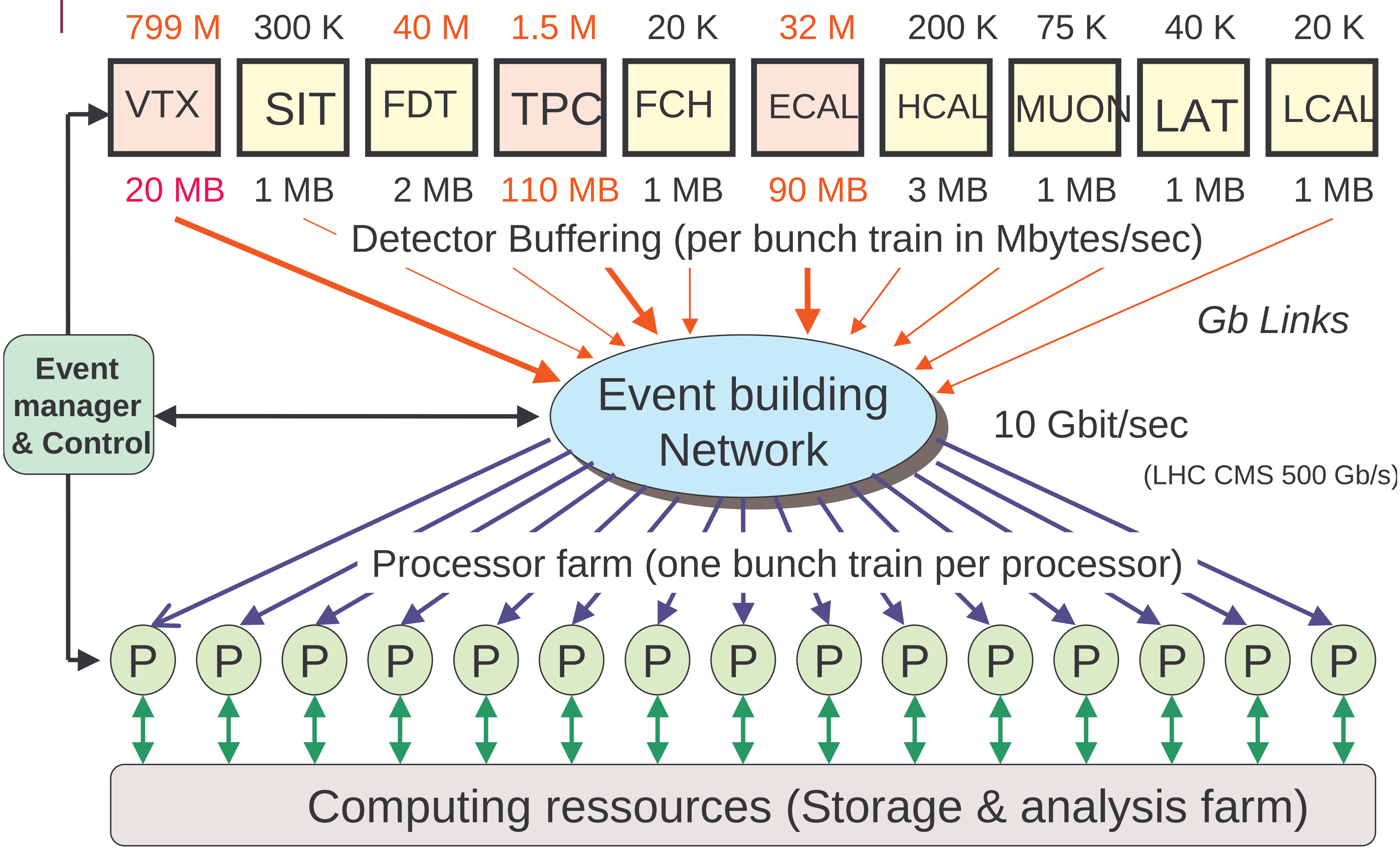
Paul Dauncey

Imperial College London

“Hardware” workpackages

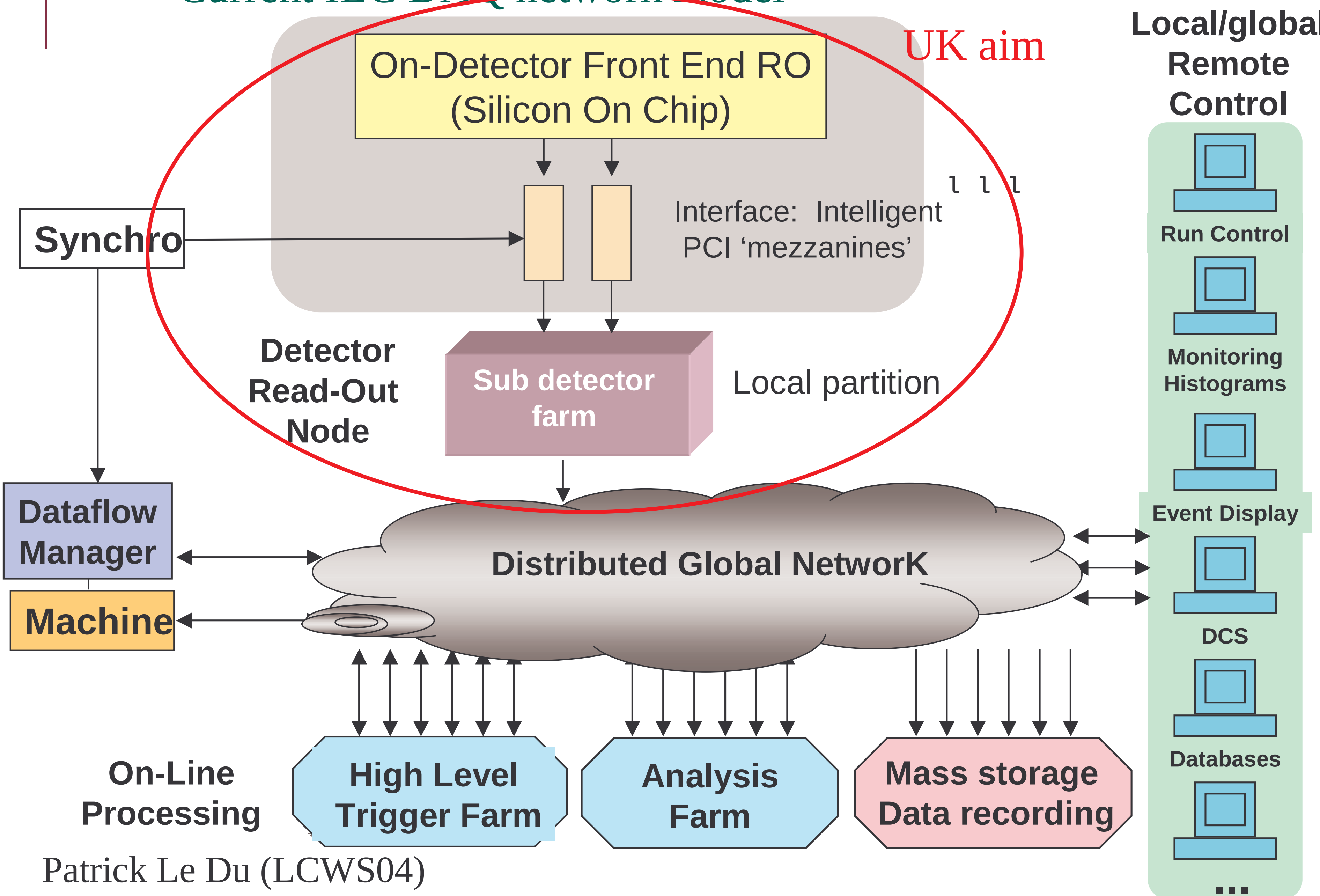
- Strategic decision
  - Want to ensure UK is positioned to take large role in calorimeters by TDR…
  - …but also believe there is enough time to be ambitious
- Hedge our bets with two major, parallel projects
  - Workpackage 2 – ECAL DAQ: definitely can be done, but many interesting issues remaining
  - Workpackage 3 – MAPS for ECAL: no existing solution yet, but a novel application of a maturing technology; very high profile if it comes off
  - In both cases, UK would be clear leader in ILC community
- Also, smaller project to take advantage of existing UK expertise
  - Workpackage 4 – ECAL thermal/mechanical issues; Manchester Atlas SCT assembly team have the knowledge to do this
  - Uses UK LHC investment to grab an important area of the ECAL
- All this work is within the CALICE collaboration umbrella

TESLA DAQ (2001)



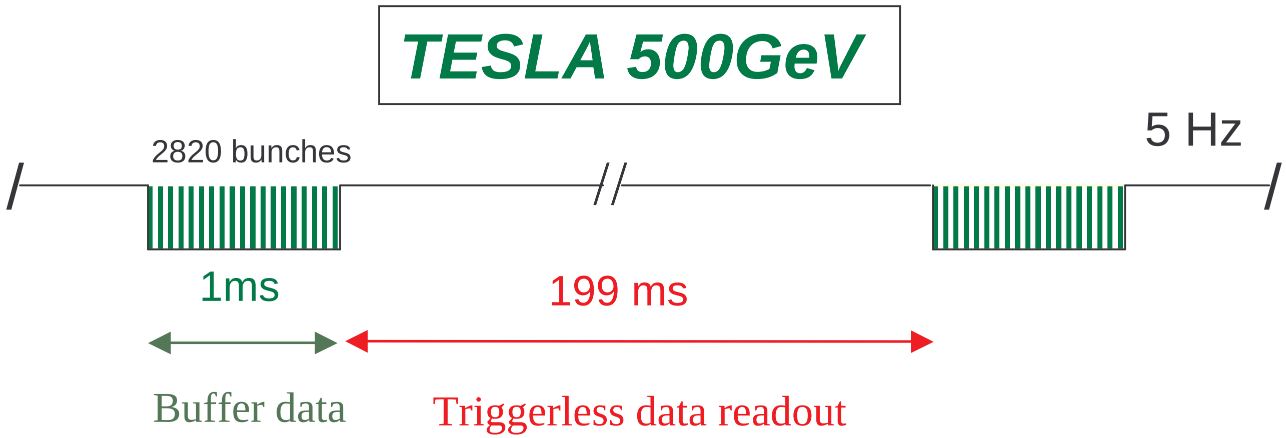
Patrick Le Du (LCWS04) 30 Mbytes/sec à 300TBytes/year

Current ILC DAQ network model



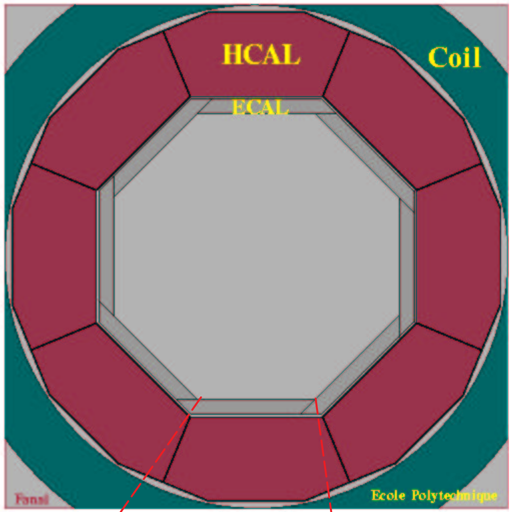
Patrick Le Du (LCWS04)

Workpackage 2 - DAQ

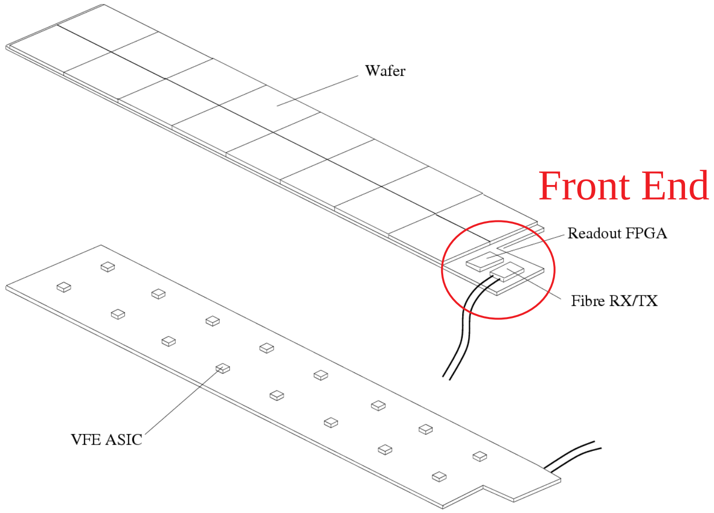


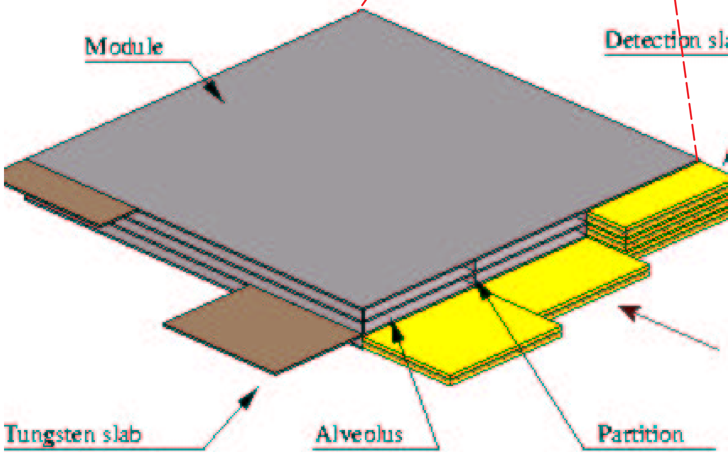
- Three parts to the DAQ system
  - On-detector: sensor/Very Front End (VFE) to Front End (FE)
  - On-detector to off-detector
  - Off-detector: receiver and farm
- Want to identify and study bottlenecks, not build DAQ system now!
  - General ILC push towards “backplaneless” DAQ
  - (Almost) all off-detector hardware commercial; minimal customisation
  - Benefits for cost, upgrades and cross-subsystem compatibility (HCAL)

DAQ – On-detector



- Wafers read out by VFE ASIC (LAL/Orsay)
  - Preamplifier and shaper per channel
  - 14 bit ADC per channel
  - Buffering and/or threshold suppression?
  - Number of channels per ASIC; 32-256

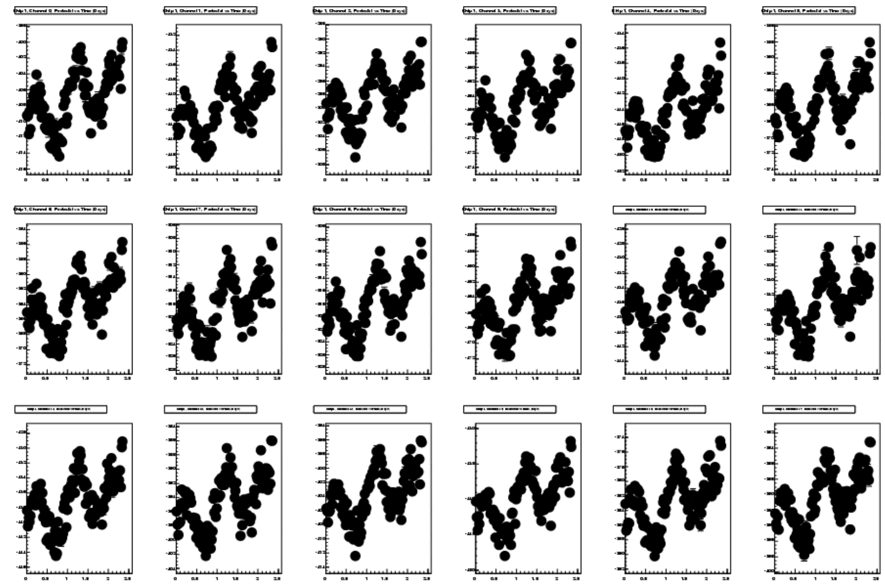




- VFE ASIC data rates during train
  - 2 bytes/channel @ 5MHz, 0.3-3GBytes/s per ASIC, 200TByte/s total ECAL
  - Probably want to do some data suppression somewhere J

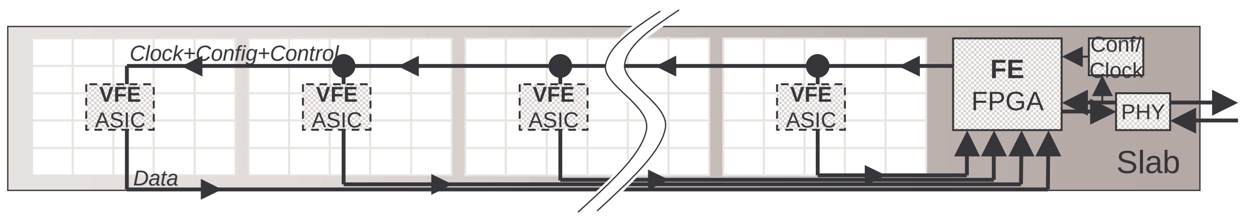
VFE readout

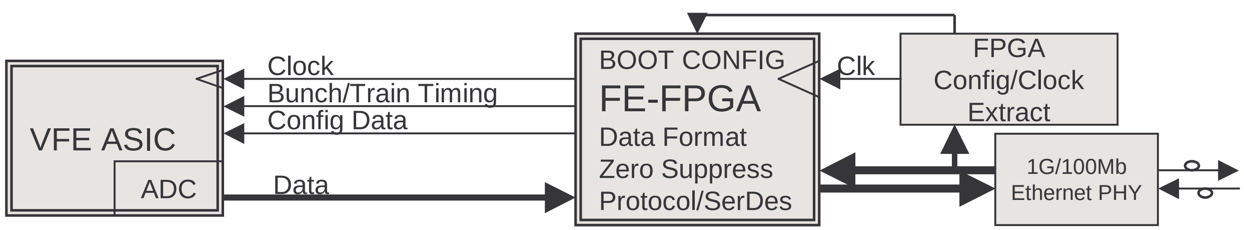
- First idea would be to suppress in VFE ASIC, but…
  - Power-cycle between bunch trains
  - Pedestals not stable to temperature
  - Need clever pedestal tracking algorithm, adjustable threshold and selective unsuppressed readout?



Pedestal variation over 2.5 days

- Much better to do in FE FPGA than ASIC; much more flexible



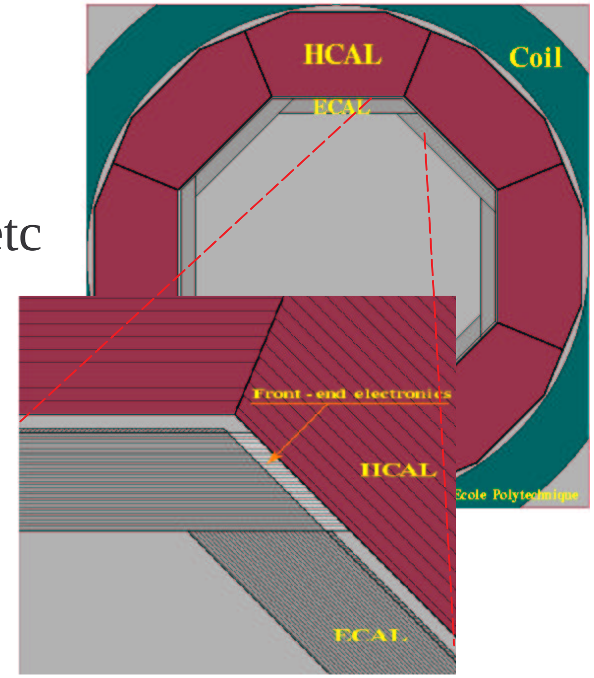


On-detector tasks

- Task 2.1: readout multiple VFE ASICs
  - Get real experience of issues involved and FE requirement
  - Feedback to new designs and redo study as new versions are produced
  - Don’t need large PCB; use simple board
  - LAL/Orsay group highly supportive; supplying large samples of VFE chips
- Task 2.2: understand data transfer of ~GBytes/s on 1.5m PCB
  - Study of transmission line performance and error recovery protocol
  - Mixture of CAD modelling and bench testing
  - No need to use real ASICs; connect two FPGAs on long PCB
  - Protocol handling would need to be designed into VFE ASIC

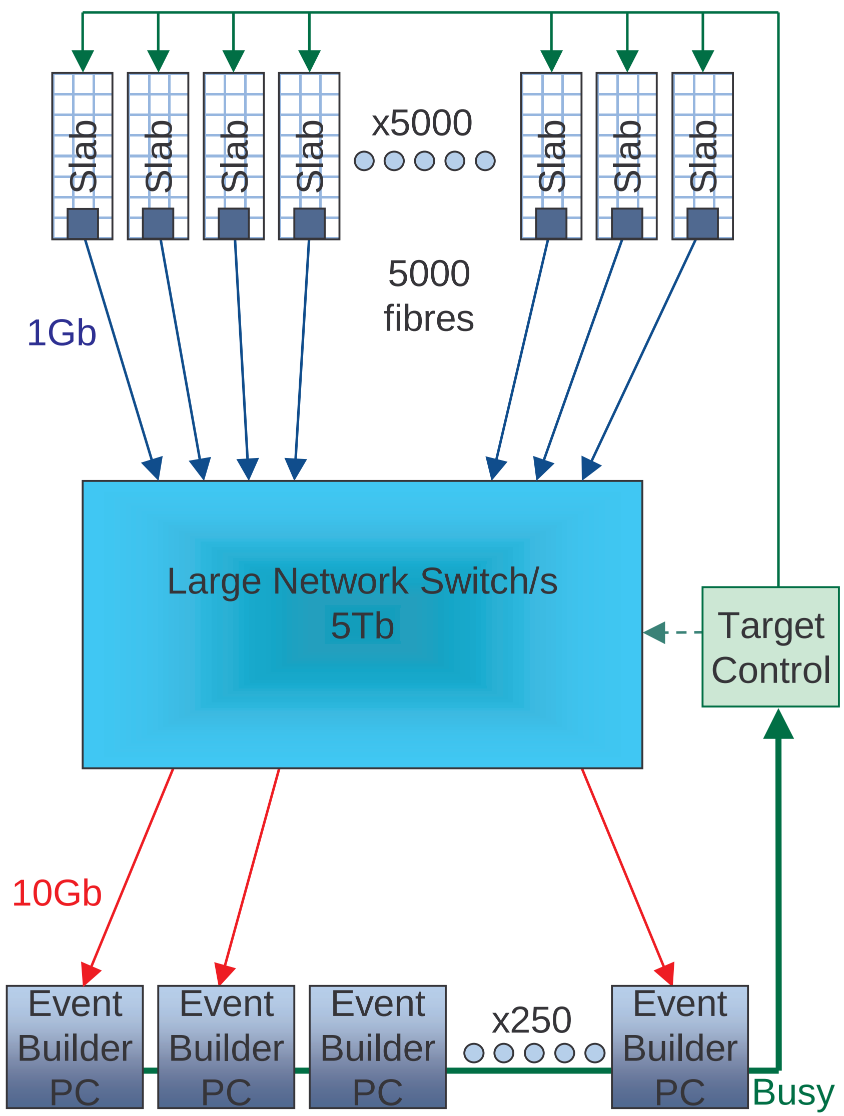
DAQ – On- to off-detector

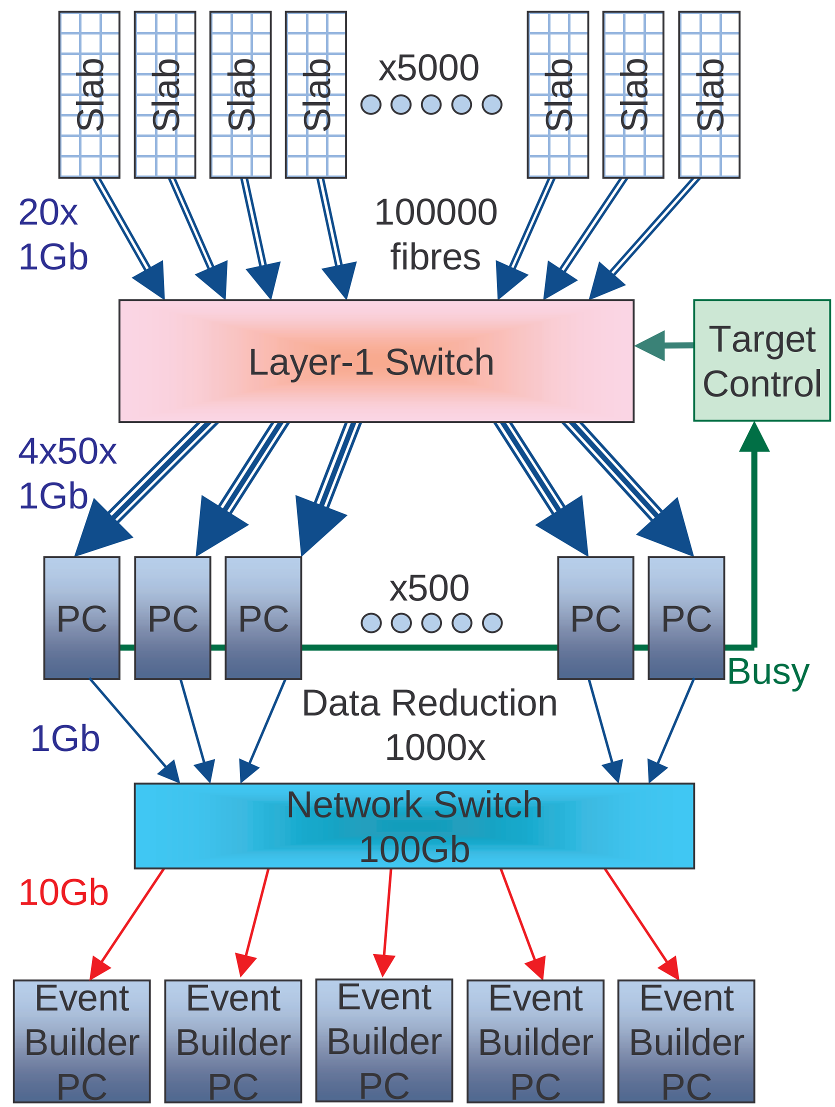
- Constrained by minimal space at end of slab
  - Few cm shared with cooling pipes, power cables, etc
  - Minimise components on-detector
- Could run TCP/IP on FE FPGA and connect directly to network
  - Bottleneck at other end of network
  - Requires large memory (~GByte) at FE



- Task 2.3: Study other options for network switching
  - Modelling and tests of data flow rates with ILC timing structure within small fast-switching networks of PCs
  - Performance studies of switching networks within failing/busy receivers and transmitters
  - Studies of optimal grouping of switches/PCs for ECAL
  - Evaluation of optical “layer 1” switch in terms of automatic re-routing of data and sending data to multiple destinations

Possible network topologies



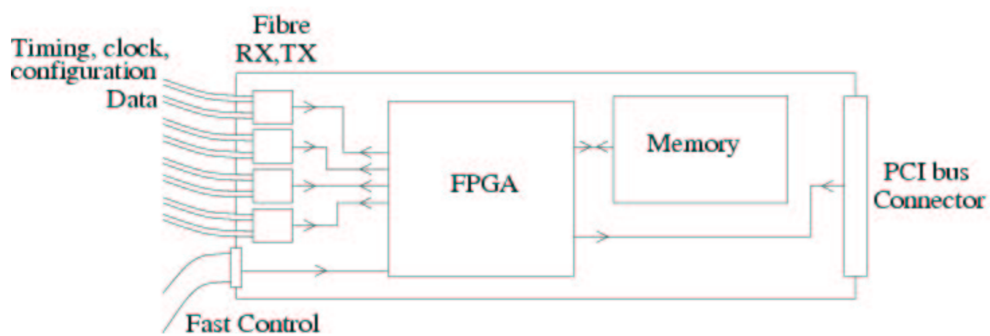


Also need reverse direction

- Need some data going upstream, off- to on-detector
  - Clock, control and configuration
  - FPGA firmware
- Need to superimpose synchronised clock and control
  - Preferably without dedicated custom Fast Control/Timing system
  - Commercial components in network; probably asynchronous and not all same clock speeds
- FE firmware reprogramming
  - Inaccessible for many years; like space hardware
  - Must be able to reprogram firmware during experiment lifetime
  - Must have failsafe system for upload so always recoverable in case of error
- Task 2.4: study aspects of these items
  - Robustness of remote reprogramming; literature search and simple test bench
  - Study clock and control synchronisation issues, using same test bench

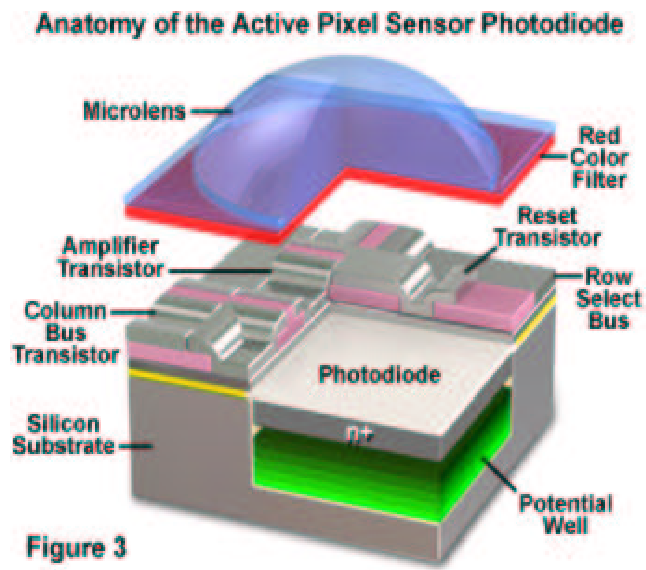
DAQ – Off-detector

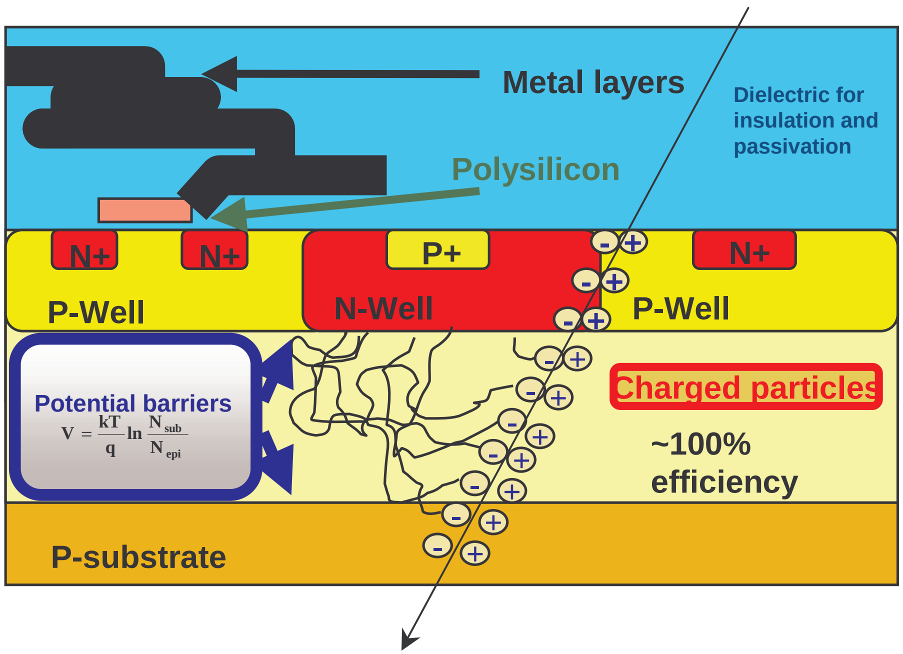
- Want to start offline reconstruction and data reduction in DAQ
  - Single hit in a layer could be a MIP or noise; need multiple layers to determine whether significant or not
  - Ideally, data for each train for whole ECAL processed in a single PC
  - May not be feasible; how much of ECAL can go into one PC?
- Task 2.5: Study of off-detector receiver
  - Simulate physics and background distributions to determine data reduction efficiency for only a fraction of ECAL in several PCs
    - Determines network bandwidth requirement downstream
  - Build test system to measure realistic rates; test bench using
    - PCI receiver card, accepting multiple fibres
    - Multiple PCI cards per PC
    - PCI Express multilane technology for PC I/O



Workpackage 3 - MAPS

- Monolithic Active Pixel Sensors
  - Developed over the last decade
  - Integrates sensitive silicon detector and readout electronics into one device
  - “Camera on a chip”; all-in-one device for light detection
  - Standard CMOS technology

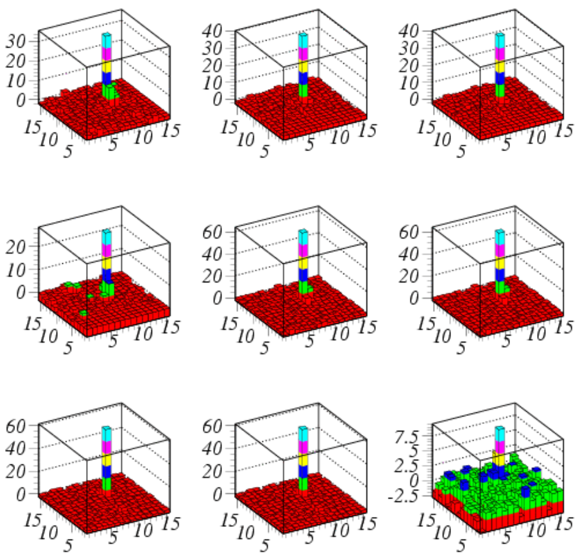




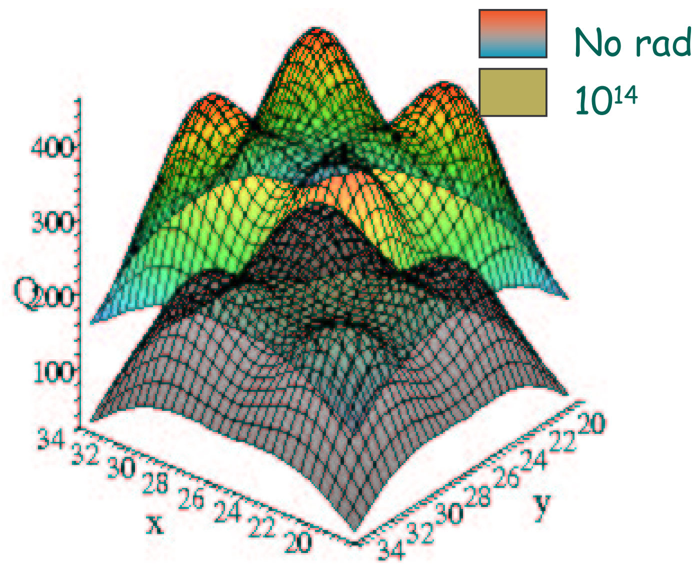
- PP/SS applications more recent
  - Need to detect higher energy X/gamma-rays or charged particles
  - Basic principle; collection of liberated charge in thin epitaxial layer just below surface readout electronics
  - In UK, PPRP granted seedcorn funding for basic development

UK “MAPS for PP&SS” collaboration

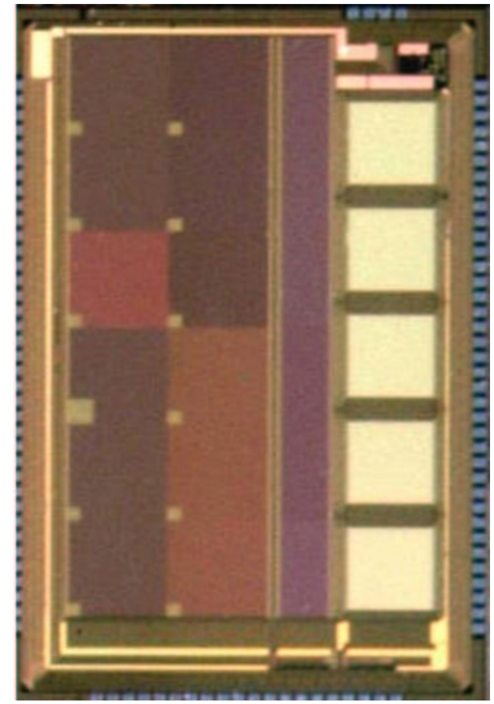
- Five institutes; Birmingham, Glasgow, Leicester, Liverpool, RAL
- Two year programme; June 2003 – May 2005
- Many aspects of sensor development
  - Multiple designs per sensor for cost reasons
  - Simulated and real devices studied; examples below



Measurements of S/N with ^{106}Ru

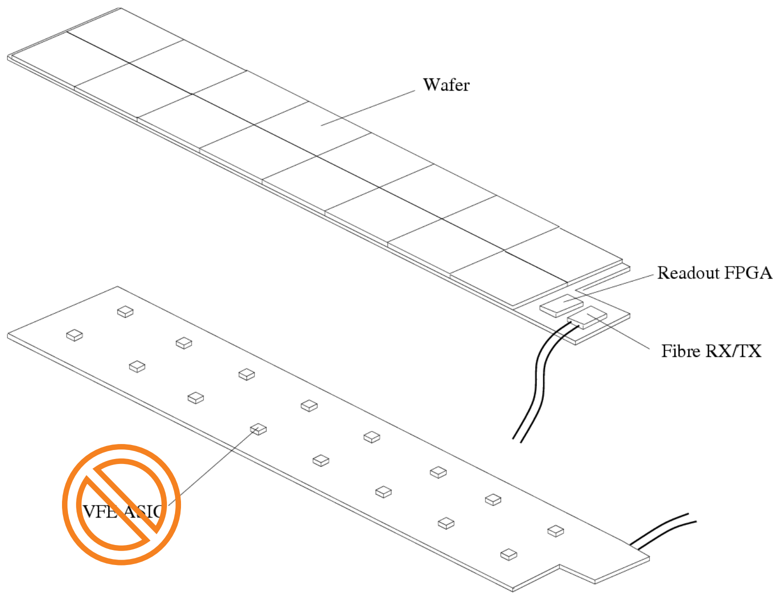


Simulation of charge collection with
4-diode structure before/after irradiation



Application to ECAL

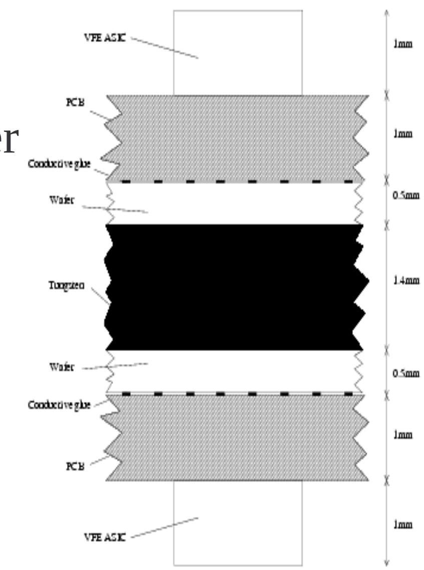
- First PPARC science application of MAPS seedcorn developments
- Replace diode pad wafers and VFE ASICs with MAPS wafers
  - Mechanically very similar; overall design of structure identical
  - DAQ very similar; FE talks to MAPS not VFE ASICs
    - Both purely digital I/O, data rates similar



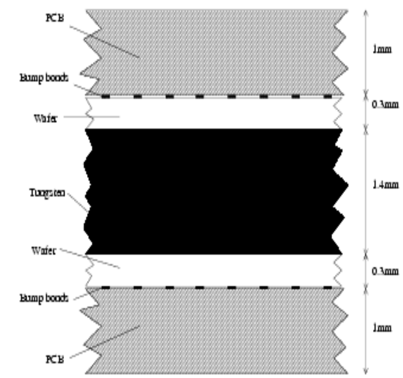
- Aim for MAPS to be a "swap-in" option without impacting too much on most other ECAL design work
  - Most of Workpackages 2 and 4 applicable to both

Advantages

- Even if MAPS identical to VFE ASIC in functionality…
  - Slab thinner due to missing VFE ASICs (and possibility of thinner wafers)
    - Improved effective Moliere radius (shower spread)
    - Reduced size (=cost) of detector magnet and outer subdetectors
  - Thermal coupling to tungsten easier
    - Most heat generated in VFE ASIC or MAPS comparators
    - Surface area to slab tungsten sheet ~1cm^2 for VFE ASIC, ~100cm^2 for final MAPS



6.4mm thick

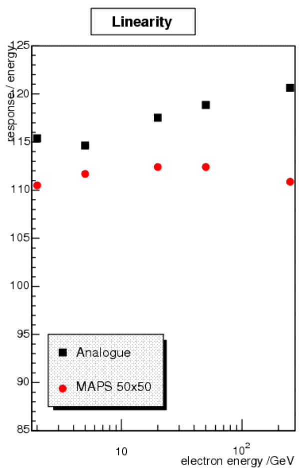


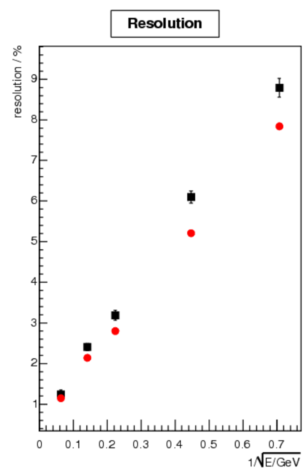
4.0mm thick

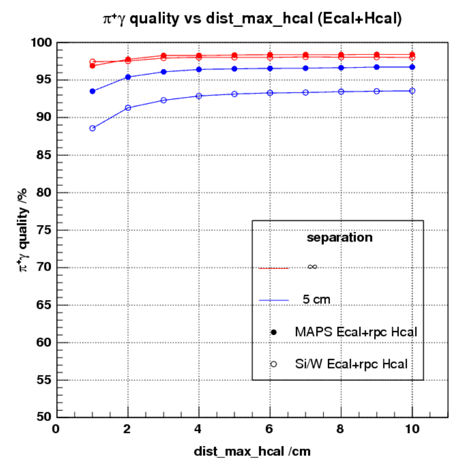
- **COST!** Standard CMOS should be cheaper than high resistivity silicon
  - No crystal ball for 2012 but roughly a factor of two different now
  - TESLA ECAL wafer cost was 90M euros; 70% of ECAL total of 133M euros
  - That assumed 3euros/cm^2 for 3000m^2 of processed silicon wafers

But can do even better…

- Forget VFE and go to much finer pixels
  - Choose size so probability of more than one particle is small
  - Can then have comparator and simple binary readout
- How fine? EM shower core density at 500GeV is ~100/mm
  - Pixels must be < 100×100μm^2; working number is 50×50μm^2





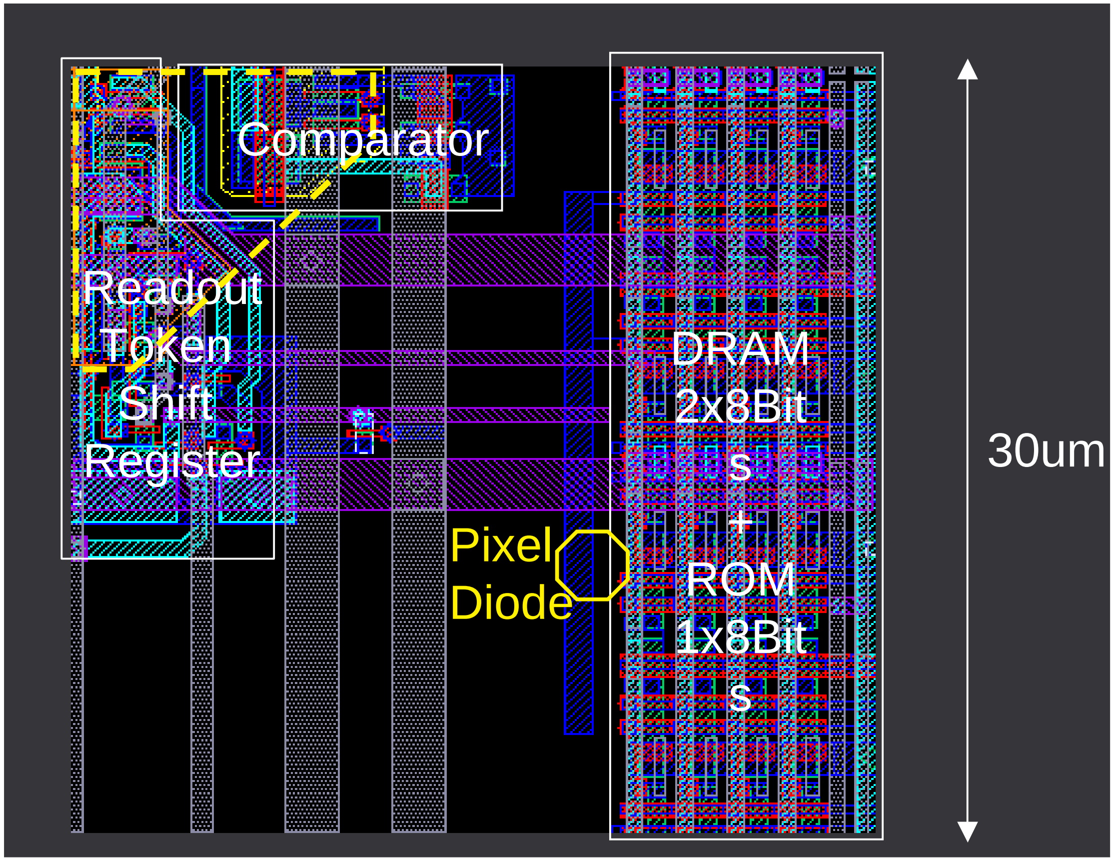


Two-particle separation

- Simulation shows improvement in performance
  - Diode pads measure energy deposited; depends on angle, Landau, velocity
  - Binary pixels measure number of particles; better estimate of shower energy
  - Finer granularity also improves two-particle separation

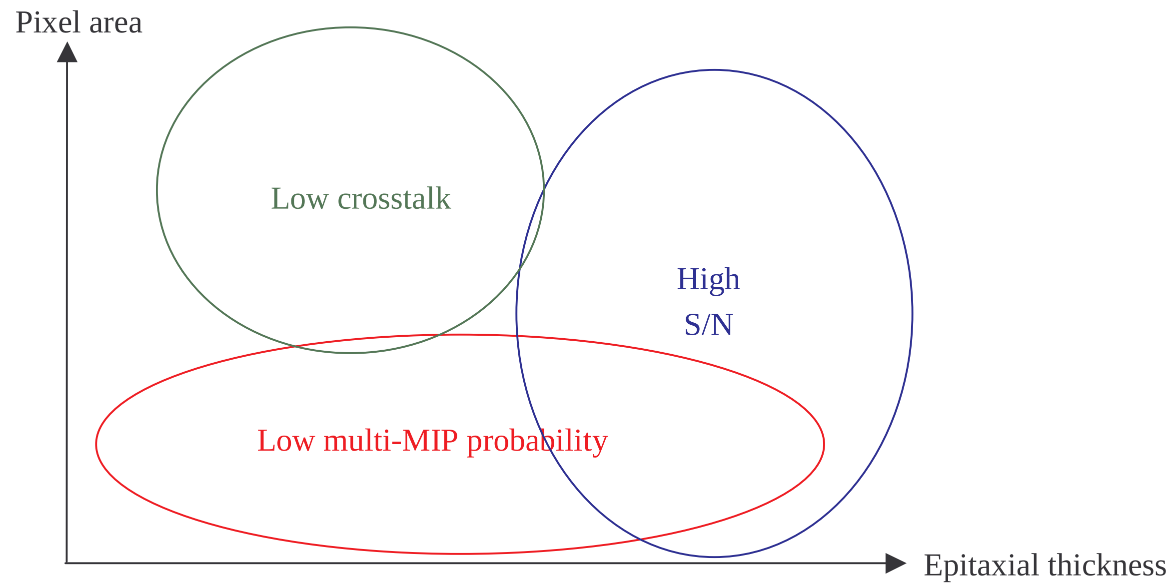
Pixel digital readout

- Buffer data during bunch train, readout afterwards
  - Store bunch crossing number whenever signal about threshold for each pixel
  - Need comparator and in-pixel memory, accessed by readout bus
- Similar to MAPS requirements for sensor of MI^3 project
  - Design including exactly these elements being fabricated next month
  - Designer (J.Crooks) will join CALICE
  - CALICE will also be able to test a few of these sensors



Pixel analogue requirements

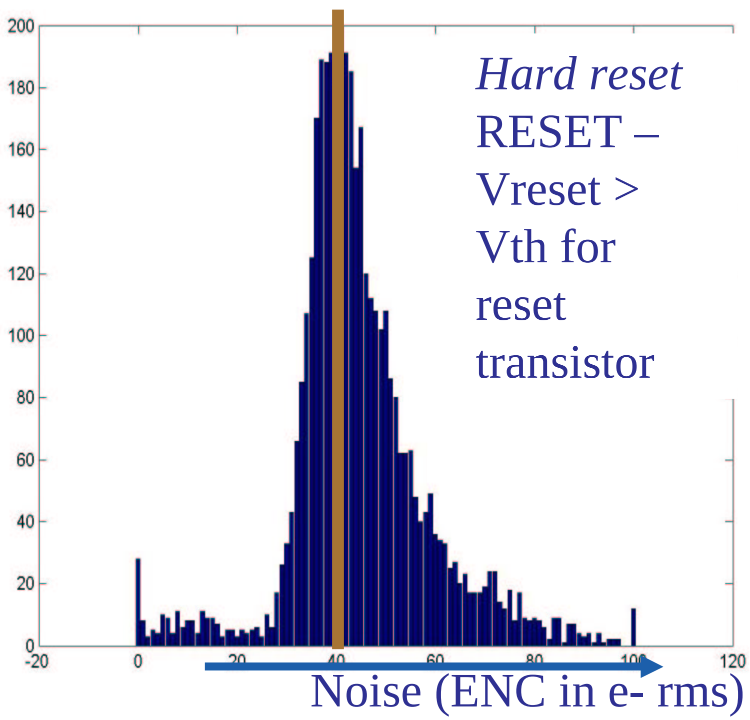
- Studies are needed to optimise
  - Charge sharing (crosstalk), MIP S/N, MIP multiple hits/pixel
  - Dependent on pixel area, epitaxial thickness, threshold, diode geometry, etc

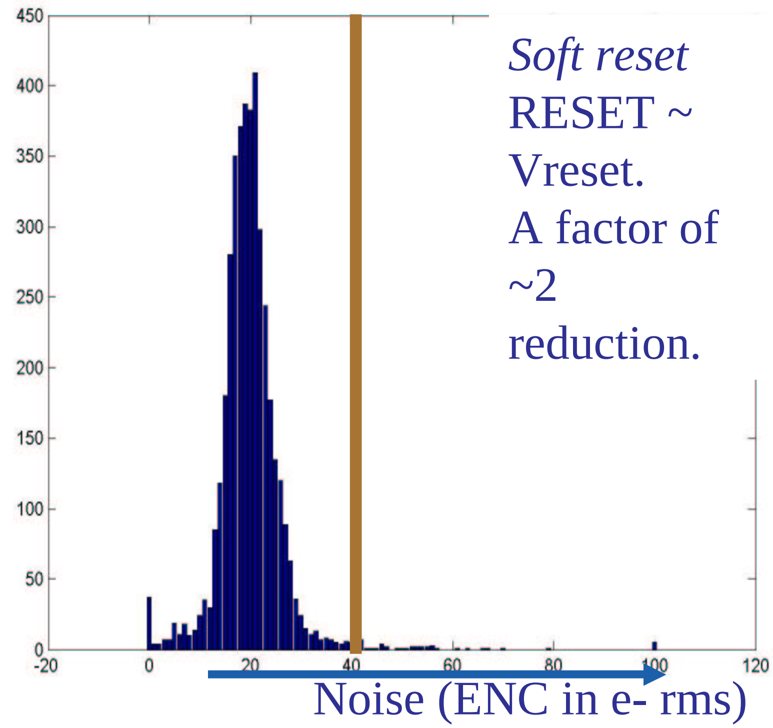


- Noise rate target < 10^{-6} (~5σ) to be less than physics background
  - DAQ and pattern recognition could handle (at least) ~10^{-5}
- Large parameter space; need to find best combination
  - Physics-level simulation needed to guide choices

Noise: soft vs hard reset

- Noise normally dominated by pixel reset, every bunch crossing
- Lower voltage “soft” reset; factor of two improvement seen
  - Not all charge cleared by next bunch crossing; “image lag”
  - Not a problem at ILC; Bhabha rate ~1 in 500 crossings, hit ~0.1% of ECAL
  - Interesting possibility; charge leaking (no reset) over several crossings

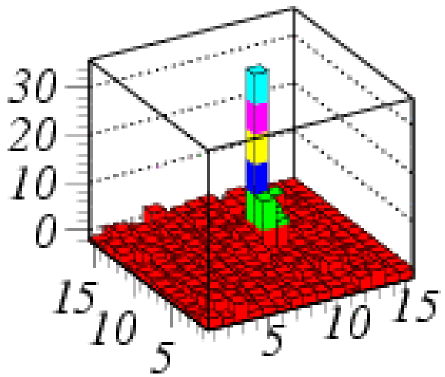




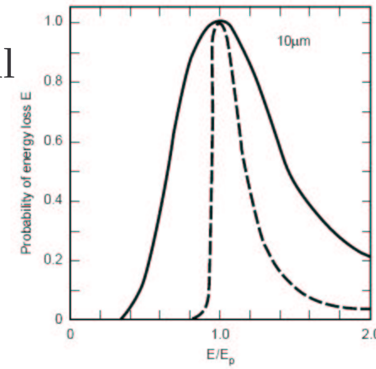
Signal/noise and crosstalk

- Signal/noise of > 20 measured with 3×3 pixel cluster
  - Average ~50% of signal seen in central pixel
  - Thin (8µm) epitaxial layer; requires threshold ~0.4 signal ~4σ

Liverpool

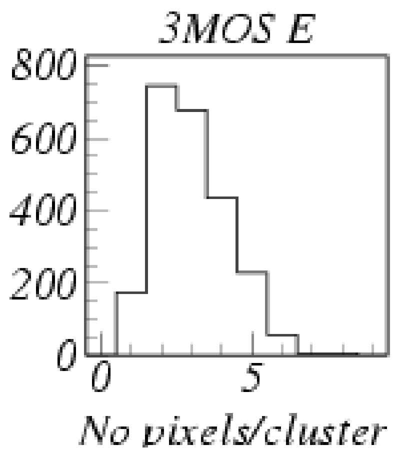


C.Damerall



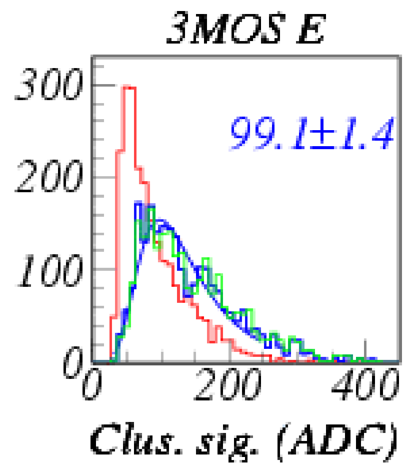
- Pixel size only 15×15µm^2 so crosstalk was significant
- But limited to 3×3 array ~ pixel size considered for ECAL

Liverpool



3x3 pixels

Cluster
1x1 pixels
3x3 pixels
5x5 pixels



Other requirements

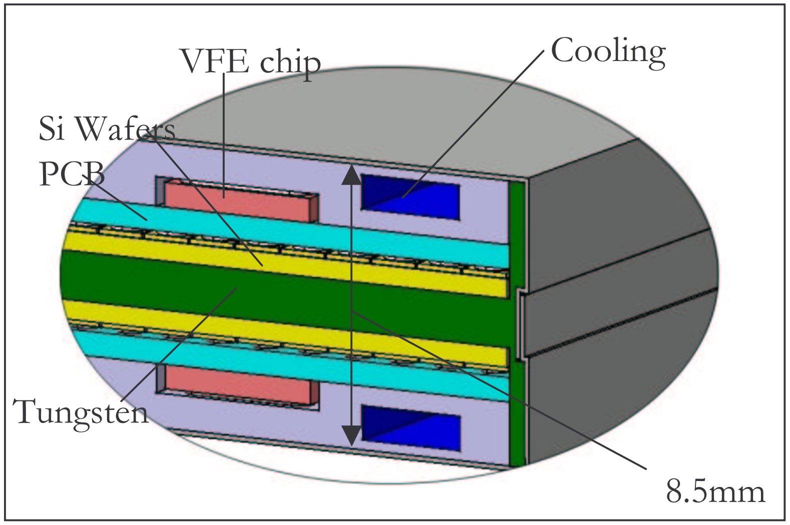
- Also need to consider power, uniformity and stability
  - Power must be similar (or better) that VFE ASICs to be considered
    - Main load from comparator; ~2.5μW/pixel when powered on
    - Investigate switching comparator; may only be needed for ~10ns
    - Would give averaged power of ~1nW/pixel, or 0.2W/slab
    - There will be other components in addition
    - VFE ASIC aiming for 100μW/channel, or 0.4W/slab
  - Unfeasible for threshold to be set per pixel
    - Prefer single DAC to set a comparator level for whole sensor
    - Requires sensor to be uniform enough in response of each pixel
    - Possible fallback; divide sensor into e.g. four regions
  - Sensor will also be temperature cycled, like VFE ASICs
    - Efficiency and noise rate must be reasonably insensitive to temperature fluctuations
    - More difficult to correct binary readout downstream

There is only one task

- Task 3.1: Determine if MAPS are viable for an ECAL
- Two rounds of sensor fabrication
  - First with several pixel designs, try out various ideas
  - Second with uniform pixels, iterating on best design from first round
- Testing needs to be thorough
  - Device-level simulation to guide the design and understand the results
  - “Sensor” bench tests to study electrical aspects of design
  - “System” bench tests to study noise vs. threshold, response to sources and cosmics, temperature stability, uniformity, magnetic field effects, etc.
  - Physics-level simulation to determine effects on ECAL performance
- Verification in a beam test
  - Build at least one PCB of MAPS to be inserted into pre-prototype ECAL
  - Replace existing diode pad layer with MAPS layer
  - Direct comparison of performance of diode pads and MAPS

Workpackage 4 – Thermal/mechanical

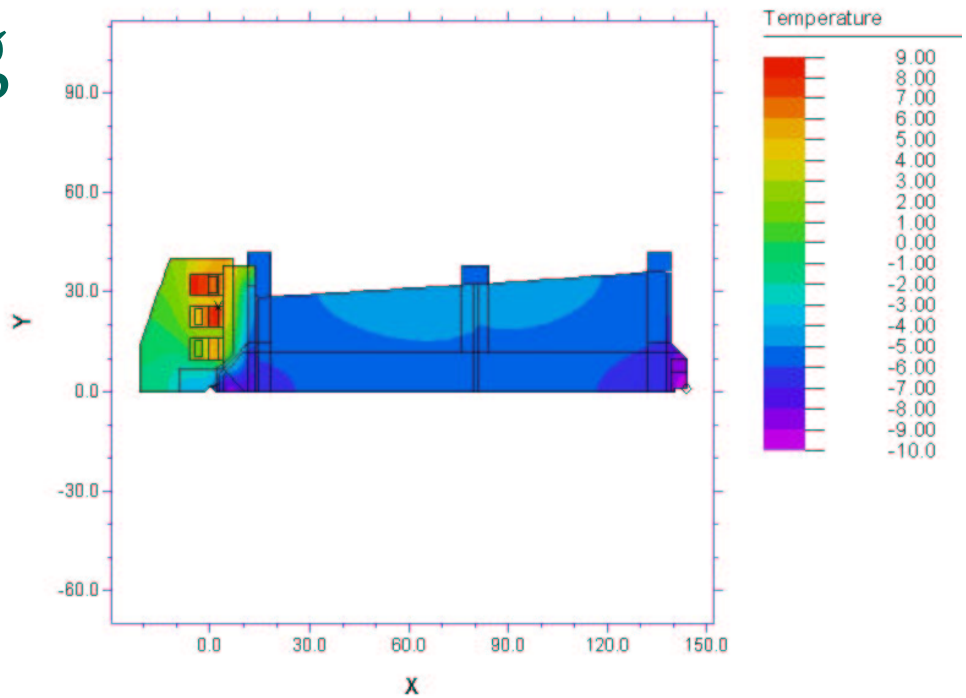
- ECAL is very dense; how do we get the heat out?
  - VFE is largest heat source; 100μW per channel when pulsed
- Thermal structure is complex
  - Power cycling for bunch trains means heat flow is never exactly steady state
  - Carbon fibre heat conductivity depends on fibre direction
- Biggest unsolved issue
  - Can cooling be at edges of ECAL only ("passive" cooling)?
  - Do pipes need to be brought inside the main structure ("active" cooling)?



- Cooling tubes ~1mm?
  - Add to effective Moliere radius
  - Increase ECAL size and cost
  - N.B. MAPS have no VFE chip

Thermal modelling

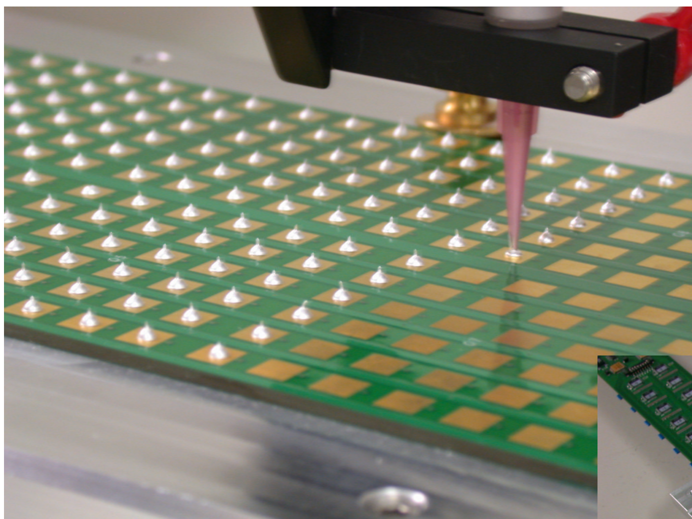
- Manchester group have experience in FlexPDE
  - Thermal modelling of SCT modules for ATLAS

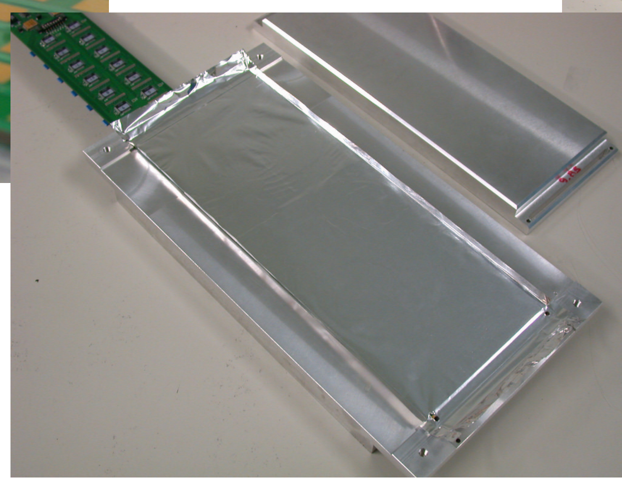


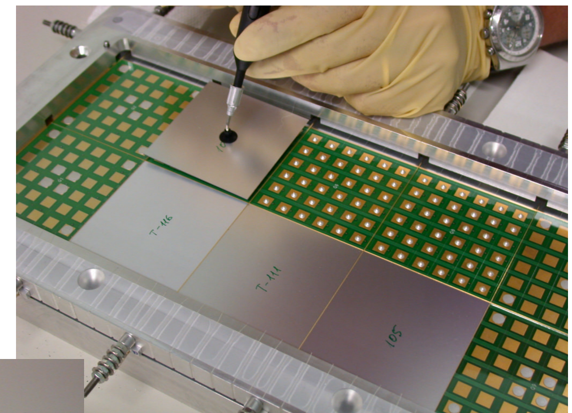
- Task 4.1: Perform thermal modelling to study issues
  - Accurately measure heat output of VFE chips (and other components)
  - Model both passive and active cooling structural designs, including different active coolants and MAPS option
  - Feed back results to mechanical design team
  - Verify accuracy of thermal modelling by comparison with measurements on detector slab mock-ups

Pre-prototype PCB construction

- Diode pads attached directly to PCB using conductive glue; ground contact to outer side of wafer using aluminium foil
  - Glue deposition automated
  - Wafer positioning and foil attachment done by hand







Final assembly must be automated

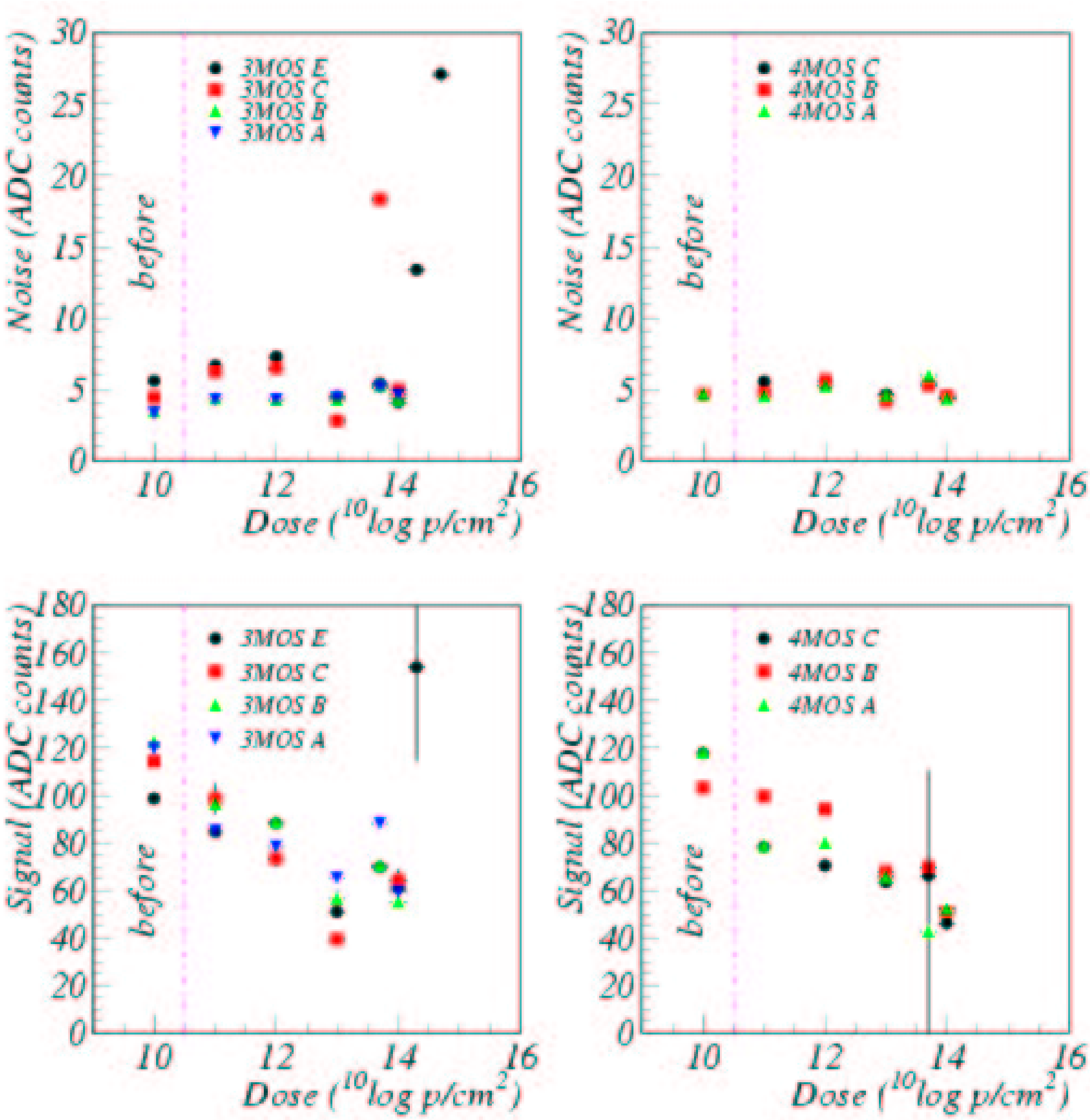
- Pre-prototype PCBs have 216 channels (= blobs of glue) and six wafers to position
  - Complete ECAL requires 60 PCBs
  - Each takes two days to complete; currently pacing schedule
- Final ECAL will have PCBs with ~4000 channels
  - Complete ECAL requires ~5000 PCBs
  - Must be industrialised and PCBs done in parallel
- Task 4.2: Study of possible glues
  - Aging through thermal cycling, failure rates, glue diffusion into wafer
- Task 4.3: Automation of assembly
  - Robot design to apply glue, wafers and foil over full 1.5m area
  - Build prototype robot and test accuracy (glue dispensing and wafer placement)
  - Reuse some equipment and machine vision software (for alignment) from similar Atlas work

Conclusions

- We have established the UK in ILC calorimetry
  - Current CALICE programme has gone very well
  - Now need the remaining funds to finish this study
- We can now place the UK in an important position in ILC calorimetry long term
  - We have done the groundwork and are ready to go
- Our strategy is to take two major paths
  - Whatever the outcome of the TDR technology choices in 2009, we can then be sure to have a leading role in the ECAL
- To do this, we need both a strong team and adequate resources
  - If we want to be major players, we need to invest now

BACKUP SLIDES

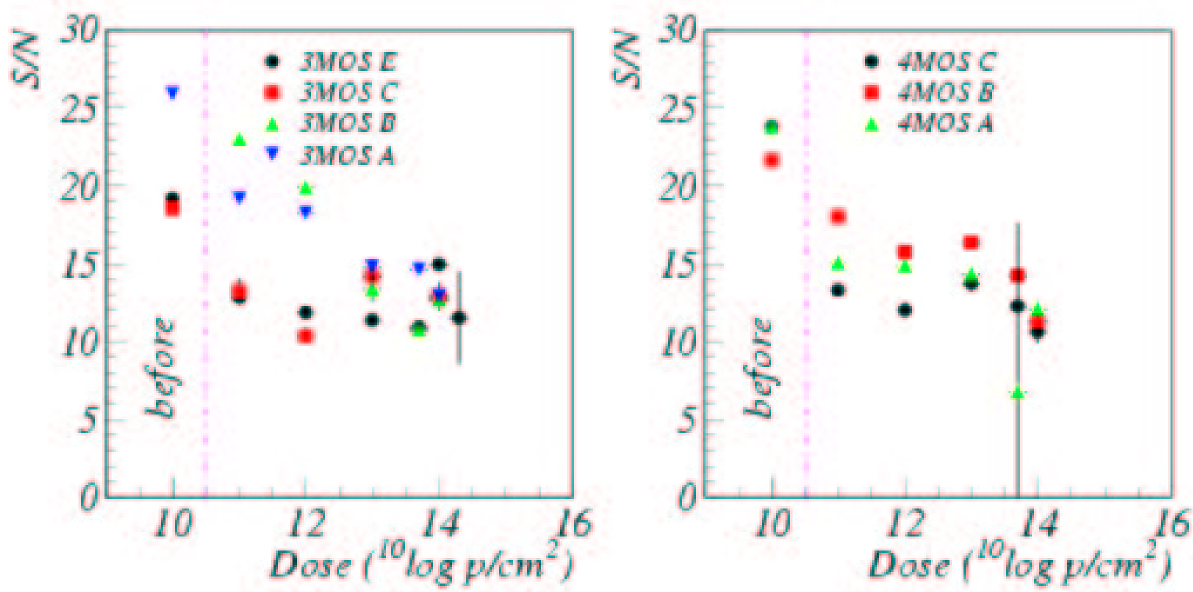
Radiation test. Source results



- Noise seems to increase slightly with dose.
- Signal decreases with dose.

3MOSA	3x3 μm^2
3MOSB	1.2x1.2 μm^2
3MOSC	GAA
3MOSE	4 diodes
4MOSA	Reference
4MOSB	Higher V_T
4MOSC	Lower V_T

Radiation test. Summary



- Sensors yield reasonable S/N up to 10^{14} p/cm^2
  - ! No efficiency measurement; need testbeam data
- 0.35 μm technology in the pixel transistors. Enclosed layout in 3MOS_E
- Especially 3MOS_E (4 diodes) looks interesting
  - - Larger capacitance yields larger noise
  - + Four diodes: less dependence of S/N on impact point
  - + After irradiation remains a larger “sensitive area”

J. Velthuis (Liv)