DESY PRC Report
The SPiDeR Collaboration

N.K. Watson, J.A. Wilson
School of Physics and Astronomy, University of Birmingham, Birmingham, B15 2TT, United Kingdom.

D.G. Cussans, J. Goldstein, J.J. Velthuis
H.H. Wills Physics Laboratory, University of Bristol, Tyndall Avenue, Bristol BS8 1TL, United Kingdom.

P.D. Dauncey
Blackett Laboratory, Imperial College London, Prince Consort Road, London SW7 2AZ, United Kingdom.

R. Gao, Y. Li, A. Nomerotski
Denys Wilkinson Building, University of Oxford, Keble Road, Oxford OX1 3RH, United Kingdom.

R.E. Coath, J.P. Crooks, M. Stanitzki, J. Strube, R. Turchetta, M. Tyndel, S. Worm, Z. Zhang
STFC Rutherford Appleton Laboratory, Chilton, Didcot, OX11 0QX, United Kingdom.

Contents

1 Introduction

SPiDeR (**S**ilicon **Pi**xel **De**tector **R**&D) [1] is a new UK-based collaboration working on silicon pixel R&D for future colliders. As particle physics colliders continue to reach higher energies and luminosities, finely segmented, low power, low cost pixel detectors will be required for vertexing, tracking and for electromagnetic calorimetry. Low power and cost are clearly crucial for large area applications, such as tracking and calorimetry. With an emphasis on the relatively clean environment of lepton colliders, high granularity has been shown to be important for the jet energy resolution using particle flow algorithms (PFA). Such algorithms require efficient separation of the jet into its constituent particles, with information relevant to each particle being measured in the detector with the best resolution, species by species. Specifically, charged particles are optimally measured in tracking chambers, photons in electromagnetic calorimeters and neutral hadrons in hadron calorimeter. The critical aspect for the PFA approach is to assign correctly all the energy in the calorimeters to avoid double counting, as the so-called "confusion" term can dominate the jet resolution obtained.

SPiDeR will concentrate on using CMOS Monolithic Active Pixel Sensors (MAPS) to achieve the goals of future detectors in terms of segmentation and resolution. The goal of SPiDeR is to investigate the key technical issues associated with silicon pixel sensors at future experiments. These include: exploring the use of novel, low-noise structures; making best use of in-pixel intelligence; and studying the best compromise between low-power consumption and performance. To some extent, each of these will depend on the specific physics environment for which the sensor is being optimised. Several devices have already been made and SPiDeR will design, fabricate and test three new sensors over the next three years. Their performance will be measured using hadronic and electron test beams at CERN and DESY. In addition, the devices will also be assessed for radiation hardness using photons, protons and neutrons. One of the first applications to be studied in detail using SPiDeR sensors will be a prototype electromagnetic calorimeter. This will provide a first demonstration of the potential of digital electromagnetic calorimetry, the so-called DECAL.

2 Historical context of SPiDeR

The UK has a long and successful history in silicon pixel R&D for linear colliders. Recently, this has involved covering a range of activities in both the CALICE and LCFI Collaborations. UK groups within CALICE have been working on a digital electromagnetic calorimeter (DECAL) using MAPS. This led to the design of the TPAC sensor for studying this application, which is described in Section 5. Three iterations of this device were made and they have been extensively tested with sources, lasers and beam. The pixel groups within LCFI worked with charge-coupled devices (CCD) primarily for linear collider vertex detectors, both on Column-Parallel CCDs (CPCCD) and In-Situ-Image Storage (ISIS) sensors.

In December of 2007, the Science and Technology Facilities Council (STFC), the main funding body for UK particle physics, unilaterally decided to "cease investment" in ILC accelerator and detector R&D in the light of a major deficit in its budget. Subsequent to this decision, funding for both the LCFI and CALICE-UK projects was rapidly reduced, with an official end of funding from STFC in December 2008 and March 2009, respectively. Despite substantial protests from the UK community and a consultation process which included a strong UK community input, the ILC-specific activities were not reinstated. In its place, a modest budget for generic R&D for both accelerators and detectors was allocated. The pixel groups from both CALICE-UK (Birmingham, Imperial College and RAL) and LCFI (Bristol, Oxford and RAL) decided to form a collaboration for generic silicon pixel detector R&D, which would have future linear colliders as a potential application. The Collaboration included members of RAL who

were also working on the FORTIS sensor (see Section 4), which was designed to study advanced pixel architectures. The Collaboration submitted a proposal which included continuing work on TPAC and ISIS, plus extending the FORTIS work to new readout architectures (CHERWELL) and construction of a DECAL demonstrator. This proposal was reviewed in October 2008 and the recommendation from the STFC Project Peer Review Panel was that funding would be provided only for the TPAC, DECAL and the CHERWELL parts of the proposal, and that additional funding to continue development and testing of the established ISIS programme could not be made available given extremely limited resources.

The SPiDeR programme was then approved and final preparations to issue funding from April 2009 were made. However, given continuing uncertainty about the balance between known commitments (of which particle physics represents a small part) and unknown budget allocations in future years, STFC decided to suspend the award of funding for this project for a year. Consequently, SPiDeR is on bridging funds until April 2010, at which time it is anticipated that the approved funding will be released.

3 Underpinning technologies

The use of silicon sensors, including CCDs and hybrid silicon pixel detectors for vertexing, hybrid silicon strip detectors for tracking and silicon pad detectors for luminosity monitoring is by now well established in particle physics. Silicon is the technology of choice where high precision measurements are required and its use is likely to continue into the future, which is evident from the current proposals for sLHC upgrades and the recently validated ILC detector concepts [2, 3]. The requirement now is to develop novel solutions which have faster readout and/or lower power density so that the material per silicon layer can be reduced by factors of 2–5. In addition the cost per unit area is a limiting factor, particularly for tracking and calorimetry applications. SPiDeR is focused on developing MAPS which provide the required granularity for future high energy and high luminosity experiments but also addresses the major issues such as power consumption, connectivity and cost reduction. Because a monolithic silicon device integrates both the sensor and the front-end electronics, it immediately decreases the material per measurement layer and simplifies assembly. The use of CMOS processes available from multiple vendors, compared with silicon detectors requiring specialised processing, provides a cost benefit and opens up the use of MAPS for large area applications like tracking and calorimetry.

3.1 Monolithic active pixel sensors

In the early 1990s, CMOS MAPS were proposed as imaging sensors. CCDs were then the dominant imaging technology but it was immediately recognised that an image sensor in CMOS has significant cost advantages as it allows the integration of the sensor with sophisticated readout electronics including analogue-to-digital conversion and signal processing. It also allows very small pixel sizes building on the reduction in feature size of CMOS. In addition, the technology has continued to improve by the introduction of features such as low dark current diodes and charge transfer, which were previously found only in CCD technology.

The use of CMOS sensors for particle physics was first proposed by a member of SPiDeR [4]. It was quickly shown that the devices can act as particle detectors and that they have the following attractive features:

- High granularity: pixel sizes down to about 1 μm and below are possible
- Simplicity: CMOS integration lowers the need for high density connection to external electronics, which requires complicated flip-chip technologies in hybrid pixel detector systems.

- Low cost: CMOS is a mature, industrial process with many vendors (although some types of particle detectors might require additional processing).
- Low power: Pixels are only active during readout and also CMOS has low voltage levels.

However, there are a number of limitations of the technology which have delayed the take-up in particle physics experiments. The size of the induced signal is small because the sensitive layers are thin (5–15 μm). Also, the time taken for signal to develop is large because the devices rely on diffusion to collect the charge. This also affects the radiation tolerance of the sensor as charge will be lost by trapping after irradiation. Another perceived limitation of MAPS is not having full CMOS capability as the additional N-wells from the PMOS transistors parasitically collect charge, thus reducing the charge collected by the readout diode. Avoiding the usage of PMOS transistors however does limit the capability of the readout circuitry significantly. In order to overcome these limitations, SPiDeR and its predecessors have been working on CMOS process enhancements with a leading-edge CMOS image sensor foundry for several years.

3.2 Deep P-well implants

The ideal situation would be to achieve full CMOS capability and maximise the charge collection efficiency at the same time. Therefore, a special deep P-well layer was developed to overcome the problems mentioned above. The deep P-well protects charge generated in the epitaxial layer from being collected by parasitic N-wells for the PMOS. This then ensures that all charge is being collected by the readout diode and maximises charge collection efficiency. This is illustrated in Figure 1.

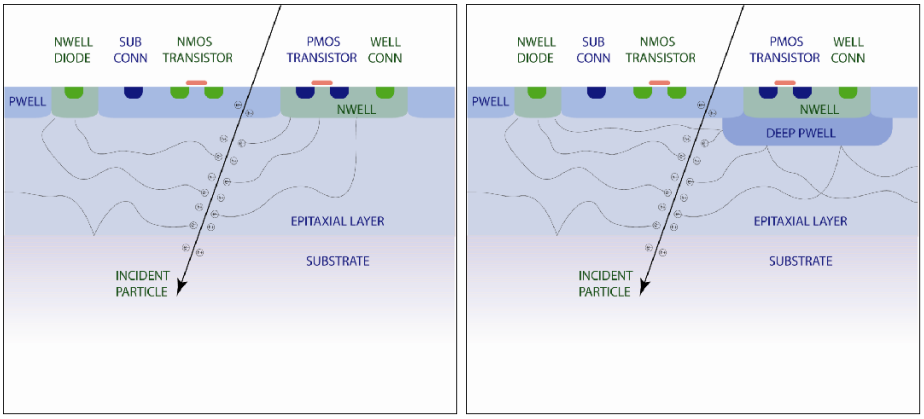

Figure 1: A CMOS MAPS without a deep P-well implant (left) and with a deep P-well implant (right).

This enhancement allows the use of full CMOS circuitry in a MAPS and opens completely new possibilities for in-pixel processing. The deep P-well layer was patented by STFC (US2006/0278943) and is currently being used in other projects outside the particle physics community and in the commercial area. This is a great example of a research result that has a direct spin-off into industry and shows that the potential of this technology is "generic" and extends well beyond the strict remit of the particle physics community.

The 180 nm INMAPS process used for the TPAC and FORTIS sensors does include the deep P-well as one of its options. These sensors were made both with and without the deep P-well processing step and the difference in performance of the TPAC sensor is discussed in Section 5.

3.3 High resistivity epitaxial layers

The benefits of using a high-resistivity epitaxial layer to manufacture MAPS sensors in the INMAPS process has also been explored.

A high-resistivity epitaxial layer should improve charge collection efficiency and reduce cross talk effects by allowing the depletion region of the diode to extend further into the silicon. It is also expected to increase the radiation hardness of MAPS devices by reducing the charge collection time thus making the sensor less sensitive to minority carrier lifetime degradation due to charge irradiation [6].

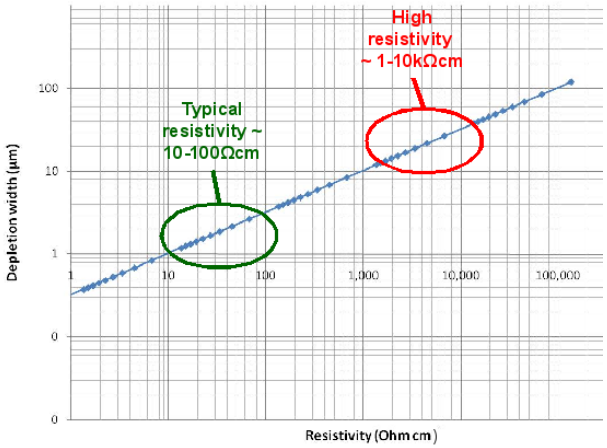

Figure 2: Depletion width versus epitaxial layer resistivity for a standard CMOS wafer (green) and a wafer with a high-resistivity epitaxial layer (red).

Both the TPAC and FORTIS sensors have been made with splits using high-resistivity wafers with epitaxial layers up to 18 μm thick. The doping levels were such that the epitaxial layer, which corresponds to most of the detecting volume, is fully depleted even with the voltage supply typical of deep sub-micron CMOS processes. The typical resistivity achieved is shown in Figure 2. The performance of these sensors is discussed in Sections 4 and 5.

4 The FORTIS sensors

FORTIS (Four-T Image Sensor) is a prototype sensor containing up to thirteen variants on a four transistor (4T) pixel architecture.

4.1 The 4T pixel architecture

The simplest pixel architecture present in CMOS image sensors is that of the 3T (three transistor) structure as shown in Figure 3. This pixel architecture consists of a diode, a reset transistor, a source follower transistor, and a row select transistor. The operation is as follows; first the diode is reset via the reset transistor, and then charge is collected. After a set "integration" time, the row select transistor is turned on and the signal from the pixel is read out via external readout circuitry. In this particular pixel, the diode is both the charge collection area and the node from which the signal is read within the pixel.

The 4T (four transistor) pixel architecture [7] is also shown in Figure 3. The architecture contains three special elements compared to the 3T architecture; the transfer gate (TX) the floating diffusion node (FD), and a pinned photodiode. When the pinned photodiode is held at a certain voltage called the pinning voltage, the diode becomes fully depleted, allowing for a noiseless transfer. Charge will be collected by the pinned photodiode as long as the transfer gate is closed. When readout is ready to occur, the floating diffusion node is first reset to a value above the pinning voltage, and then the transfer gate is opened, which transfers all of the charge from the pinned photodiode and resets it simultaneously. Charge is therefore collected on the pinned photodiode, but transferred to and read out from the floating diffusion node, leading to separate nodes for these two functions.

There are two key benefits to the 4T pixel architecture due to the separated charge collection and readout nodes. The first is that lower noise operation is achievable via correlated double

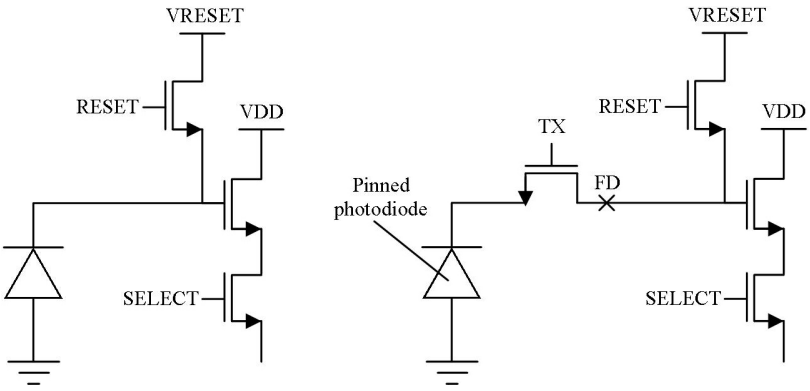

Figure 3: Left: Standard 3T CMOS pixel architecture. Right: Advanced 4T CMOS pixel architecture.

sampling. If a sample is done before and after the transfer gate is opened, the kTC noise, which is the main source of noise within a pixel, can be removed as it is highly correlated.

The second benefit of the 4T pixel architecture is that a high conversion gain can be obtained, which increases the sensitivity of the pixel to small amounts of charge. The conversion gain is given by $V = q/C$. If charge is transferred from the large diode capacitance (with a low conversion gain) to the smaller floating diffusion capacitance (with a higher conversion gain), then the sensitivity to small amounts of charge is increased.

4.2 The FORTIS sensors

There have been two iterations of this sensor; FORTIS 1.0, and FORTIS 1.1, where the latter explored the variants chosen for FORTIS 1.0 further via fabrication with and without the deep P-well layer, and on both standard and high resistivity substrates. FORTIS 1.1 also contains an optimised processing step to reduce the noise associated with the source follower.

FORTIS 1.0 and FORTIS 1.1 are shown in Figures 4 and 5. Both sensors consist of the

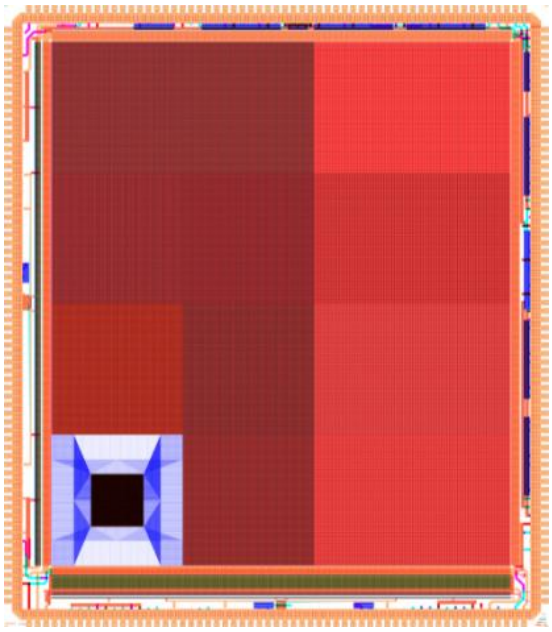

Figure 4: FORTIS 1.0

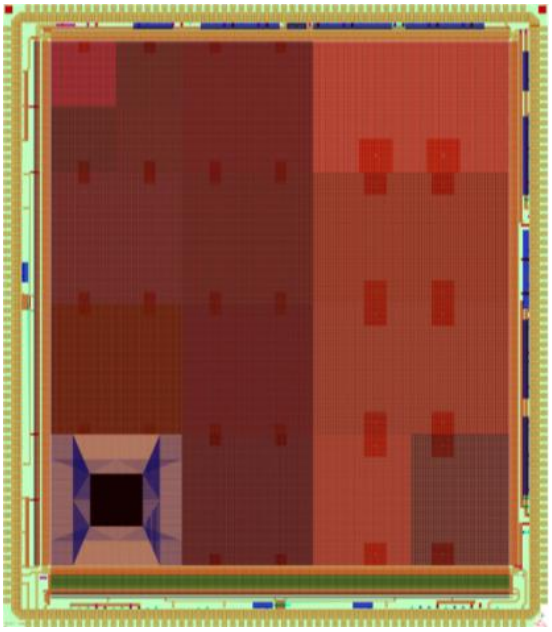

Figure 5: FORTIS 1.1

same simple readout architecture, with decoders for row and column access to focus on one pixel variant array at a time, and a simple analogue output stage with sampling capacitors for storage of the reset and signal samples for correlated double sampling. In FORTIS 1.0, there were twelve different pixel variants, consisting of the original designs plus several geometric variations, such as variations in the size of the source follower transistor, the diode size, and the pixel pitch (6μm, 15μm, 30μm and 45μm). FORTIS 1.1 contains an extra pixel variant where four diodes have been combined at the floating diffusion node.

4.3 Test results

The sensors have been extensively tested: the gain and noise were measured using the Photon Transfer Curve (PTC) technique; a laser scan was performed to measure the charge sharing between the pixels; and finally the sensors were placed in a test beam for a first evaluation of their response to high energy charged particles.

4.3.1 Gain and noise measurements

For the characterisation of the FORTIS sensor, the Photon Transfer Curve (PTC) technique was used. A photon transfer curve is a plot of the dark-corrected signal obtained from an image sensor against the noise for that signal. It is obtained via one of two methods; an intensity sweep, where the integration time is fixed and the light level/temperature is varied, or via an integration sweep, where the light level/temperature is fixed and the integration time is varied. At least two identical images are required for each step to obtain the PTC and the mean signal and variance are taken from these two frames. The subtraction of the two frames to calculate the variance removes fixed pattern noise, leaving only read noise (which is the noise of interest for an image sensor) and shot noise. Shot noise scales with the square root of the signal, giving a characteristic 0.5 gradient when plotted on a log-log plot, and is the basis of the photon transfer curve [8].

Many parameters can be extracted from a photon transfer curve to give the basic characteristics of an image sensor. The noise is taken from the y-intercept of the graph (i.e. the noise for 0 signal). The gain is taken from the x-intercept of the best fit line taken from the plot, which if plotted on a log-log scale, should give the characteristic gradient of 0.5. The linear full well capacity is taken from the peak in the photon transfer curve. This is where the noise begins to reduce as the variation in signal is dampened as no more signal can be collected. The maximum full well capacity is taken as the maximum signal level which is plotted on the graph. If an integration sweep was performed, the dark current can be obtained from the gradient of the dark signal level plotted against the integration time. A result for the PTC [9] from the best pixel variant for FORTIS 1.0 is shown in Figure 6. This pixel had a very low noise of 5.8 e^-, and a high conversion gain of 61.4 $\mu V/e^-$, demonstrating the benefits of the 4T pixel architecture.

4.3.2 Radiation hardness

Three FORTIS 1.0 sensors were irradiated up to 1 Mrad in steps of 10 krad, 20 krad, 50 krad, 100 krad, 200 krad, 500 krad and 1 Mrad, using 50 kV x-rays from an x-ray tube. In between the irradiations, when not being tested, the sensors were stored at $-25\,^{\circ}$C. At each radiation step the noise of the best pixel variant was measured using the PTC technique. Figure 7 shows the noise distributions for one sensor measured before irradiation and after 500 krad, while Figure 8 presents the average noise for each of the three sensors as a function of dose [9]. The sensor is seen to work well up to 500 krad. A logarithmic increase with respect to irradiation level was found between 0–500 krad from 6–9 e^- r.m.s., and the noise distribution clearly spreads out, suggesting that random telegraph signal noise and $1/f$ noise has increased, which are both associated with

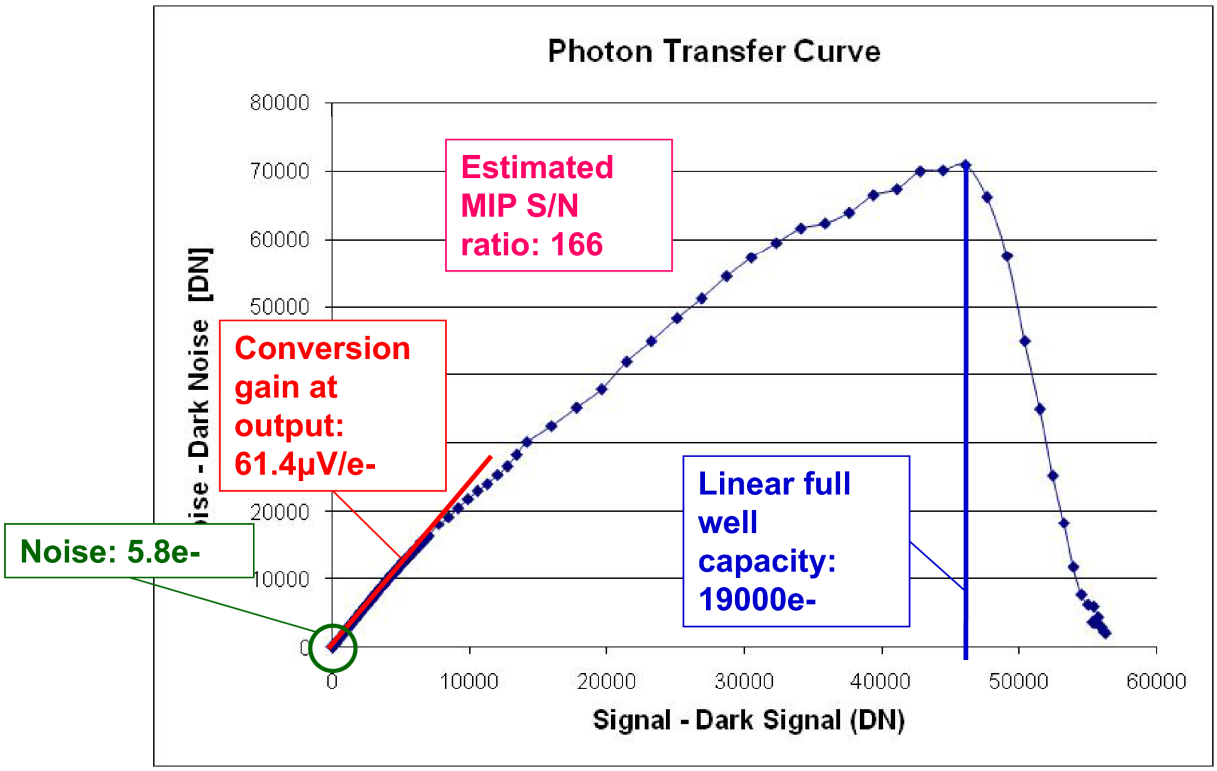

Figure 6: Results from the best pixel of FORTIS 1.0.

charge trapping in the source follower transistor gate oxide and the corresponding silicon-silicon dioxide interface [10].

It was found that the noise significantly increased beyond 500 krad to a point where the signal-to-noise ratio decreased substantially and a MIP would not be reliably detected, therefore the suggested radiation tolerance for FORTIS 1.0 is between 500 krad and 1 Mrad. Note, none of the FORTIS 1.0 sensors were made with high-resistivity epitaxial layers.

4.3.3 Laser scan

When electron-hole pairs are generated by a MIP, the electrons will typically diffuse through the epitaxial layer, and if they are sufficiently close to the depletion region of the diode, they will be collected. In the ideal situation, the entire epitaxial layer underneath the diode would be completely depleted, changing the main charge transport mechanism from diffusion to drift, where the increased electric fields from the larger depletion region attract more charge than in the case of a smaller depletion region. As the depletion region width increases with increasing resistivity of the epitaxial layer, one way to extend the depletion region further into the epitaxial layer and improve the charge collection efficiency is to use an epitaxial layer with a high resistivity[12, 13]. The use of a high resistivity epitaxial layer should also reduce the charge spread as less charge will be diffusion to and get collected by the neighbouring pixels, improving the hit finding efficiency.

FORTIS 1.1 has been fabricated with both a standard (10–100 Ω cm) and a high resistivity epitaxial layer (1–10 kΩ cm). To test the difference in charge collection, a white light source was focused down to a $2 \times 2\,\mu m^2$ spot size and then horizontally scanned across the centre of the diodes of three adjacent pixels. The results are shown in Figures 9 and 10. The peaks and troughs represent the diode and metal within the pixel respectively, and the secondary peaks are

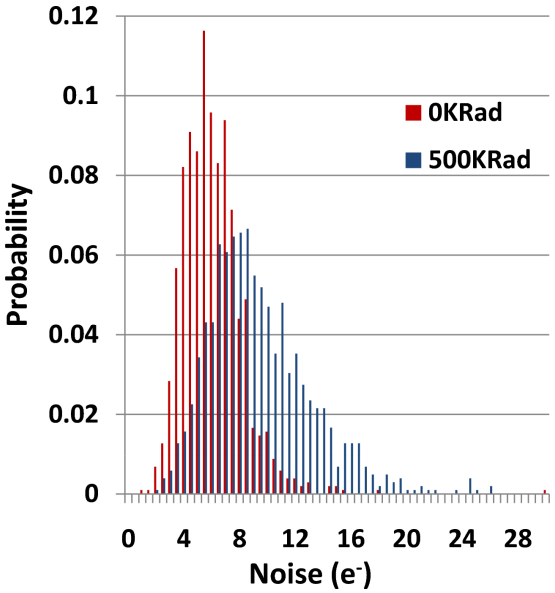

Figure 7: Noise distributions measured before and after irradiation.

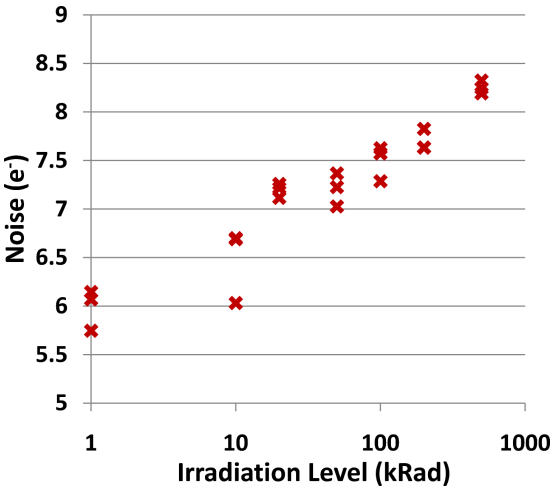

Figure 8: Average noise as a function of irradiated dose, for three FORTIS1.0 sensors.

due to charge being collected by the neighbours. Clearly, the charge collected by the neighbours is significantly lower when using a high resistivity epitaxial layer. The effects on hit finding and position reconstruction are still under investigation.

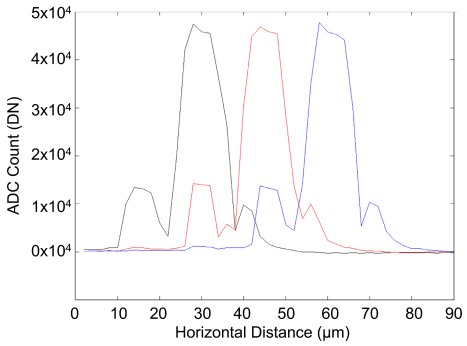

Figure 9: Laser scan using a FORTIS 1.1. with a standard resistivity epitaxial layer.

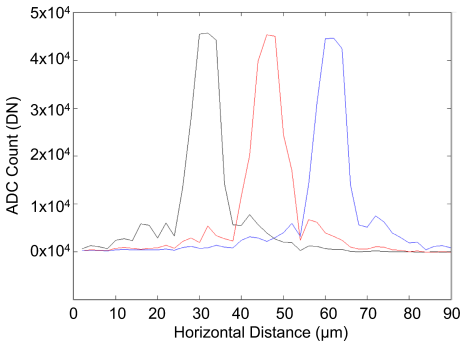

Figure 10: Laser scan using a FORTIS 1.1. with a high resistivity epitaxial layer.

4.3.4 Beam test

During August 2009, the FORTIS sensors were tested at the CERN SPS using a 120 GeV pion beam. Both standard and high resistivity epitaxial layer sensors were tested, as well as sensors with and without deep P-well. The results are currently being analysed. In Figure 11 an event display obtained with a high resistivity FORTIS 1.1 sensor is shown. The plot demonstrates the first detection of MIPs by a 4T architecture. In Figure 12 the pedestal corrected signal for each pixel in each event is shown for a short pedestal run and a larger beam run. This result also demonstrates that particles are clearly observable with the sensors.

In Figures 13 and 14 the cluster signal distribution and the pixel noise distribution are shown. As can be seen there are just a few pixels with very low noise. This particular pixel design (which is not the one with a noise of 5.8 e^-) displays a signal-to-noise ratio of ~50. The

sensor alignment is an ongoing task.

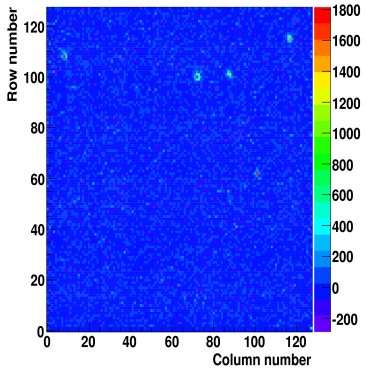

Figure 11: Event display taken with a high resistivity FORTIS 1.1. Five hits can clearly be seen.

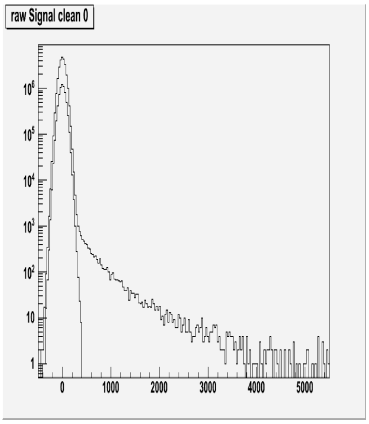

Figure 12: Pedestal corrected signal for each pixel in each event with and without beam.

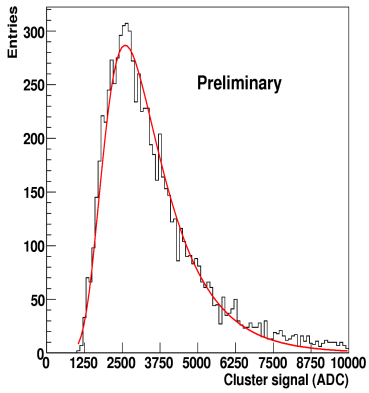

Figure 13: Cluster signal distribution for the high resistivity FORTIS 1.1.

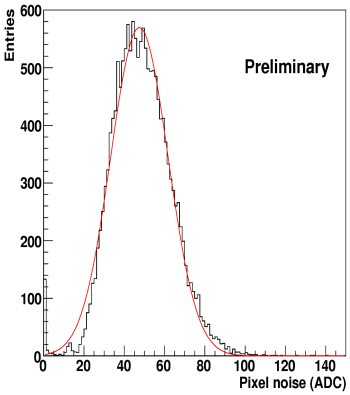

Figure 14: Pixel noise distribution for the high resistivity FORTIS 1.1.

5 The TPAC sensors

The TPAC (Tera-Pixel Active Calorimeter) sensor has been designed by the CALICE-UK groups for studying the issues associated with digital electromagnetic calorimetry. Three sensor iterations have been designed and fabricated, namely TPAC 1.0, 1.1 and 1.2. TPAC 1.2 is the latest submission and its design and functionality will be described below.

5.1 TPAC sensor layout

The TPAC 1.2 sensor comprises 28224 pixels, row control logic, on-sensor SRAM memory banks and I/O circuitry in a $9.7 \times 10.5\,\mathrm{mm}^2$ die. This is shown in Figure 15. The sensor collects the charge deposited by an incident particle in pixels arranged on a $50\,\mu$m pitch. This signal is compared with a global threshold and if a particle is detected, the time-code and location of the event are recorded in memories for readout at a later time. The individual TPAC pixel is based on a conventional analogue front-end for a charge-collecting detector.

Four diodes are connected in parallel to a charge preamplifier, which generates a voltage step output in proportion to the collected charge. A CR-RC shaper circuit generates a pulse in proportion to the input signal with further circuit gain to yield 150 μV/e$^-$ with respect to total collected charge.

The shaper circuit returns to a stable state, depending on the signal size, and is then able to respond to another input signal. Each pixel contains a comparator, which determines whether the shaper signal has exceeded a global threshold with per-pixel trim value adjustment. The output of the comparator generates a fixed length pulse which forms the output from the pixel. A schematic of the in-pixel circuit is shown in Figure 16. The row controller logic samples pixel outputs and stores the location and timestamp of hits in SRAM memories. The row control logic has 19 SRAM registers available for storage of hit data. A memory controller is implemented to organise the use of these registers, such that registers are not overwritten once used, and only those with valid data participate in readout. Each column of SRAM registers is read out in turn and multiplexed to a parallel digital

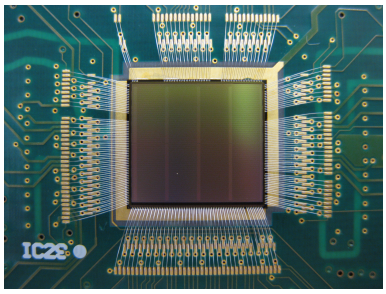

Figure 15: The TPAC 1.2 sensor bonded on its PCB.

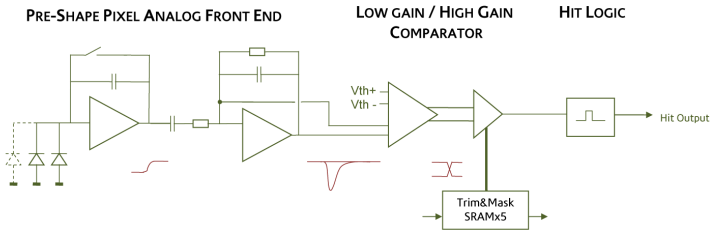

Figure 16: Schematic of the TPAC pixel circuit with pre-amplifier, shaper circuit and comparator.

output. The full TPAC1 sensor comprises 4 columns of row logic, each with 168 rows, hence there are 12,768 SRAM registers of 22 bits each in total. The row control logic and the SRAM register bank occupy a 250 micron wide region adjacent to the 42 pixels (2.1 mm). The logic and SRAM are insensitive to incident particles; therefore this sensor has approximately 11% dead area, which is distributed amongst the pixels in strips. A schematic of the row-controller logic is shown in Figure 17.

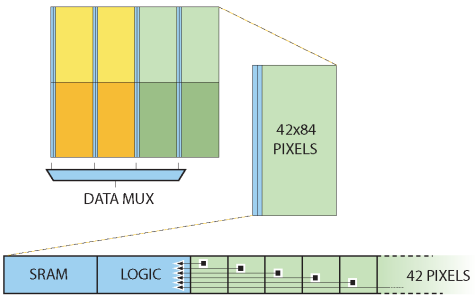

Figure 17: The TPAC row-logic for hit storage and readout.

5.2 Test results

The sensors have been characterised using radioactive sources, lasers and test beams, to provide measurements of absolute noise and gain calibration, and to permit investigations of charge collection/transfer and response uniformity across the sensor.

One important characterisation issue is to measure the pedestal and noise values for each pixel, such that a per-pixel trim setting can be established. This ensures that all pixels have pedestals within a single narrow range so that the noise hit rate above threshold is uniform across the whole sensor. The absolute calibration and gain uniformity are also critical parameters for an understanding of the optimal threshold level to use for high MIP efficiency.

5.2.1 Pedestal uniformity

Threshold scans are carried out for each of the 28224 pixels. Using an iterative procedure, the trim values are optimised for uniformity of thresholds. The measurements of pedestal means and r.m.s., before and after the trimming procedure, are shown for a typical sensor in Figure 18, illustrating the excellent pedestal uniformity achieved. Note that the trim correction is always an upwards adjustment to the threshold value, as clear from the Figure 18.

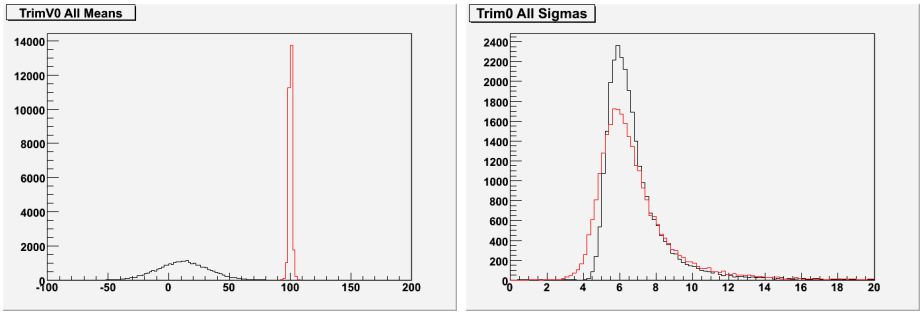

Figure 18: Example of the distribution of mean pedestal values (left) and the corresponding r.m.s. values. Values before trimming (black) and after trimming (red) are shown, in arbitrary threshold units.

5.2.2 X-rays

Photons from ^{55}Fe sources deposit approximately 5.9 keV of energy (corresponding to 1620 e^-) at random locations within the pixel volume. This energy is similar to that deposited by a MIP passing through a 20 μm depth of silicon and provides an absolute gain calibration via a characteristic photopeak, assuming all of the energy is collected by a single pixel. In general, the initially deposited charge will diffuse and be shared between collecting diodes of more than one pixel, smearing out the otherwise distinctive peak. Charge collection inefficiency can also contribute to this effect.

Very occasionally, the energy will be deposited in the vicinity of the depletion region of a single diode within a pixel. In these cases, the full charge will be collected and a clear (but small) peak observed, as shown in Figure 19, using one of the analogue test pixels. The position and width of the primary peak give preliminary measurements of the calibrated gain and noise of 128 $\mu V/e^-$ and 27 e^-, respectively.

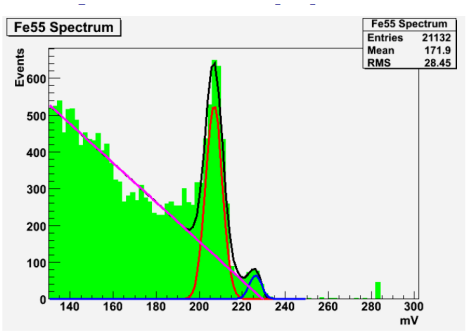

Figure 19: Example of ^{55}Fe photopeak in TPAC sensor, see text for details.

5.2.3 Lasers

For laser light to produce ionisation within the epitaxial layer itself, it is necessary to illuminate the sensor substrate to avoid obstructions from the metal layers on the front face. An infra-red wavelength of 1064 nm is used to penetrate the ~500 μm P-substrate. Two types of measurements are made: charge collection efficiency and time across an individual sensor (using analogue test pixels, surrounded by dummy pixels), and pixel gain uniformity (using the 28224 pixel array). The latter shows uniform gain response, with a spread of 12%, while the former shows good agreement with TCAD simulations and the very substantial benefits of the deep P-well design. Figure 20 shows the charge collection fraction as a function of position along a 50 μm section through a TPAC pixel for four different cases: sensors with deep P-well implants, for both measurements ("Real+DPW") and TCAD simulations ("GDS+DPW"), and corresponding results for sensors without the deep P-well implants ("GDS-DPW" and "Real-DPW"). The simulation is in good agreement with the data and illustrates the substantial improvement in efficiency due to the deep P-well.

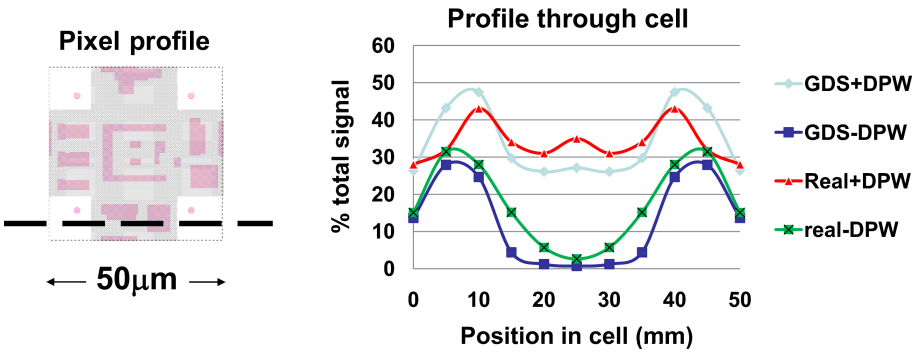

Figure 20: Charge collection efficiency across an analogue TPAC test pixel. The dashed line shows the section of the pixel along which the efficiency measurements are plotted, for variants with and without deep P-well implants, together with corresponding TCAD (GDS) simulations.

5.2.4 Test beam

The TPAC 1.2 sensors were also studied in the same test beam run as the FORTIS sensors, as described in Section 4.3.4 with a primary goal of measuring their efficiency for detection of MIPs. The experimental configuration consisted of six sensors: two sensors under test, separated by ~ 25 mm in the beam direction, and a further four standard deep P-well TPAC sensors acting

as a telescope, located at $\sim \pm 12\,\mathrm{mm}$ and $\sim \pm 18\,\mathrm{mm}$ from the test sensors. A beam signal was provided by means of the triple coincidence of two small scintillators upstream and one downstream of the TPAC sensors. Tracks formed from high energy pions in the four telescope detectors were were used to identify regions of interest in the test sensors and from these an efficiency was extracted as a function of distance relative to the interpolated track crossing position. Both the standard deep P-well sensor and the variant with high resistivity epitaxial layer were used in the tests.

In deriving the intrinsic performance of the pixels to MIPS, several well-understood design artefacts which contribute to inefficiency are taken into account, specifically: geometrical inefficiencies in the sensors (memory, control logic); a small fraction of noisy pixels which have been masked out; and potential saturation of the limited 19 SRAM register available to store hits within a group of 42 pixels during an 8000 timestamp bunchtrain. The efficiency for the pixel which the particle passed through to give a hit was calculated for both sensor types tested as a function of the global threshold and preliminary results are shown in Figure 21.

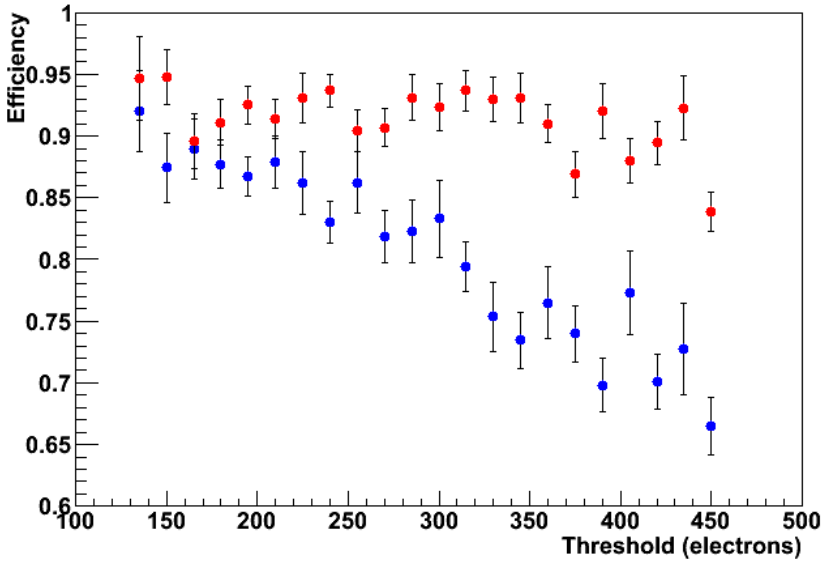

Figure 21: MIP efficiency for TPAC sensors as derived from high energy pion test beam in August 2009. High resistivity (red) and standard deep P-well (blue) sensors are compared as function of threshold applied.

These first results from the test beam run indicate an encouragingly high MIP efficiency is possible for both the standard and high resistivity deep P-well alternatives.

6 Future plans

After the evaluation of the FORTIS and TPAC devices, SPiDeR plans to work on three further sensors, the CHERWELL sensors (two iterations) and a sensor for the DECAL. The Collaboration also plans to continue our test beam efforts and explore the radiation hardness of the existing TPAC and FORTIS devices.

6.1 The CHERWELL sensors

The overall aim of designing the CHERWELL devices is to produce a sensor with low power, low noise and no inactive area. It particularly builds on the experience gained from the FORTIS sensor, and is aimed at improving aspects of previous sensor architectures. Compared to the TPAC design it will have lower power and noise because it is based on a rolling shutter architecture and uses double correlated sampling and a 4T front-end. There will also be no inactive area as the control and readout electronics is distributed over the active area. The trade-off is that it will have poorer timing resolution but this would be adequate for CLIC, where the bunch trains are very short and a first study has shown that the pixel size can be reduced to $\sim 25\,\mu m$ which increase granularity and allow to cope with higher beam backgrounds. For CHERWELL, the aim is to distribute the readout and memory over the active area, minimising the dead area.

6.1.1 The CHERWELL architecture

The 4T architecture with rolling shutter readout has been pioneered by the FORTIS (see Section 4) test sensor, funded by the RAL Centre for Instrumentation. The slower readout will potentially give an order of magnitude reduction in power compared to the TPAC architecture. The basic electronics structure will include a Correlated Double Sampling (CDS) circuit and a trimming facility for the comparator. The mode of operation of the CDS circuit is that the voltage output is sensed twice in quick succession before and after transferring the signal charge to the output gate using the TX transfer transistor. The memory buffer is 14 bits wide: 5 bits for the timestamp information and 9 bits to encode the location within the row. The proposal is to divide a column into short 128 cell strixels, shortening the readout time by a factor of 10.

For example, for the ILC, within a 1 ms bunch train, there would be at least ten slices, i.e. ten complete readouts of the sensor. For an individual readout cycle of the sensor a duration of 200 ns is foreseen. To match the requirements for ten time slices, the possibility of multiple rolling shutters per strixel will be explored. Future linear colliders with superconducting cavities all have a duty cycle of 1 %, where the bunch trains with an average length of 1 ms are followed by 199 ms of quiet time. Most studies therefore plan to power off most of the detectors during this time, a feature called power-pulsing. CHERWELL will support power pulsing, implying the switch-off of the electronics during the 199 ms quiet time. The analogue information will then be processed at the end of the strixel (see Figure 22) and it can be read out using either a comparator or a purely analogue readout.

For further processing the analogue information then needs to be digitised off-sensor. In terms of reducing the dead area of the design, the intention is to embed the electronics within the pixels themselves as is shown in Figure 23. This requires the use of deep P-wells and so the INMAPS process will be used. The amount of dead area within a strixel is effectively reduced to zero using this approach. The critical integration of the 4T process with a deep P-well implant for the embedded electronics has already been demonstrated with the FORTIS sensor. Another benefit of this approach is to reduce the amount of minimum feature size capacitors and resistors, which will lead to better matching and less spread between individual strixels.

6.1.2 CHERWELL schedule and plans

The Collaboration plan to submit the first iteration of CHERWELL (CHERWELL1) in spring of 2010. This will be a proof-of-principle device with 5x5 mm size which which will exploit a subset of the planed features for CHERWELL2. It will also be used to guide the technology decision for the DECAL sensor (see Section 6.2.2).

The second iteration of CHERWELL (CHERWELL2) will the include all the features of CHERWELL1. CHERWELL2 will be using two $25\,\mathrm{mm}^2$ seats on a 180 nm multi-project run,

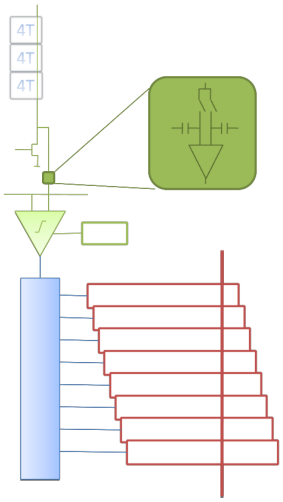

Figure 22: The CHERWELL strixel with the shared readout electronics at the end of the row.

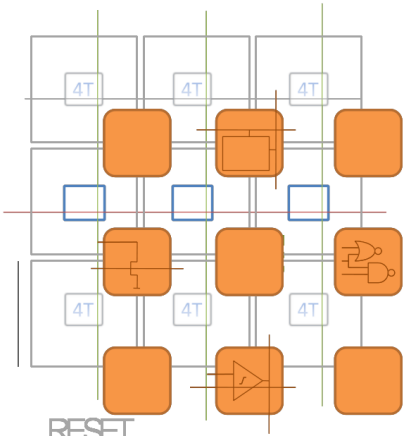

Figure 23: The CHERWELL island approach to embed electronics

with a geometry of $10 \times 5\,\mathrm{mm}^2$. Its basic pixel size will be $25 \times 25\,\mu$m and have 128 pixels forming a strixel. It will already include the embedded electronics and will feature binary readout and a purely analogue readout. The data will be realised as a 14-bit wide parallel bus, and the purely analogue data will be digitised using ADCs on the sensor mounting board. The goal is to submit this device around the beginning of 2012.

6.2 The DECAL sensor

SPiDeR aims to design a sensor which will be able to measure a realistic energy resolution in a functioning, full-depth, electromagnetic calorimeter (ECAL). This sensor will have digital (binary) readout, hence it is called the digital ECAL (DECAL) sensor, and will be used to construct a sampling calorimeter with alternating tungsten converter and silicon sensor layers in a stack. This sensor is planned as a first application of the SPiDeR CMOS technology to build a detector for scientific measurements.

This work is being done in association with the CALICE Collaboration and the motivation for, and expected performance of, a digital ECAL is discussed within the CALICE submission to this PRC meeting [14].

6.2.1 Sensor and stack requirements

The sensor needs to be highly granular and a pixel size of $50 \times 50\,\mu\mathrm{m}^2$ is assumed. The pixels also need to be efficient for detecting single MIPs; this means any sensor will need to use the deep P-well implant (developed by members of the Collaboration, see Section 3.2) and hence will use the INMAPS process.

To get a realistic ECAL resolution, the active layers will need to be wide enough to contain electromagnetic showers. The scale is set by the shower width, where full containment requires several times the Molière radius (which for tungsten is 9 mm), and by any beam spread when operating the stack in a beam test. The latter area can be controlled by the size of the trigger used, at the cost of beam rate. Experience with previous beam tests indicate an area per layer of at least $6 \times 6\,\mathrm{cm}^2$ will be needed, either with one large sensor or several smaller sensors tiling the layer.

Enough sensors will also need to be produced to instrument the stack in depth. A typical linear collider ECAL design has of order 30 sensitive layers spread through a total tungsten

depth of order $24\,X_0$ so this is gives some indication of the numbers needed. With a single large sensor, this would clearly require 30 fully functional sensors. For smaller sensors, then to avoid gaps in the critical central core of the electromagnetic showers, a tiling pattern of at least 3×3 sensors per layer would be needed, resulting in a total of 270 working sensors. In either case, each layer will have over one million pixels. The actual number of layers produced may be limited by financial or yield constraints but the target is currently for 30 layers. The production, testing and assembly of this number of layers, particularly for the small sensor option, will be a significant task and a large fraction of the effort on SPiDeR has been allocated to this in 2011 and 2012.

6.2.2 Technology choices

The choice of a single large sensor or for nine smaller sensors per layer will depend on the technology chosen for the DECAL sensor. The TPAC pixel design has been demonstrated to work well; see Section 5. However, one of the limiting factors in this design is the power distribution to the pixels over the sensor area. Given the current CMOS process used, it is unlikely that this would scale up beyond another factor of two in each dimension without causing significant voltage droop when pixels far from the sensor edge register hits. This would limit a TPAC-like DECAL sensor to the standard CMOS reticle limit of around $2 \times 2\,\mathrm{cm}^2$ and so would require nine per layer. This raises issues of dead space between the sensors. For shower reconstruction, it is better to distribute dead area as uniformly as possible so as to affect all showers equally; the resolution then degrades statistically as $\sqrt{N}$, due to the lower number of particles observed. The design will investigate moving I/O pads away from the periphery of the sensor and so allow active pixels to be placed within a few $100\,\mu$m of the sensor edge. Wirebonds could also leave large gaps between the sensors; this could be overcome using bump bonding but a simpler solution would be to bond through holes cut in the PCB, as shown in Figure 24. Note, for either interconnect solution, the substrate side of the sensor is not in contact with the PCB. However, the TPAC sensor performance has been shown to be unaffected by an explicit substrate ground so this is not an issue. The TPAC option also consumes a reasonably high power load and a DECAL stack made with such sensors could generate of order several 100 W. This would require a cooling system, complicating the overall stack mechanical design.

In contrast, the FORTIS 4T pixel design results look very promising, see Section 4, but the design is newer and some further validation would be needed before committing to using this for the DECAL sensor. The first CHERWELL sensor will therefore in part act as a study sensor for the DECAL 4T application. The main advantage of a 4T design would be that a larger sensor could be made; using stitching, then a sensor up to the required $6 \times 6\,\mathrm{cm}^2$ should be feasible. A single sensor would simplify testing and assembly and reduce the dead area within the fiducial region to effectively zero. A 4T design would also be likely to be lower power than the TPAC option. However, such a DECAL sensor would have rolling shutter readout and so would not be applicable to an ILC-like beam timing structure. It would however serve as a possible design for CLIC-like beam timing, where the bunches within a train are too close together to resolve. In this application, the full rolling shutter readout would need to complete before the next bunch train, which means within of order 10 ms, which should be feasible.

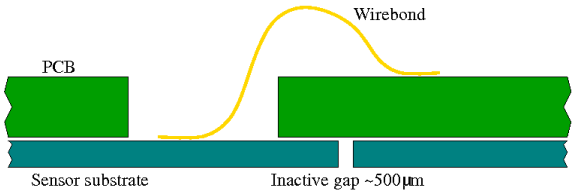

Figure 24: Conceptual diagram of wirebonding through holes in the PCB to minimise sensor gaps.

The primary goal of the DECAL task is to verify the feasibility of the digital ECAL by producing a proof-of-principle detector. As such, it is an application of the SPiDeR technology rather than a sensor for technology development itself. Hence, the sensor design will be relatively conservative and the choice of which design to use will be made to minimise the risk.

6.2.3 DECAL schedule and plans

The decision on the TPAC or 4T design for the DECAL sensor will be made in 2010, when results from CHERWELL are available. The DECAL sensors will then be fabricated in 2011, following which the sensors will be tested for functionality. This will include detailed studies with laser and ^{55}Fe sources. These tests will continue for some time but the basic proof of performance should be achieved within around three months. Following this, then the production testing and assembly of the sensors and stack layers and the commissioning of the completed stack are assumed to take around eight months. The stack will then be exposed to beam in 2012. The beam programme will entail a wide range of electron and pion energies, from around 1 to 100 GeV. Such a programme will take around four to six weeks of data-taking in total, potentially in two or three shorter periods.

6.3 Test beam and irradiation plans

Following the successful characterisation of sensors, it is important to test them in test beams and also evaluate their radiation hardness. SPiDeR plans to have a test beam at DESY for February 2010 using the 6 GeV electrons to study electron showers in TPAC 1.2. For CHERWELL we are planning to use the CERN SPS test beam for pions and electrons. Funding constraints prevent us from using the Fermilab test beam area as an alternative. For both CHERWELL devices, the EUDET telescope infrastructure will be used. For the DECAL stack, a longer test beam campaign of around six weeks is envisaged at CERN and DESY using electrons up to 100 GeV to establish the principle of digital electromagnetic calorimetry.

After successful characterisation, devices will also be irradiated by various sources. Standardly, CMOS sensors rely on diffusion to collect the charge, there being no significant potential difference to accelerate the charge towards the collection diodes. Due to the random motion and low velocity of the signal charge, trapping may become a significant problem at even relatively low radiation doses. The use of high-resistivity epitaxial layers may help in this respect. Another damage mechanism occurs when the charged particles generate electron-hole pairs in the oxide of the transistors. The hole mobility in the oxide is very small leading to the charging up of the oxide and hence shifts in the flatband voltage. It also leads to the creation of leakage paths, in a decrease in carrier mobility in the channel and an increase in the flicker noise. This affects the sensor operation. The dose dependence of these effects depends on the feature size of the CMOS technology. These tests are very important for the further developments in sensor technology in general.

The three future SPiDeR sensors will be irradiated with photons from ^{60}Co, with neutrons and with protons. The irradiation with ^{60}Co only affects the electronics of the sensor and does not damage the bulk. The proton irradiation yields both damage to the electronics and bulk damage, while the neutron irradiation only does bulk damage. The combination of the three irradiations will allow the Non-Ionising Energy Loss (NIEL) damage to be disentangled from the other damage. The dose range is determined by the maximum dose expected both the ILC and at CLIC. At ILC the innermost sensors at 15 mm radius receive a dose of about 100 krad for the entire lifetime of the ILC. At CLIC this increases to around 100 krad/year.

To cover this range, the sensors will by irradiated with ^{60}Co in several steps up to 1000 krad. To study the bulk damage, the SPiDeR sensors will be irradiated using neutrons and protons. The neutron irradiation will be done in Ljubljana. The proton irradiation could be done at

CERN or in Birmingham. The expected doses at both ILC and CLIC for NIEL are quite small around 10^9–10^{10} n/cm^2. However, the radiation dose scale needs to be set keeping other applications and the bulk damage simulation in mind. Therefore, the chosen irradiation doses will be varied in steps up to 10^{14} p/cm^2. The Birmingham cyclotron is an especially attractive and economical option for irradiation studies as an in-house facility. The 38 MeV protons available there will induce twice as much bulk damage compared with the usual standard of 1 MeV neutrons. An initial comparison of damage effects caused by these protons and neutrons will allow us to certify the cyclotron as irradiation facility. All of the sensors will be characterised thoroughly before and after each step in irradiation. This will not only provide information on the radiation hardness of the sensors, but also on the understanding of the radiation damage models, which is important for future sensor developments in general. The Collaboration plans to irradiate the TPAC and FORTIS sensors in spring 2010, the CHERWELL1 device in 2011 and the DECAL and CHERWELL2 sensors in 2012.

7 Summary

SPiDeR is a recently formed collaboration which will develop generic pixel technologies for particle detectors. It has been approved and should have funding released in April 2010 to cover the following three years. It builds on a long established UK role in the major ILC projects LCFI and CALICE, and on world-leading expertise in CMOS sensors within the microelectronics group at RAL.

SPiDeR will develop CMOS MAPS sensors to study the issues of low cost, noise and power. The CHERWELL family of sensors will be "technology development" sensors but could have applications in tracking detectors at a future linear collider. The DECAL sensor will be used to construct a prototype calorimeter and provide a first demonstration of the potential of digital electromagnetic calorimetry.

References

[1] `https://heplnm061.pp.rl.ac.uk/display/spider/Home`.

[2] ILD Letter of Intent, `http://www.ilcild.org/documents/ild-letter-of-intent/LOI.pdf/at_download/file`.

[3] SiD Letter of Intent, `http://silicondetector.org/download/attachments/46170132/SiliconDetectorLetterOfIntent.pdf?version=1`.

[4] R. Turchetta *et al.*, "A monolithic active pixel sensor for charged particle tracking and imaging using standard VLSI CMOS technology", Nucl. Inst. Meth. **A 458** (2001) 677-689.

[5] G. Villani, R. Turchetta and M. Tyndel, "Analysis and simulation of charge collection in Monolithic Active Pixel Sensors (MAPS)", Nucl. Phys. Proceedings Supplements, **B 125** (2003) 184-188.

[6] R. Turchetta, "CMOS Monolithic Active Pixel Sensors (MAPS) for scientific applications: Some notes about radiation hardness", Nucl. Inst. Meth. **A 583** (2007) 131-133.

[7] R.M. Guidash *et al.*, "A 0.6m CMOS Pinned Photodiode Color Imager Technology", Technical Digest of the IEEE Electron Device Meeting (1997) 927-929.

[8] J.R. Janesick, "Photon Transfer: DN $\rightarrow \lambda$", SPIE Press (2007).

[9] R. Coath *et al.*, "Advanced Pixel Architectures for Scientific Image Sensors", presented at TWEPP '09, Paris, France, September 2009 and to be published in the proceedings thereof.

[10] X. Wang *et al.*, "Random Telegraph Signal in CMOS Image Sensor Pixels", in Technical Digest of the IEEE International Electron Devices Meeting, IEDM'06, San Francisco, USA (2007) 1-4,

[11] J. A. Ballin *et al.*, "Monolithic Active Pixel Sensors (MAPS) in a quadruple well technology for nearly 100% fill factor and full CMOS pixels,", Sensors **8** (2008) 5336.

[12] O.V. Kononchuk *et al.*, "High Resistivity Silicon Wafer with Thick Epitaxial Layer and Method of Producing Same", US Patent Application 10/008,440, December 2001.

[13] W. Chen *et al.*, "Active Pixel Sensors on High-Resistivity Silicon and their Readout", IEEE Trans. Nucl. Sci. **49(3)** (2002) 10061011.

[14] The CALICE Collaboration, "Report to the DESY PRC", Oct 2009.