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# CALICE OVERVIEW

# Themes

- ⦿ Hardware
  - MAPS
  - DAQ
  - Glue/Mechanics
- ⦿ Physics
  - Ongoing studies
  - Eagerly anticipated results and upcoming conferences
- ⦿ Future
  - DevDet etc.

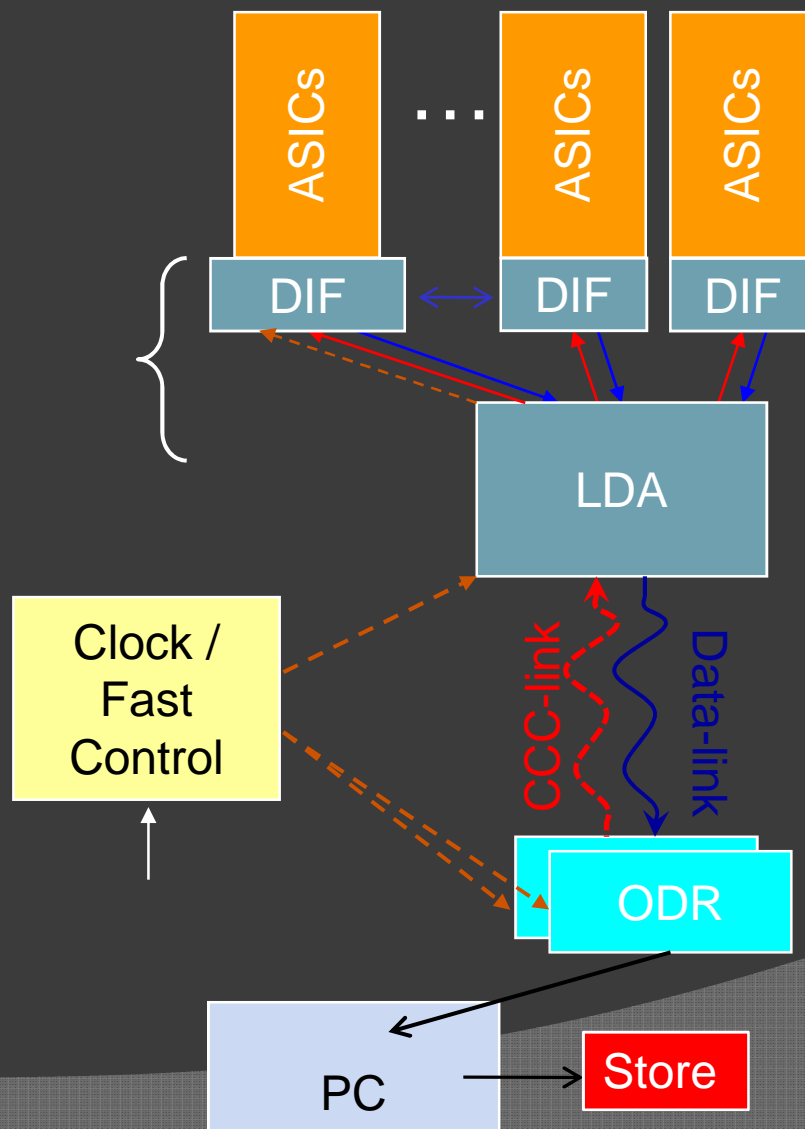
# MAPS

- ◉ Selected highlights...
  - [Anne-Marie](#)

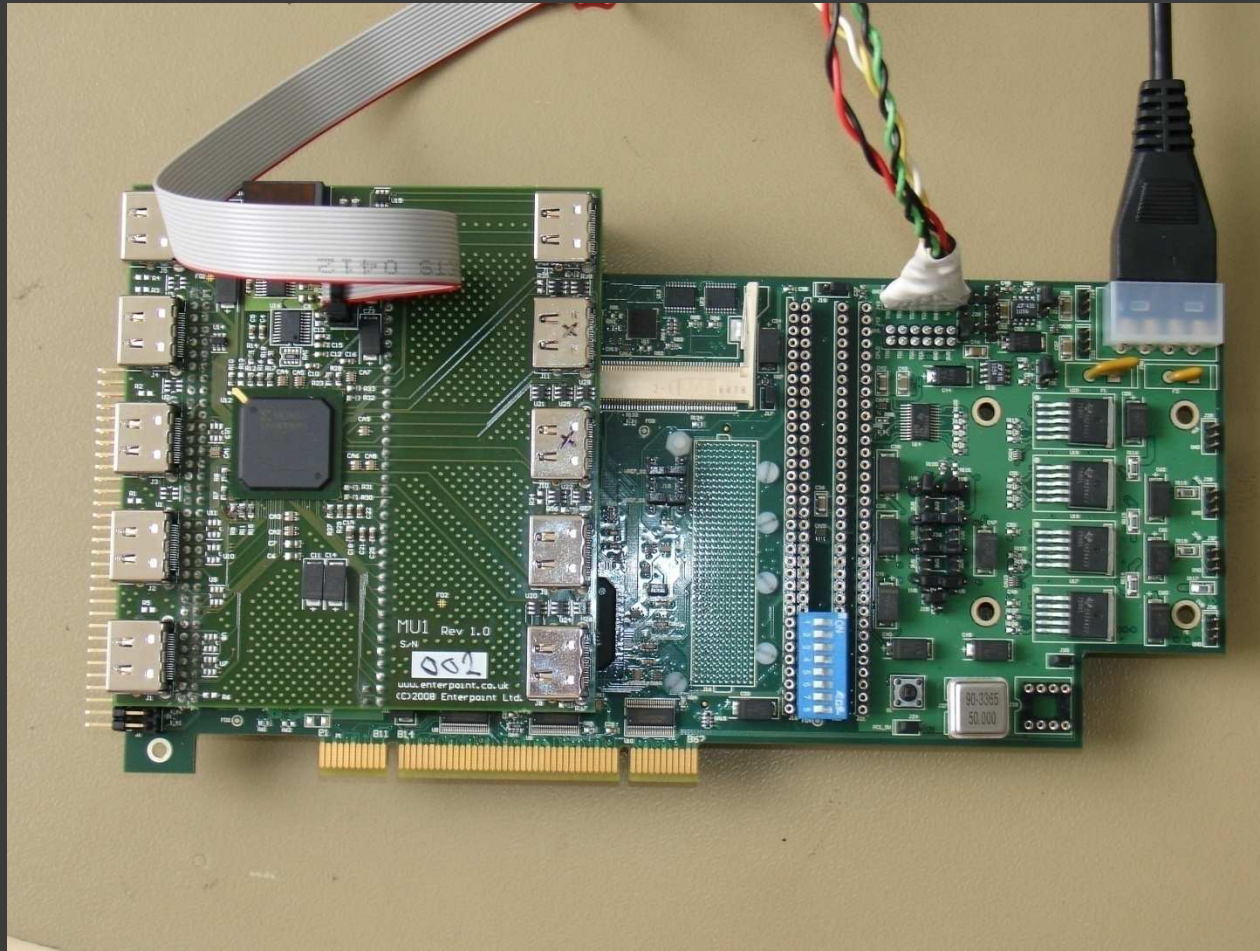
# DAQ

- ⦿ Hardware
  - Marc
  - Maurice/Bart
- ⦿ Software
  - Valeria & Tau

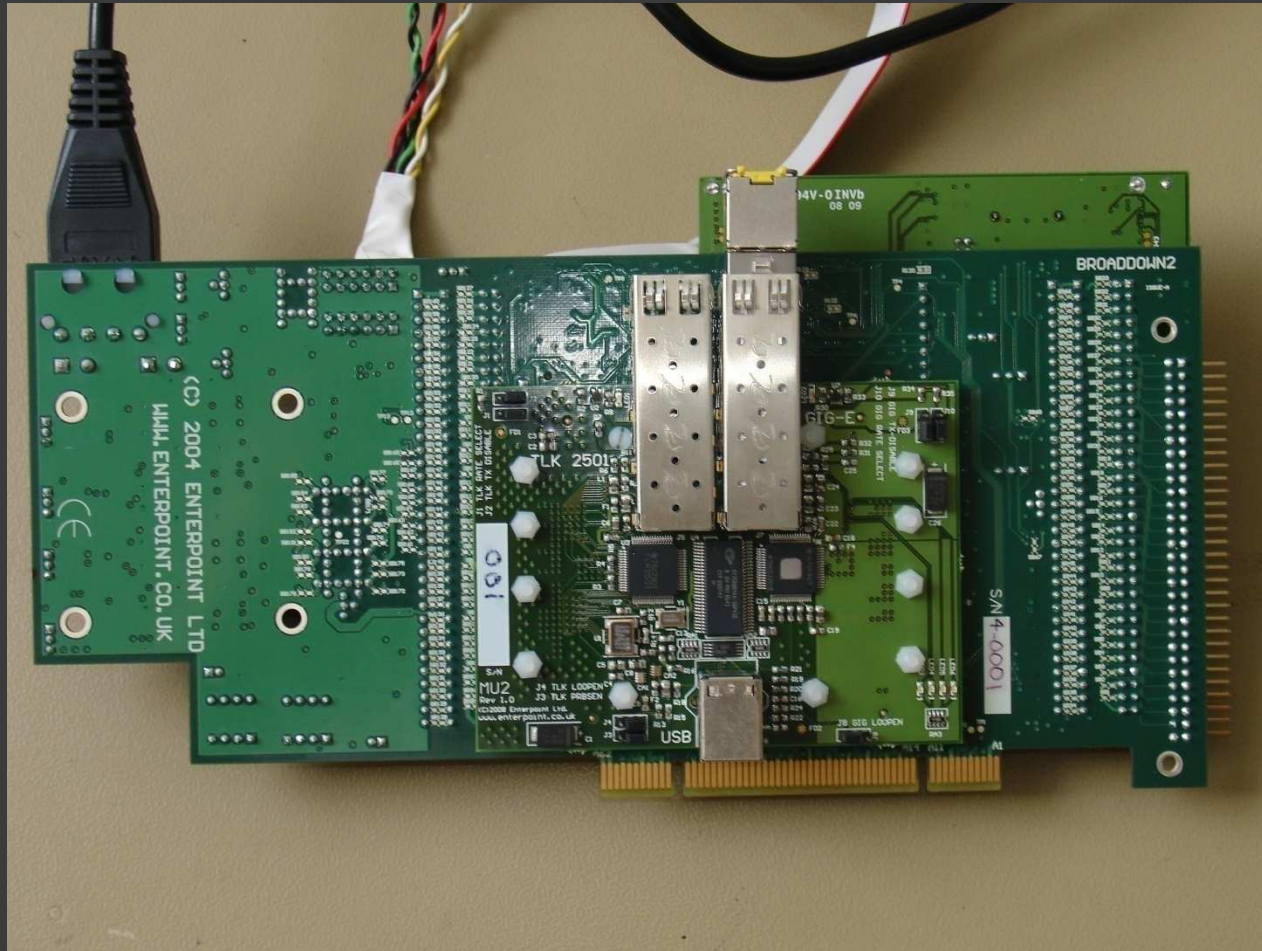
# DAQ Architecture



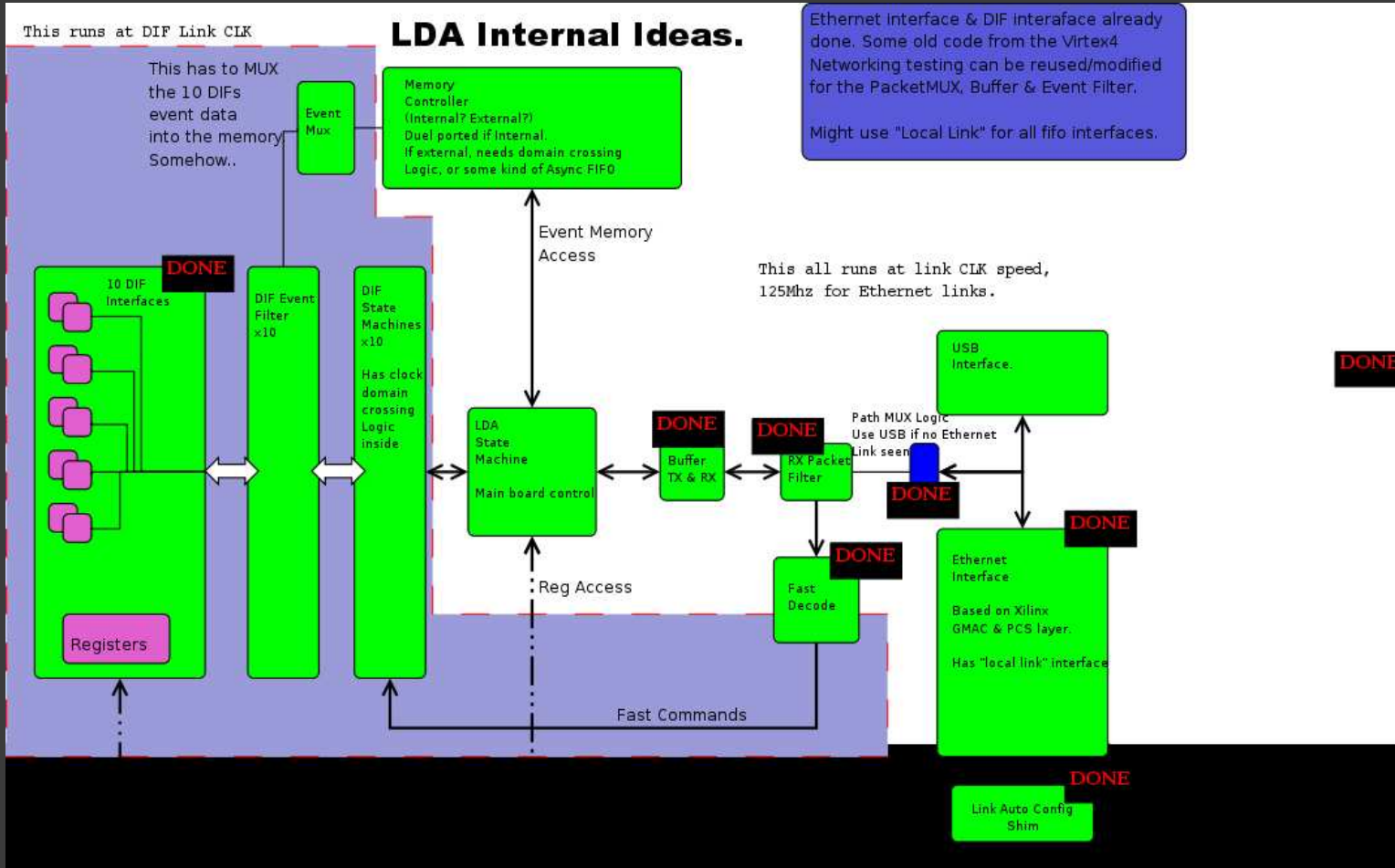
# LDA Hardware Delivered



# LDA Hardware



# Firmware



Ethernet interface & DIF interface already done. Some old code from the Virtex4 Networking testing can be reused/modified for the PacketMUX, Buffer & Event Filter.

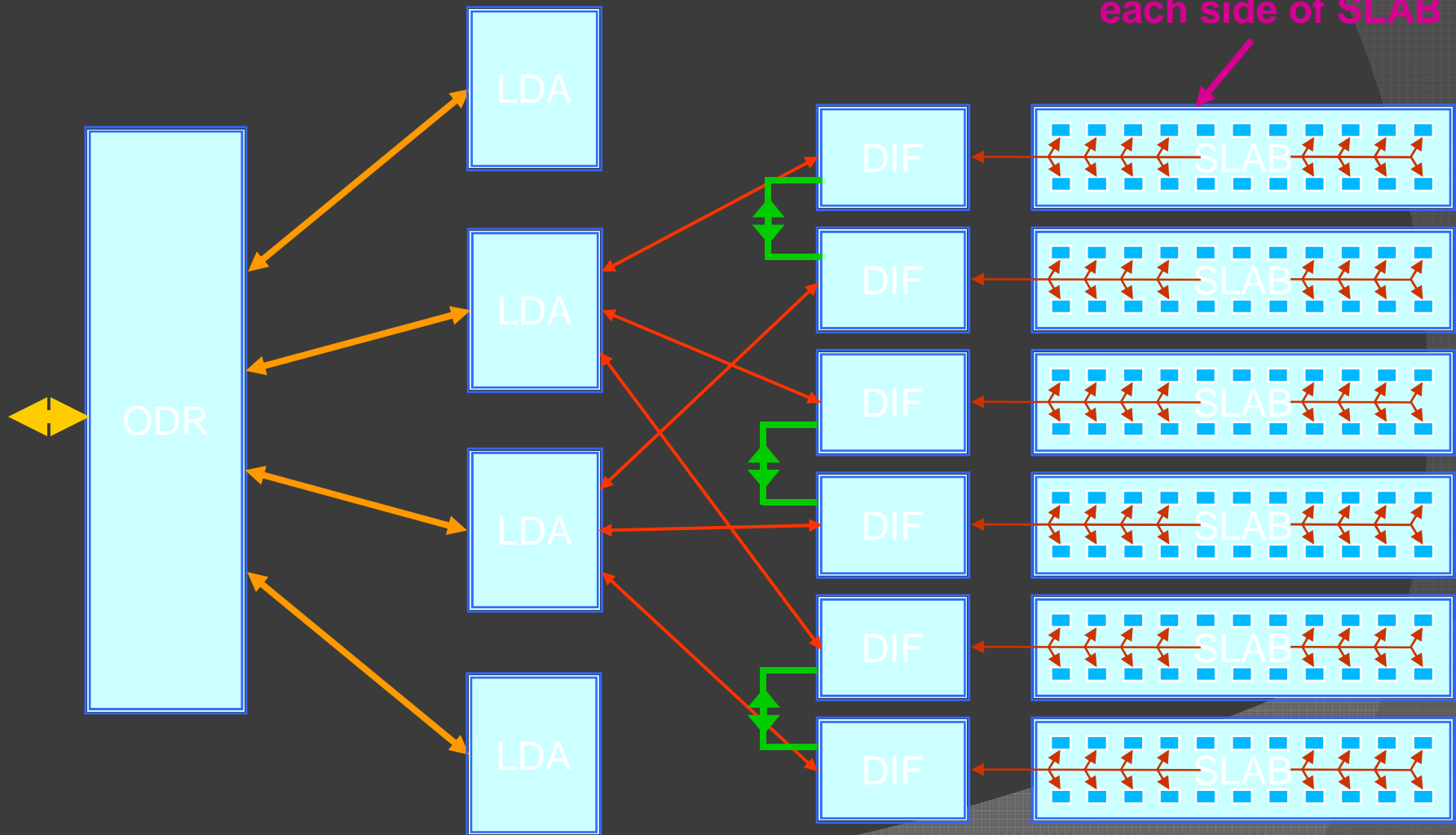
Might use "Local Link" for all fifo interfaces.



# ECAL SLAB Interconnect

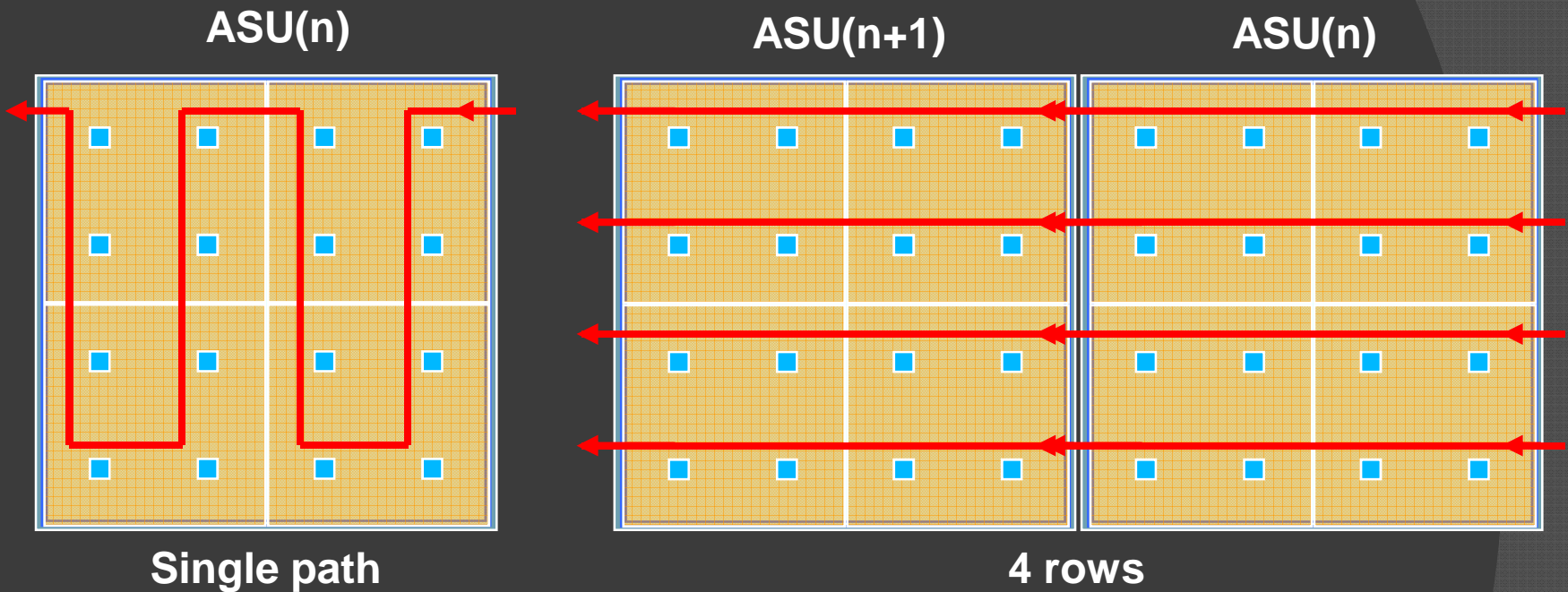
## DAQ Architecture - Overall view

~150 VFE ASICs on each side of SLAB



# ECAL SLAB Interconnect – Why Multi-Rows?

How to read them out – **single path** or in **4 rows**?



Per ASU: L ~ 720mm, C ~ 72pF

Per ASU: L ~ 180mm, C ~ 18pF

Per Slab of 9 ASUs:  
L ~ 6.5m, C ~ 650pF

Per Slab of 9 ASUs:  
L ~ 1.6m, C ~ 160pF

Do these look **BIG ??**

## ECAL SLAB Interconnect

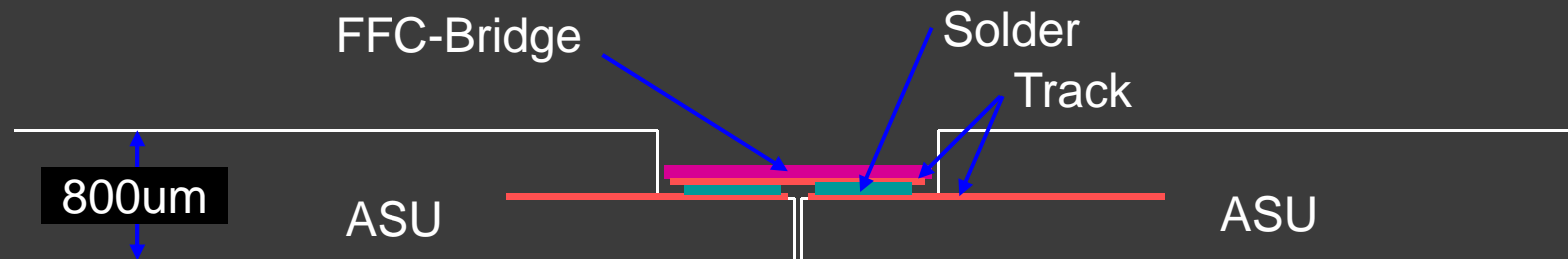
We have been looking at using “Bridges” to jumper multiple connections between adjacent ASUs

The Bridge would be soldered onto pads on the ASU (or DIF) PCB

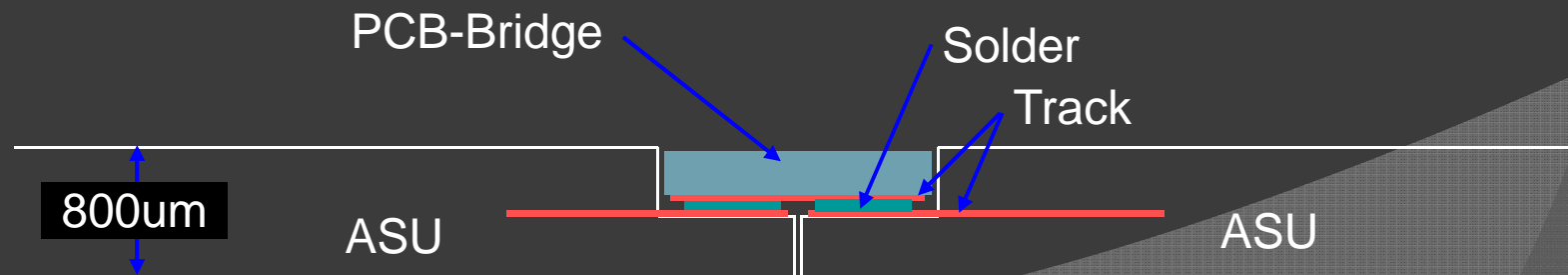
Each Bridge would provide 30-40 connections  
Up to 4 Bridges fit in the width of an ASU  
... 1 per path would be an ideal solution JJ

## ECAL SLAB Interconnect

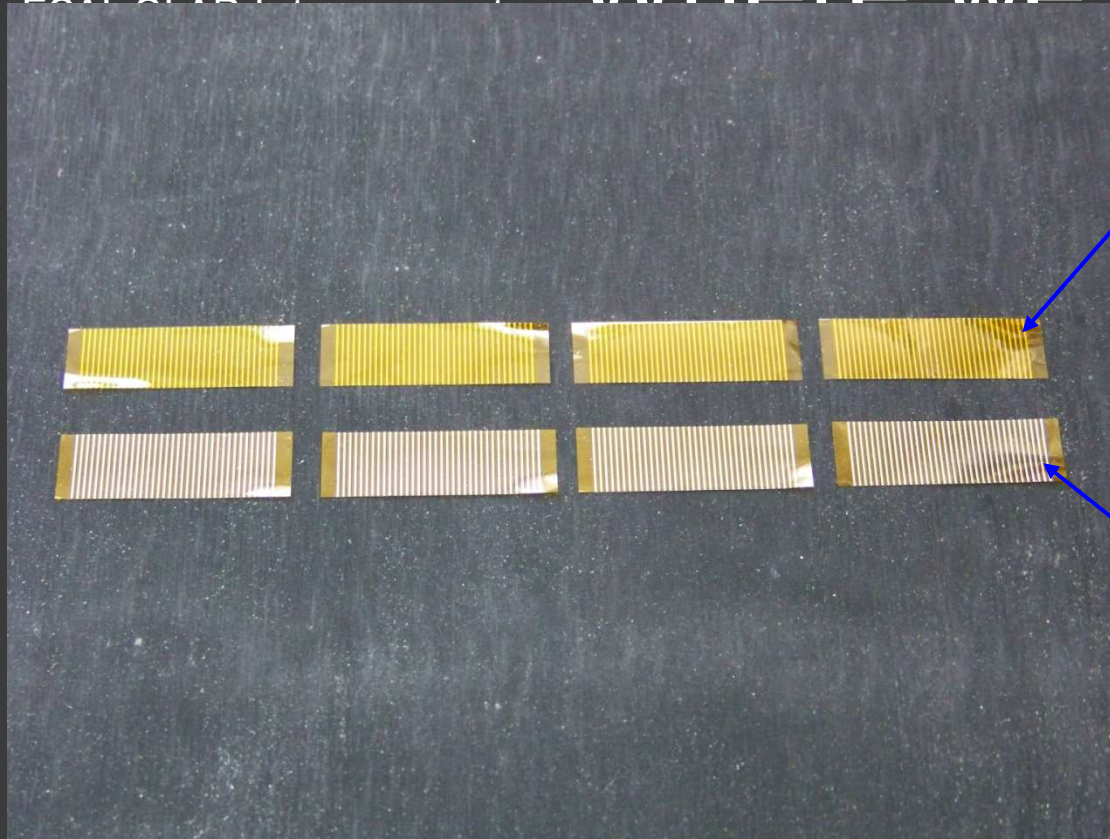
Short FFC (Flat, Flexible-Cable) Bridges make connections on a 1mm pitch – OK for at least 120 connections



Alternatively the Bridges can be thin PCBs, also with 1mm pitch connections. This gives a mechanical as well as electrical joint



# Where we



Top View

Thin traces on  
Kapton backing

Under View

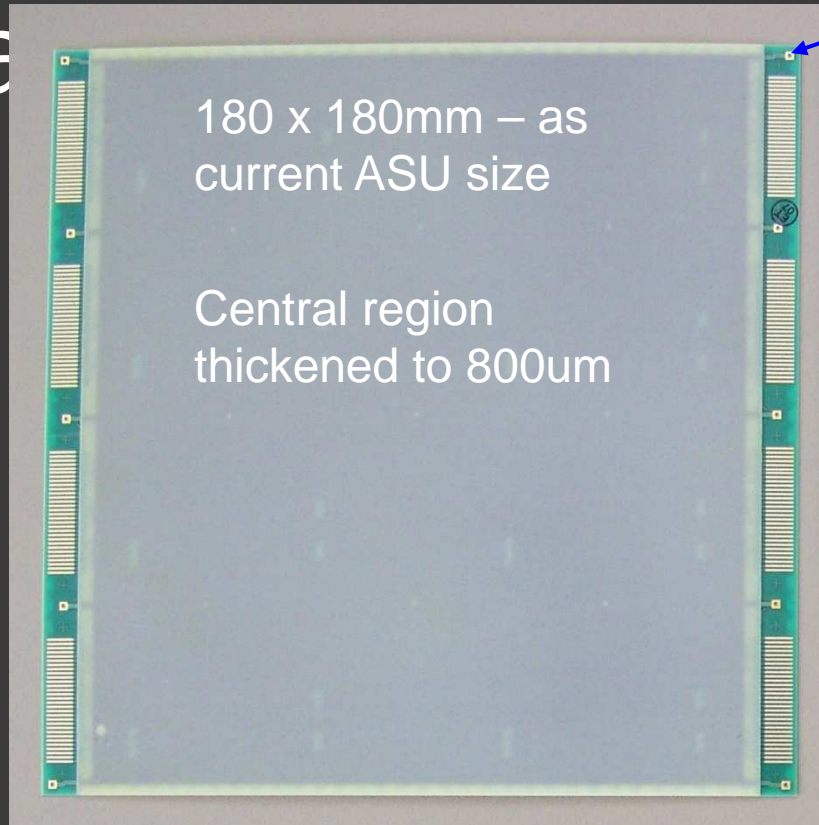
**FFC-Bridges:** we have 250 cut, 250 on roll

EGAL SLAB Interconnect –  
Top view

# Where we

Interconnect  
region

a



400um

4 identical rows of differential tracks  
connecting 36 way interconnect pads  
on left and right

Can be sliced into 4 sections, so  
provides for many trials

Differential tracks have a range of  
spacings & other characteristics to test  
signal propagation and cross-talk

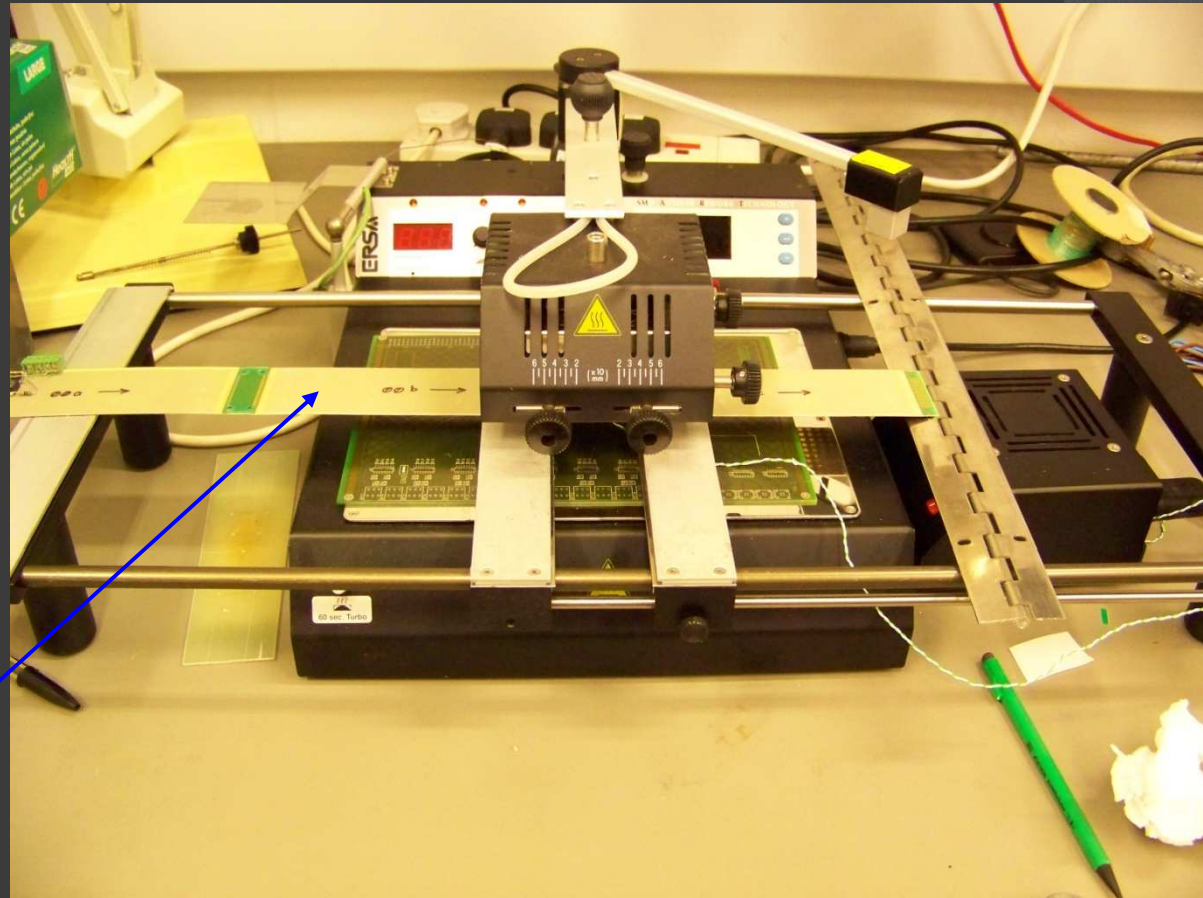
ASU-Test PCB: we have 15

ECAL SLAB

Interconnect –

# Where we are

3 bits of ASU-Test  
being joined: reflow  
of 2<sup>nd</sup> and 3<sup>rd</sup>



Using the IR Re-work station

ECAL SLAB Interconnect:

# Conclusions

There are major advantages in using Bridges:

- Removes major bottleneck in number of connections
- Promises greater reliability
- Rework likely to be easier

There's a lot to be done:

- We are trying out many things
- LAL Mechanical Prototype will also test PCB-Bridge mechanics

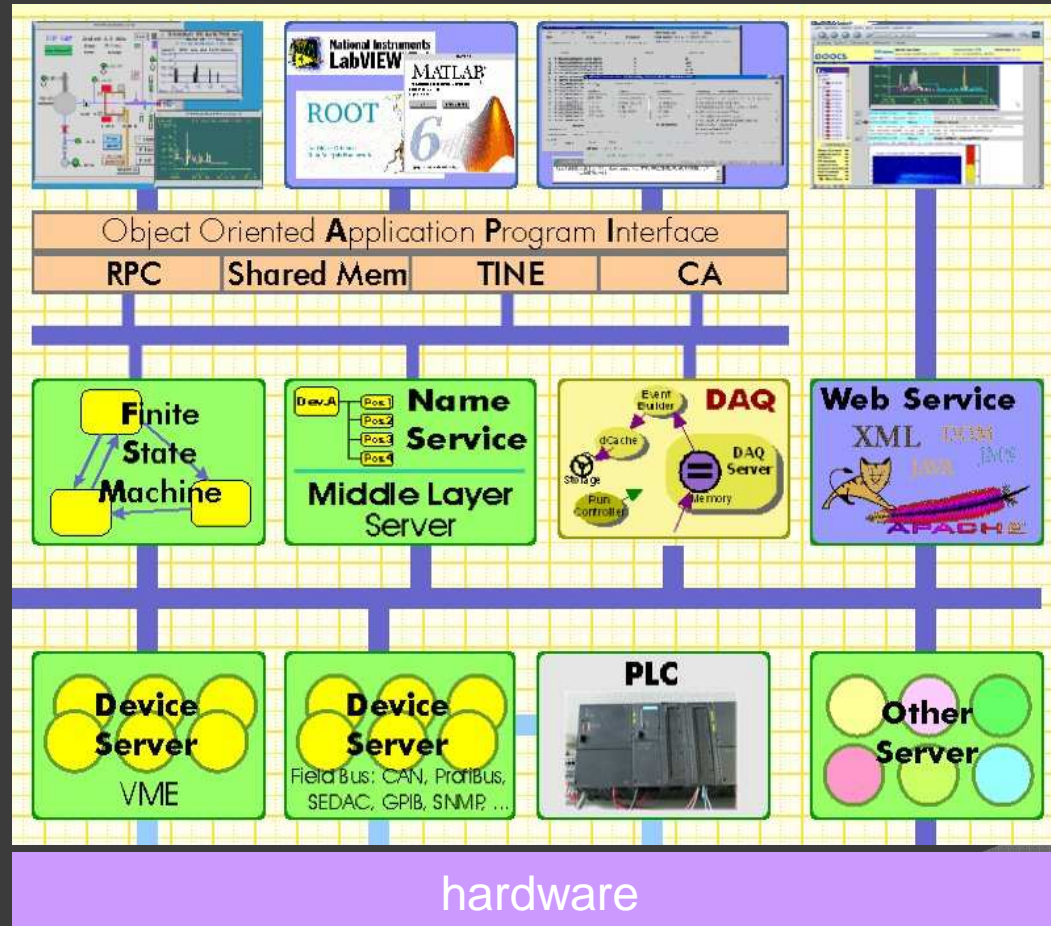
We are finding answers:

- 1mm pitch connections with continuity and no shorts
- IR re-flow looking very good:
  - ERSA Re-work station OK
  - Home-brew Imaging IR source may fit well into large-scale assembly procedures: full width re-flow, multiple heads,...



# DOOCS overview

- 3 layers
- common APIs
- modular design
- multi protocol (RPC, TINE, EPICS, shared memory)
- device level (~200 server types)
- middle layer (FSM, FB, DAQ)



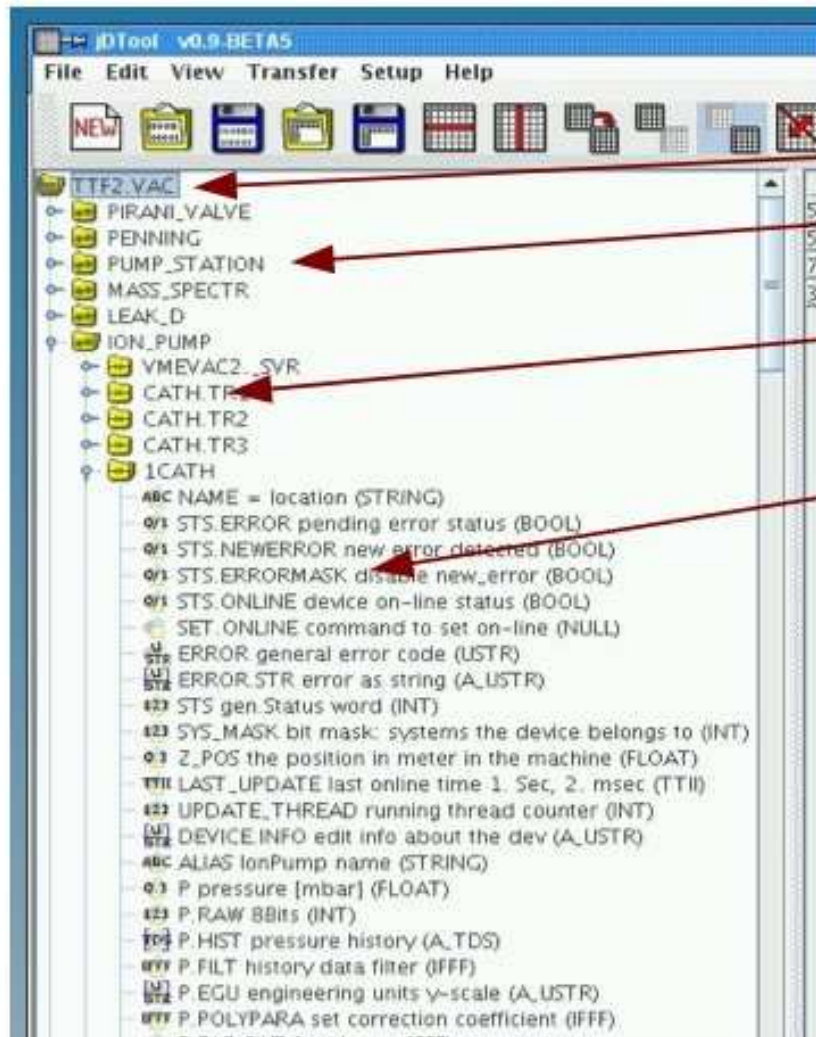
User Interface

Program Interface

Middle Layer

Hardware interface

# ENS naming service



FACILITY == Accelerator

DEVICE == Type of a device

LOCATION == position inside the accelerator

PROPERTY == list of properties

Example:

CALICE.ECAL/ODR/ODR1/STATUS

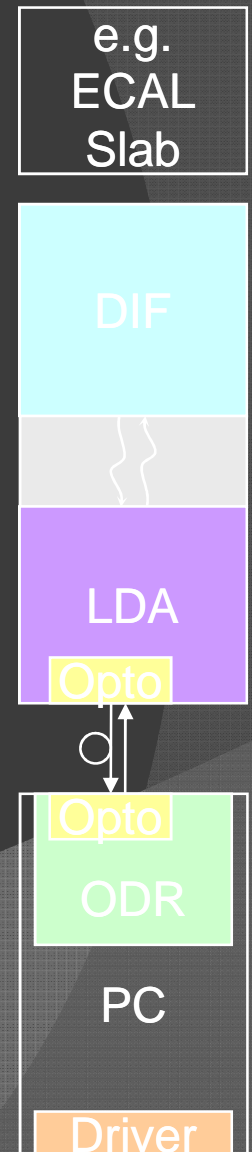
# ENS naming service: hierachical DAQ system

- send data to DIF by wrapper through ODR and LDA (have switch to configure debugging modes which go directly to the LDA or DIF)
- ENS naming service can signal connections by additional properties, e.g. for device DIF:

CALICE.ECAL/DIF/DIF1/ODR\_CON

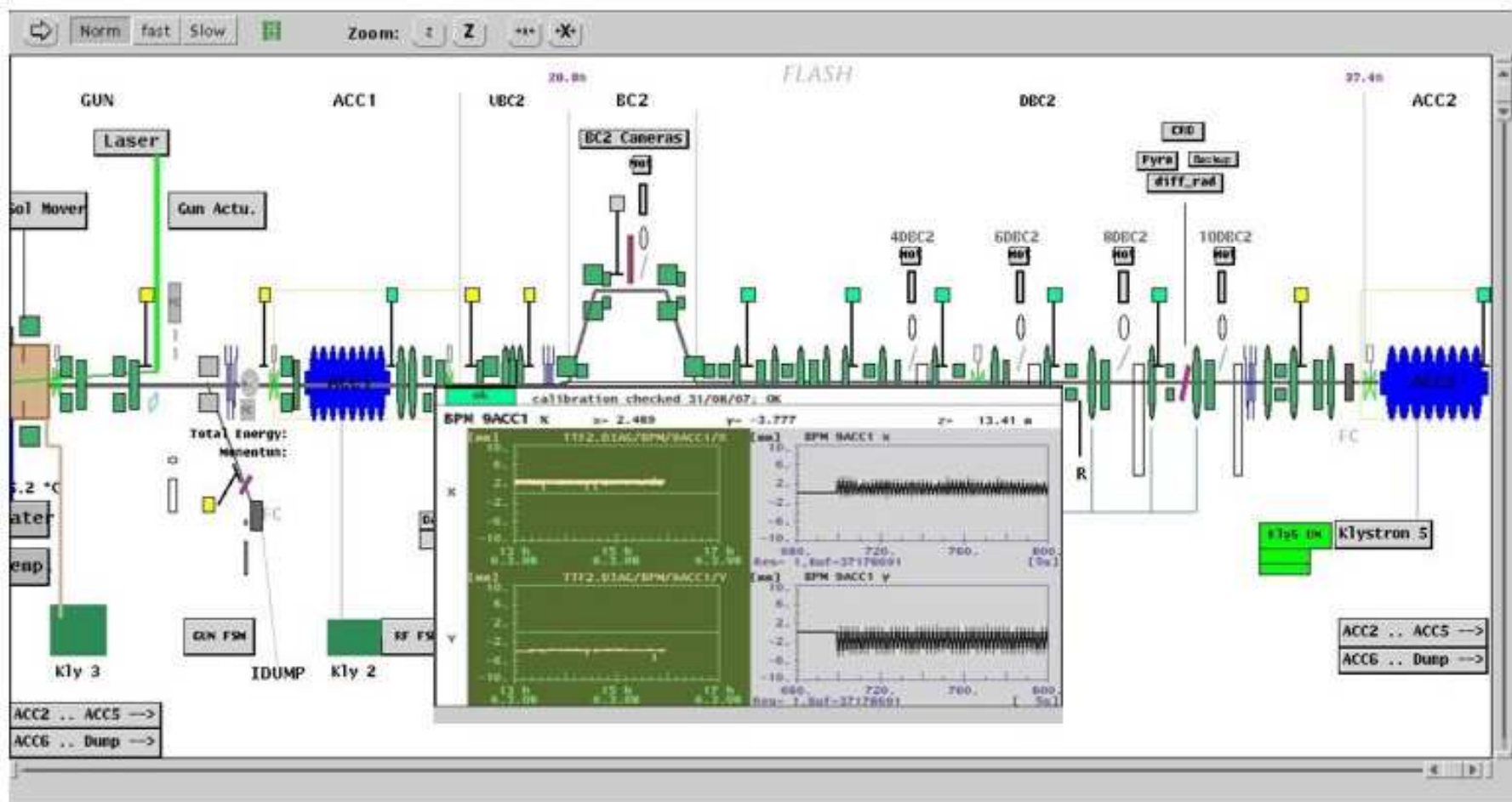
CALICE.ECAL/DIF/DIF1/LDA\_CON

CALICE.ECAL/DIF/DIF1/DEBUG\_MODE



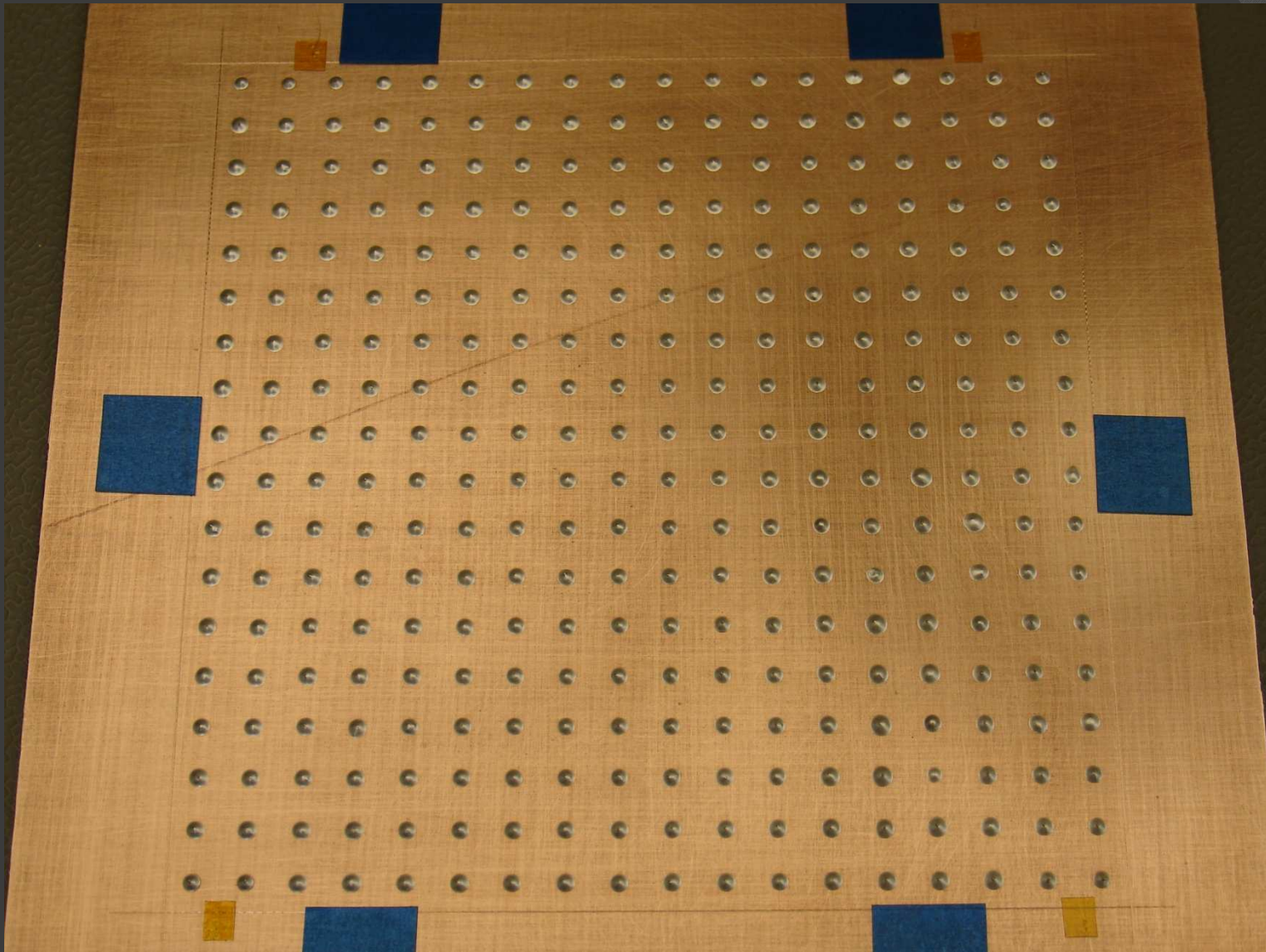
# Example of monitoring GUI

DOOCS Data Display (DDD)

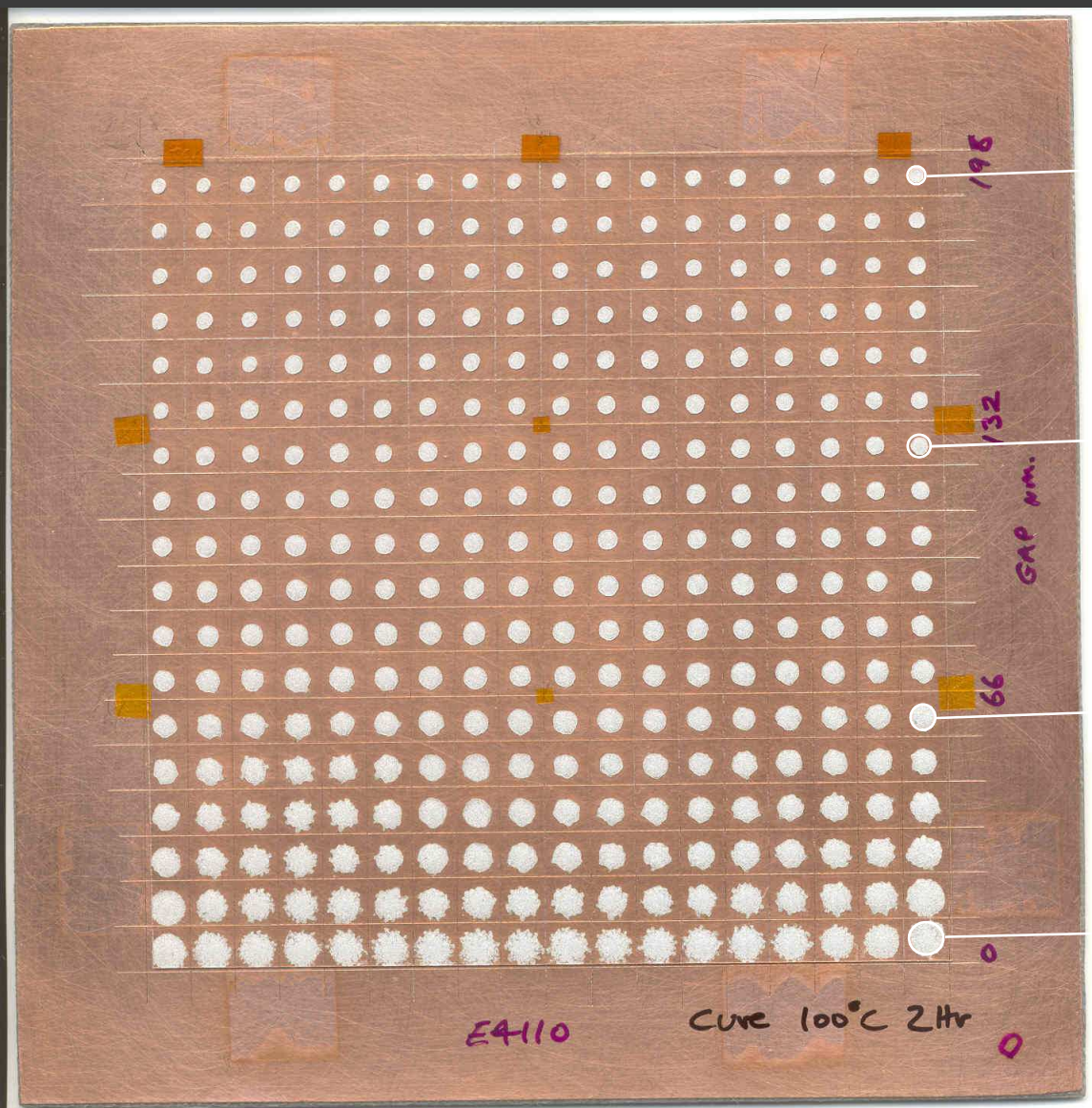


# Glue/Mechanics

- Sticky stuff



The baseboard before overlaying glass plate



Ø1.6mm

Ø2.0mm

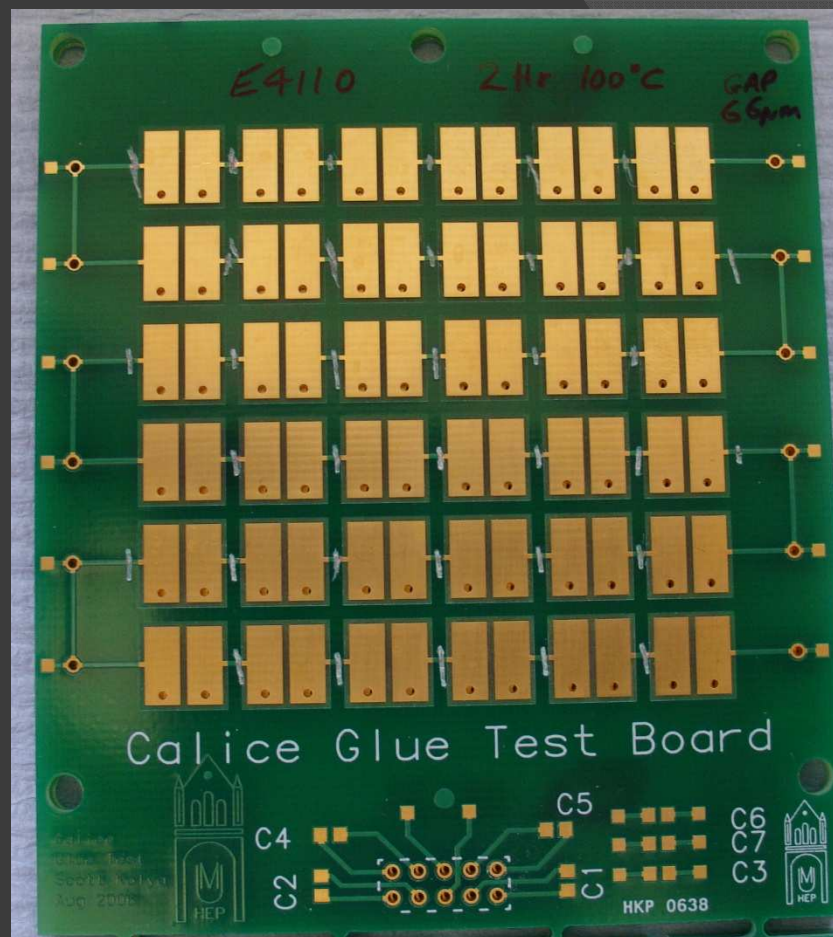
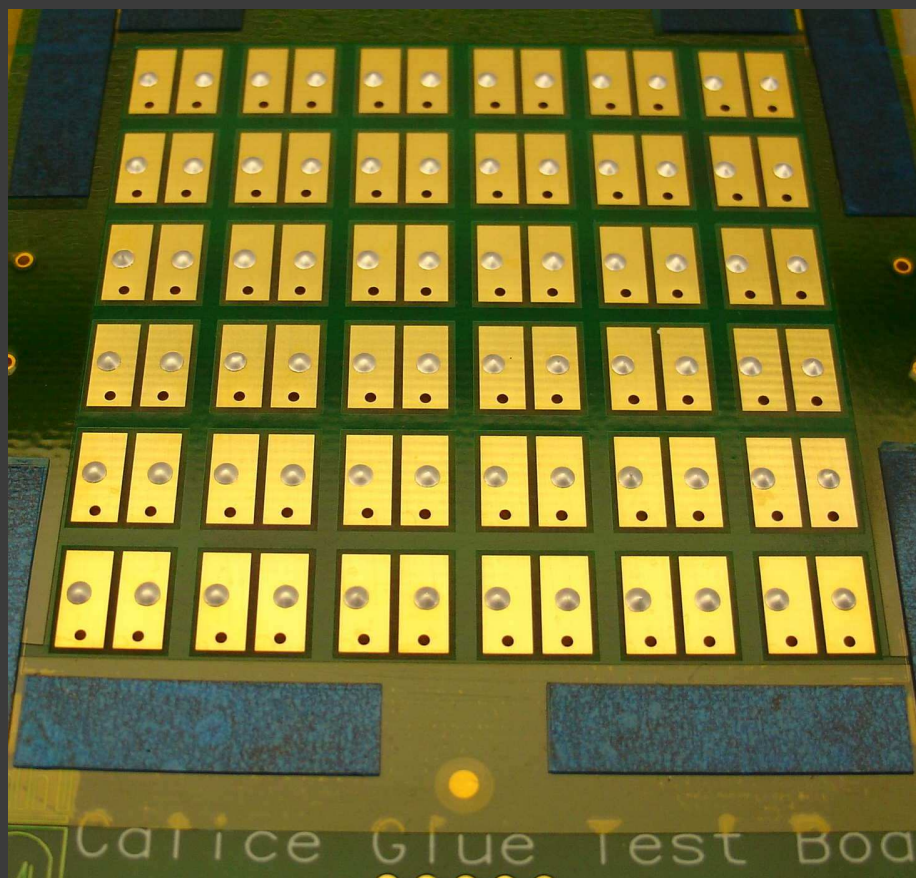
Ø2.5mm

Ø3.6mm

Glass Plate #2

0.2 sec per dot

Mid spacers under plate



12 x 6 dots @0.2 sec on CALICE test board  
Two boards sandwiched together, 66µm gap  
Interpad links cut on top board  
Resistances between overlapping pads measured –  
<math><0.005\Omega</math> per pad





# Physics

- ◎ [Neural Networks](#)
- ◎ [G4 physics lists and data](#)

# Upcoming Conferences and Plans

## Upcoming Conferences

- CALOR'08 (Pavia, 26-30 May)
- ECFA ILC Workshop (Warsaw, 9-12 June)
- NDIP 2008 (Aix les Bains, 15-20 June)
- ICHEP'08 (Philadelphia, 29 July-5 August)
- PSD8 (Glasgow, 1-5 September)
- IEEE (Dresden, 19-25 October)
- IPRD08 (Siena, 1-4 October)

## 16 Abstracts submitted to CALOR'08; 4 to ICHEP.

## Papers/Analysis notes

- ECAL Commissioning paper (Anne-Marie)
- ECAL electron response paper (Cristina)
- Three AHCAL notes planned
- "Final" ScEcal note on 2007 data

# Future

## ⦿ DevDet

- UK involved in ECAL and DAQ workpackages
  - Low level participation to keep our fingers in the pie...

## ⦿ STFC SOIs

- Due in May
- MAPS and DAQ under consideration