Tera-Pixel APS for CALICE

Progress meeting, 6th June 2006

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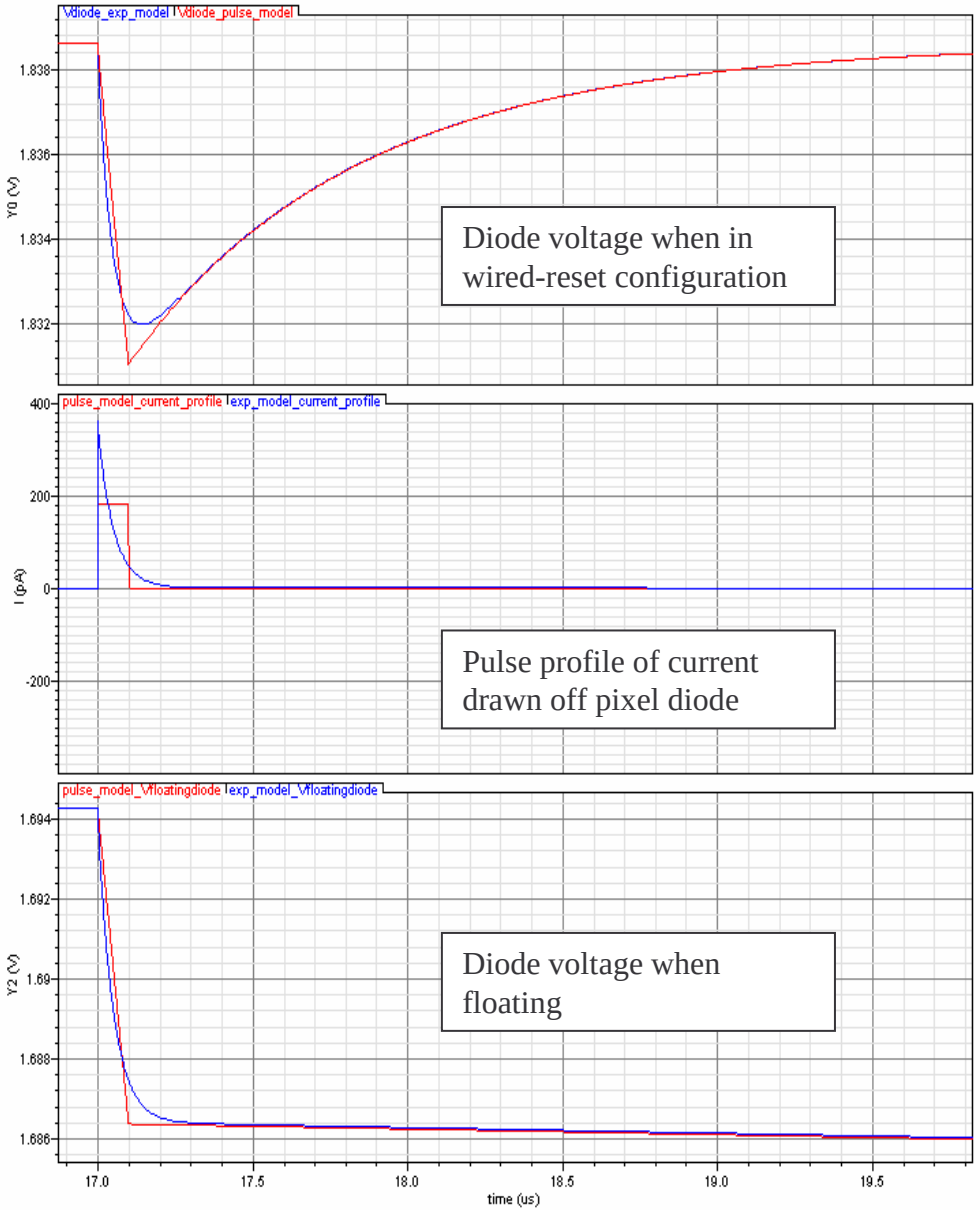
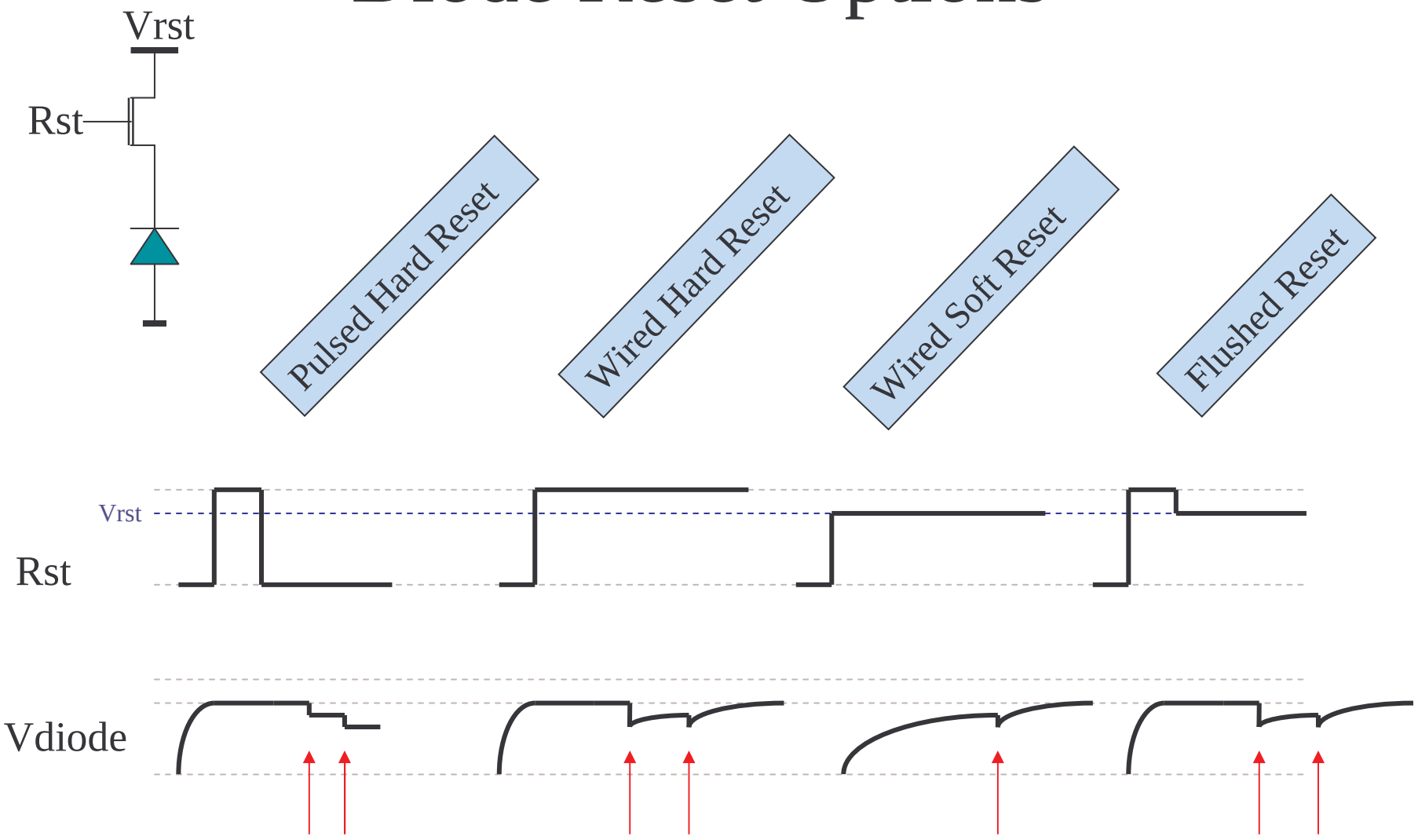
Charge collection simulation model

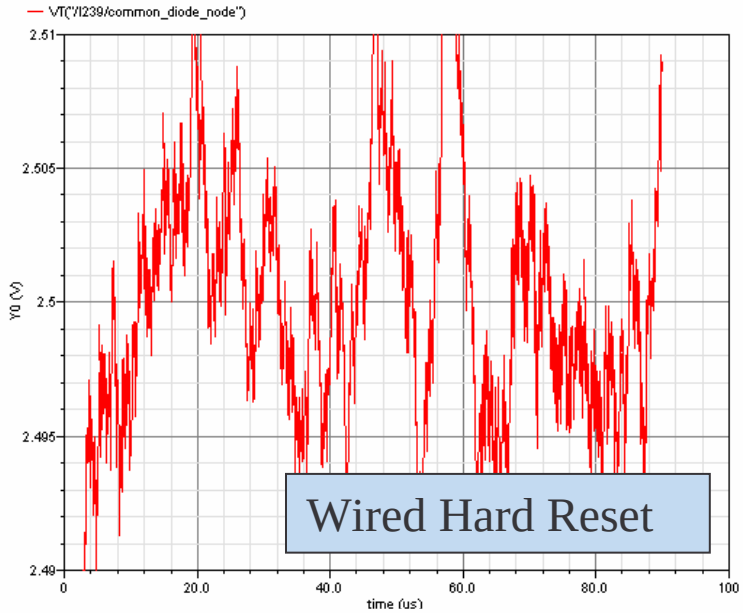
- So far have been using a 100ns pulse of constant current to model a physics hit
- Guilio recommended an exponential decay would be more appropriate
- Guilio sent some numerical data for hits – have estimated a decay time constant
- Example simulations show subtle difference in circuit response & verify correct calculation from simulation parameter ***number_of_electrons***
- Will use this model from now on

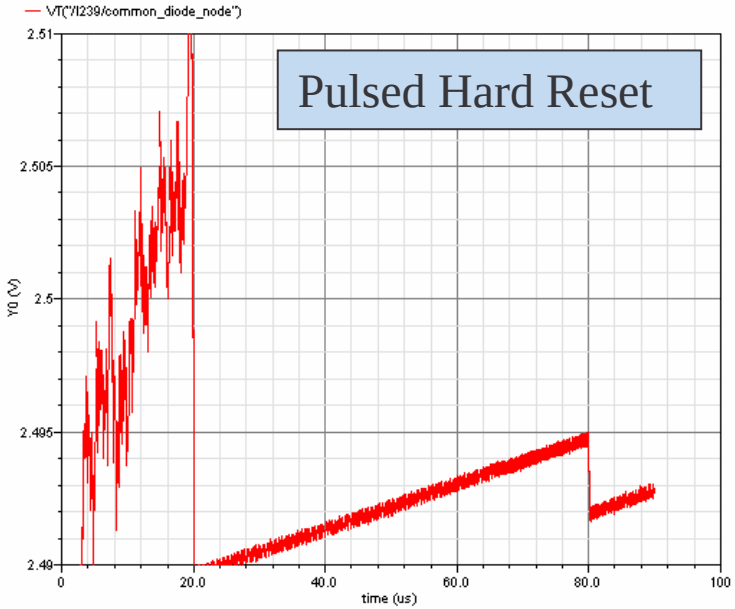


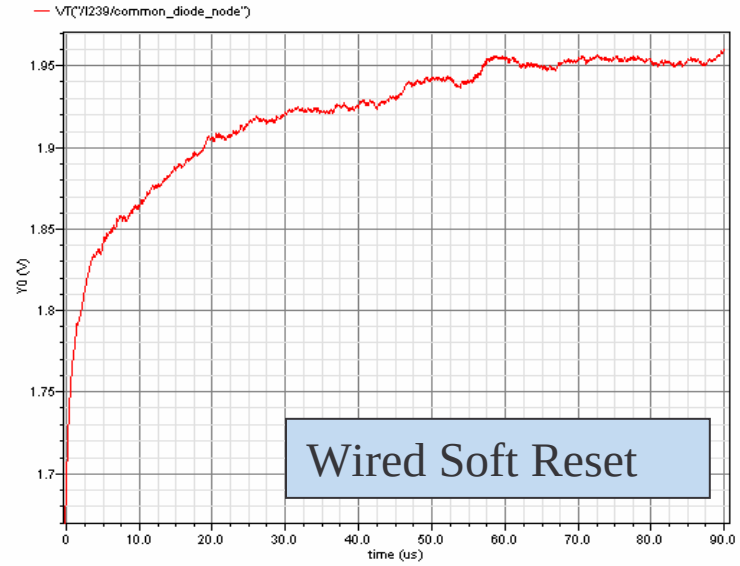
Diode Reset Options

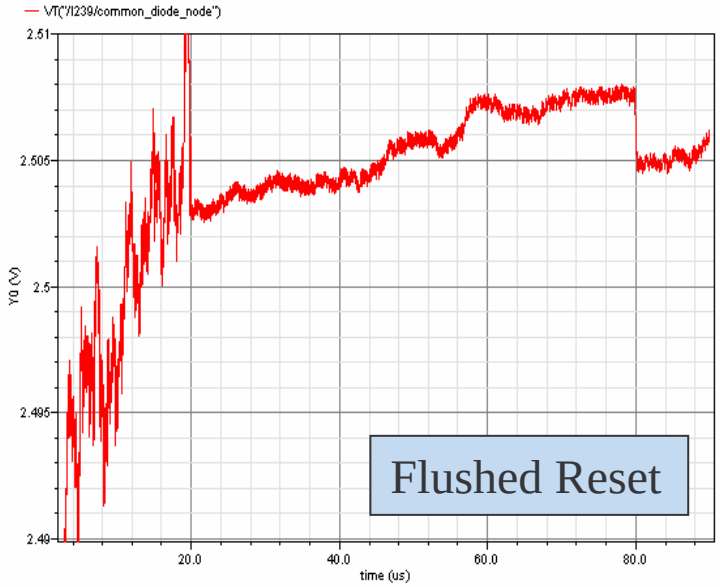


Diode Reset Options: Transient Noise Simulations



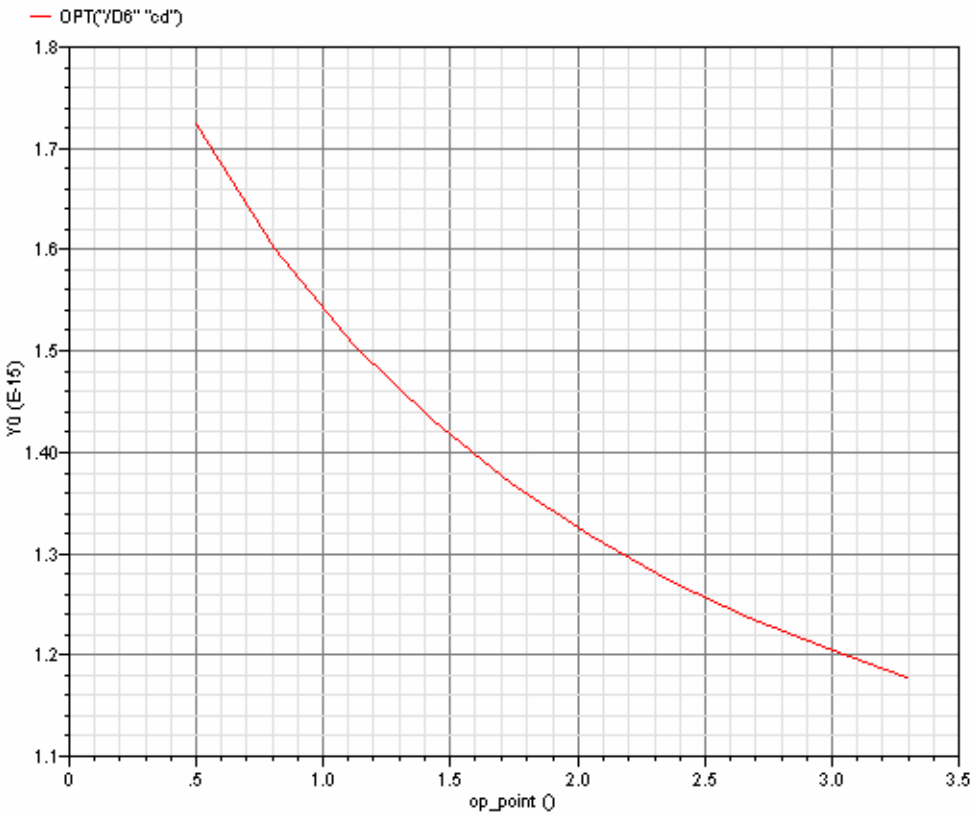




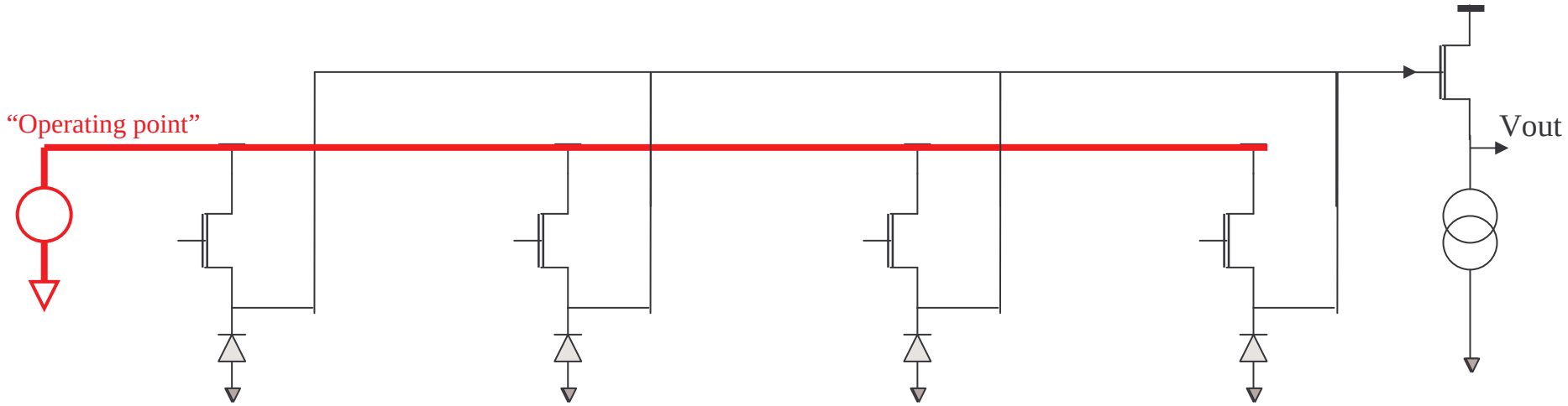


Diode operating point

- Capacitance of diode increases for higher voltages
- By choosing to bias the diode favourably will achieve higher voltage for same charge deposit
- Operating point may be set by analog-sum circuit or other constraints, may not have the choice!
- 0.9umx0.9um diode
- Hard reset to “op_point”



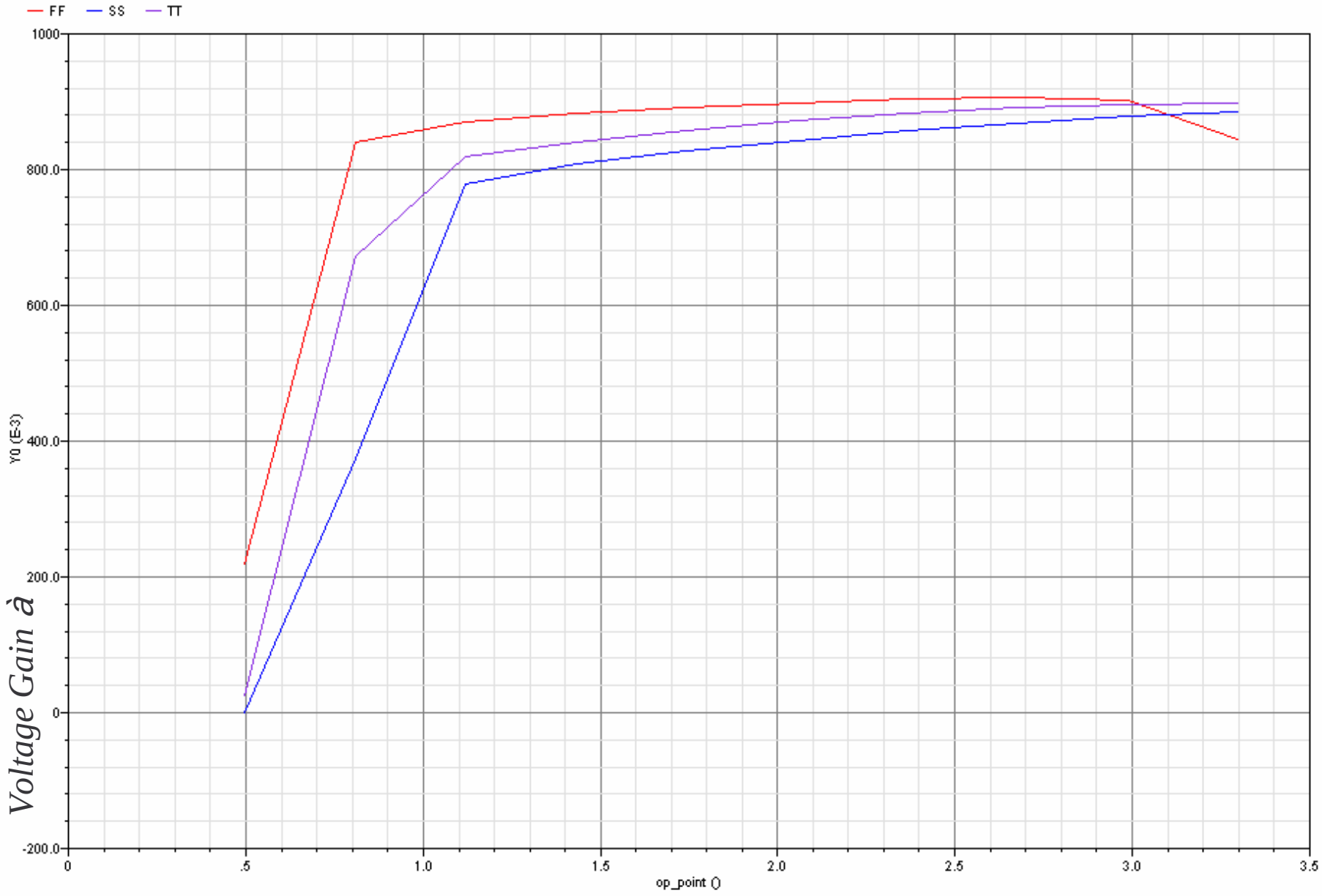
Parallel Diodes + Source Follower



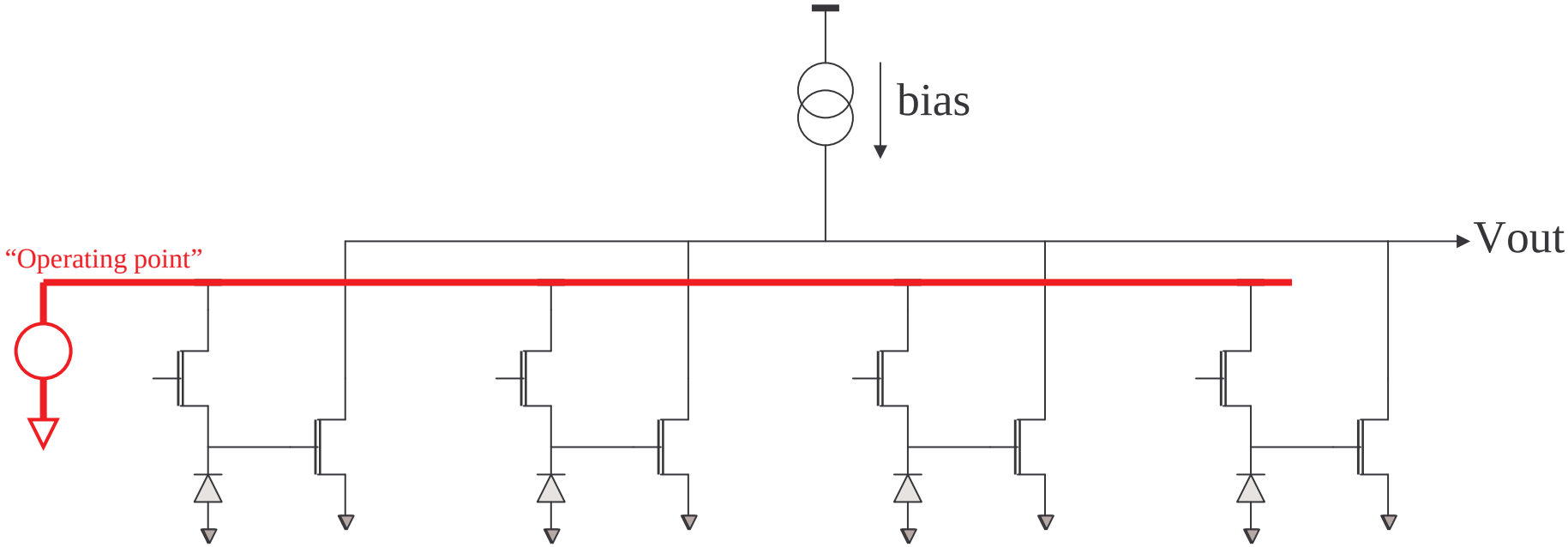
Diode Sum: Source Followers

		Single diode Source follower			4 Parallel diodes Source follower			
Number of pmos		0			0			
Vdd		2.5			2.5			
Static current		500nA			500nA			
Process Corners		**Slow**	**Typ**	**Fast**	**Slow**	**Typ**	**Fast**	
Vout step for 450e- input stimulus (mV)	1diode	8.0	7.4	7.0	2.34	2.32	2.36	*Expect identical results since charge summing node is common to all diodes: The perfect sum!* *But – high capacitance à small voltages*
	2diode				2.34	2.32	2.36	
	3diode				2.34	2.32	2.36	
	4diode				2.34	2.32	2.36	
Voltage Gain	(min) (max)	0.77 0.87	0.8 0.9	0.84 0.90	0.77 0.87	0.8 0.9	0.84 0.90	*Lower range could be achieved using low Vt devices if required*
Range of operation	(min) (max)	1.0 3.3	1.0 3.3	0.8 3.3	1.0 3.3	1.0 3.3	0.8 3.3	
Ton/Toff								
Noise								

(4 Parallel Diodes) Source Follower: Gain vs Diode voltage: Process Corners

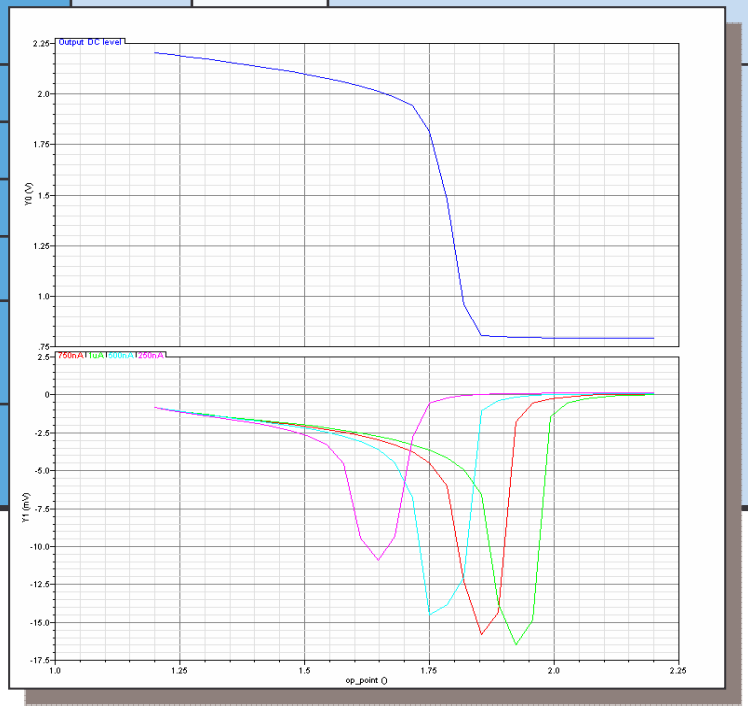


Inverter Sum

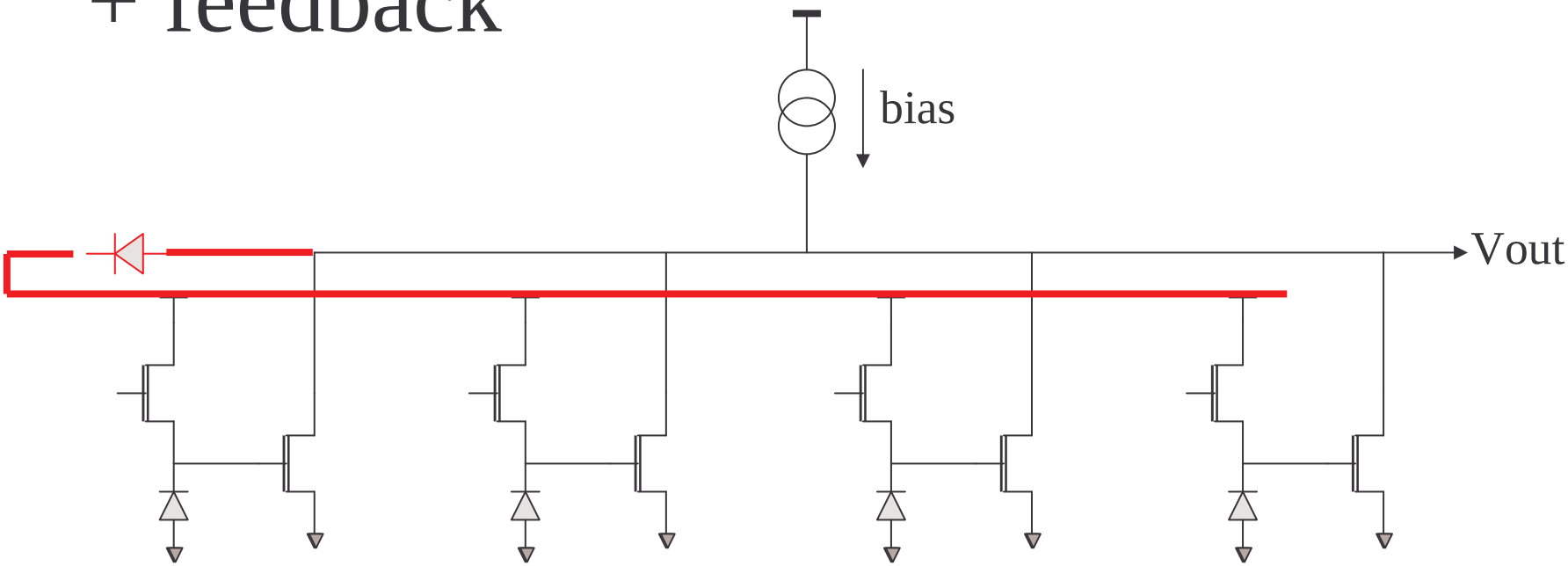


Diode Sum: Other Circuits

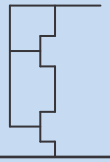
		Forked source follower [JC]			Inverter sum [RT]			Nmos amplifier [Dorokhov/mimosa 15]
Number of pmos		0			1			0
Vdd		2.5			2.5			
Static current		500nA			500nA			<3uA Not current limited!
Process Corners		**Slow**	**Typ**	**Fast**				
Vout step for 450e- input stimulus (mV)	1diode	4.23	4.3	4.40				
	2diode	4.68	4.78	4.77				
	3diode	4.84	4.94	4.90				
	4diode	4.92	5.0	4.97				
Voltage Gain	(min) (max)	0.185 0.244	0.190 0.252	0.196 0.255				
Range of operation	(min) (max)							



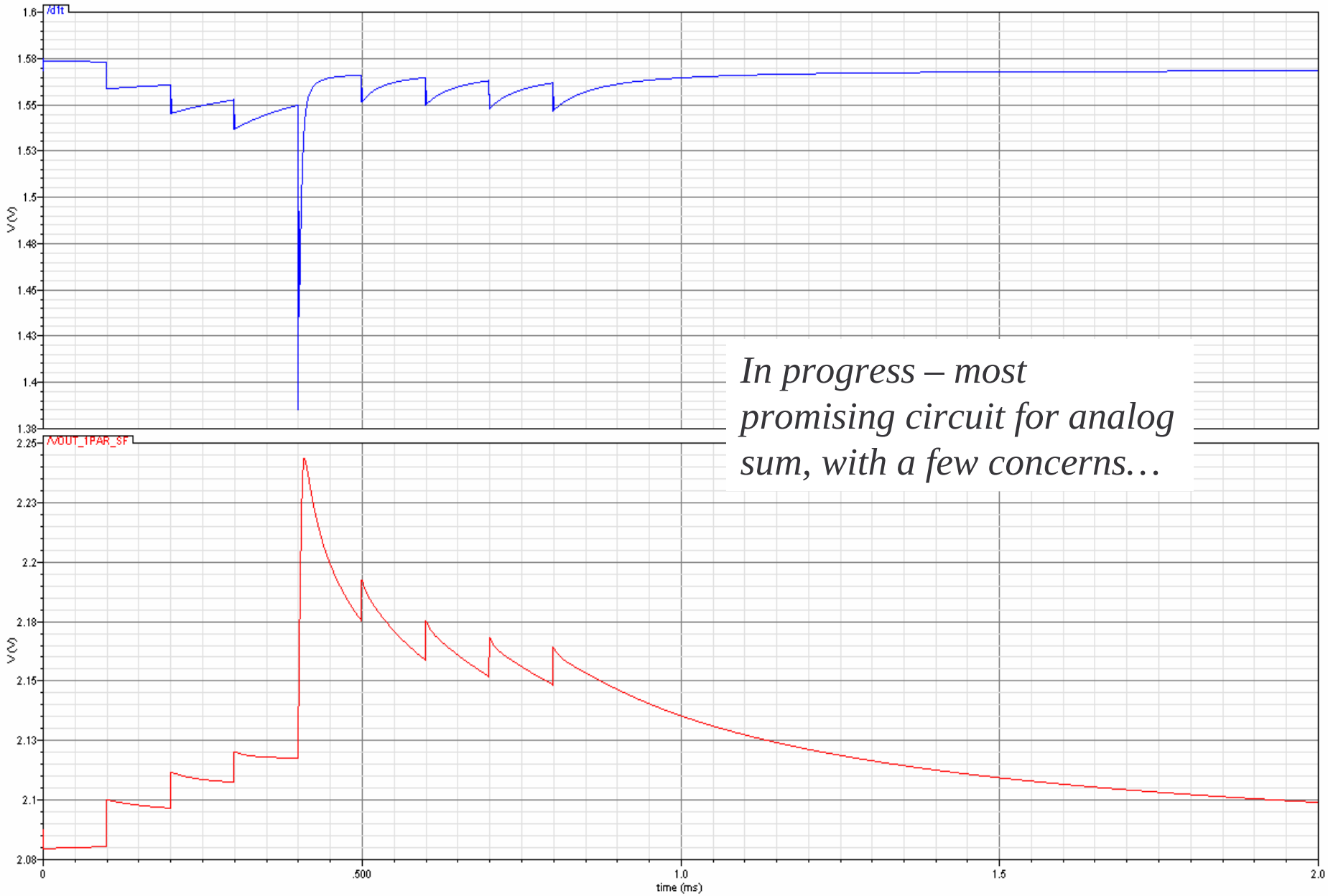
Inverter Sum + feedback



Diode Sum: New Inverter with Feedback

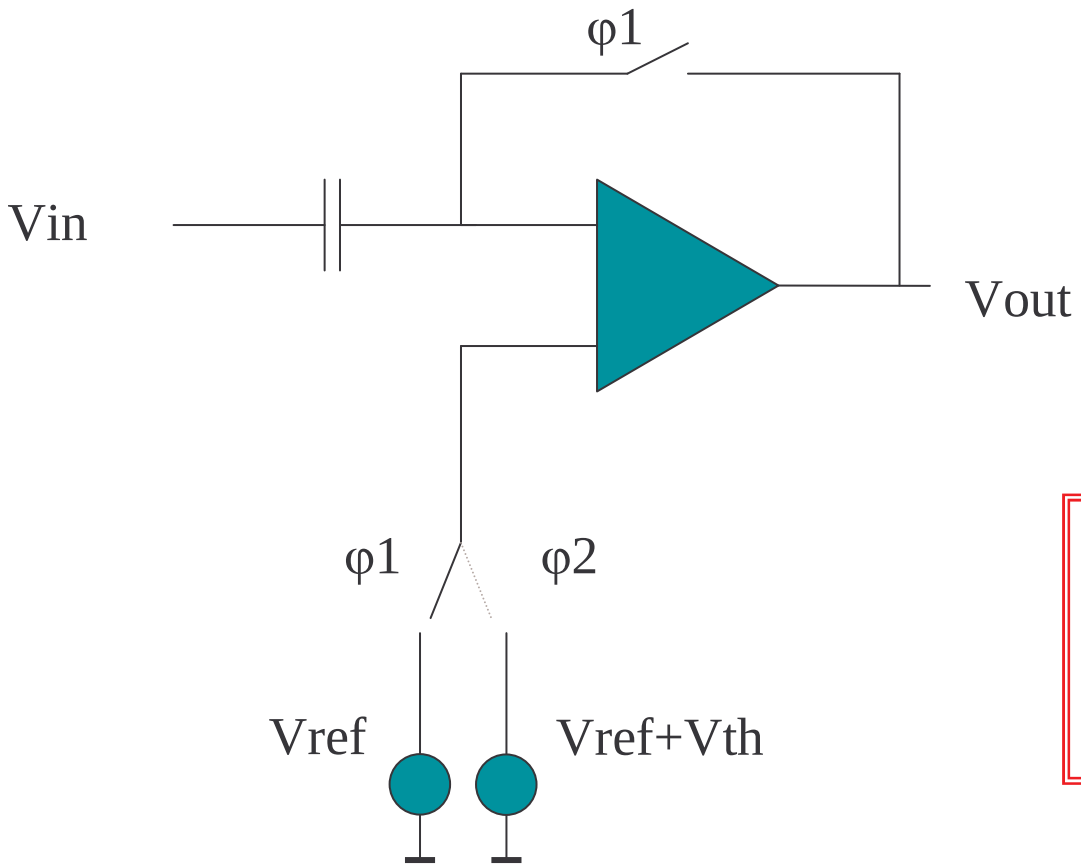
		Feedback circuit 						
Number of pmos		1						
Vdd		3.3						
Static current		500nA						
Process Corners		**Slow**	**Typ**	**Fast**				
Vout step for 450e-input stimulus (mV)	1diode	18.6	17.3	16.1				*Note that diode voltage varies significantly in different process corners, so the step voltage seen to 450e charge will vary also due to diode capacitance dependence on bias voltage.*
	2diode	20.4	18.9	17.3				
	3diode	21.0	19.4	17.6				
	4diode	21.4	19.7	17.7				
Voltage Gain	(min) (max)							
DC diode voltage		1.8	1.6	1.3				
DC output voltage		2.5	2.1	1.5				

Diode Sum: New Inverter with Feedback



In progress – most promising circuit for analog sum, with a few concerns…

1st Auto-zero Comparator



φ1: Reset: Unity gain amplifier stores amp and signal offsets on capacitor

φ2: Compare: Open loop amplifier compares auto-zeroed signal with reference + threshold

1uA not quite enough current to meet speed required (quick test) – principal demonstrated in simulation