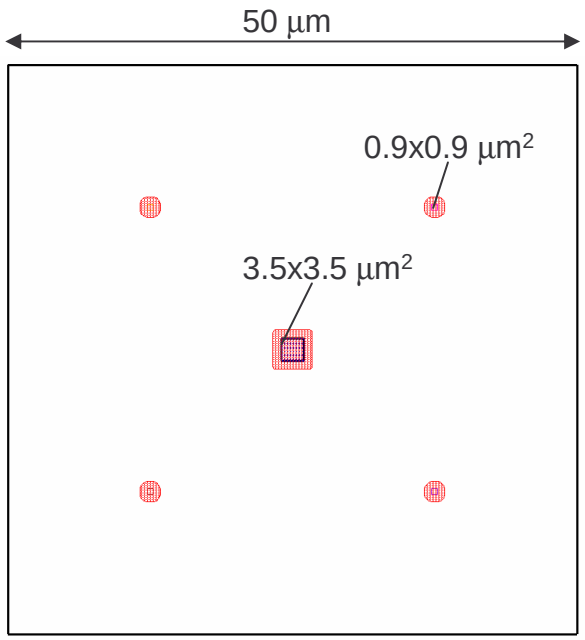
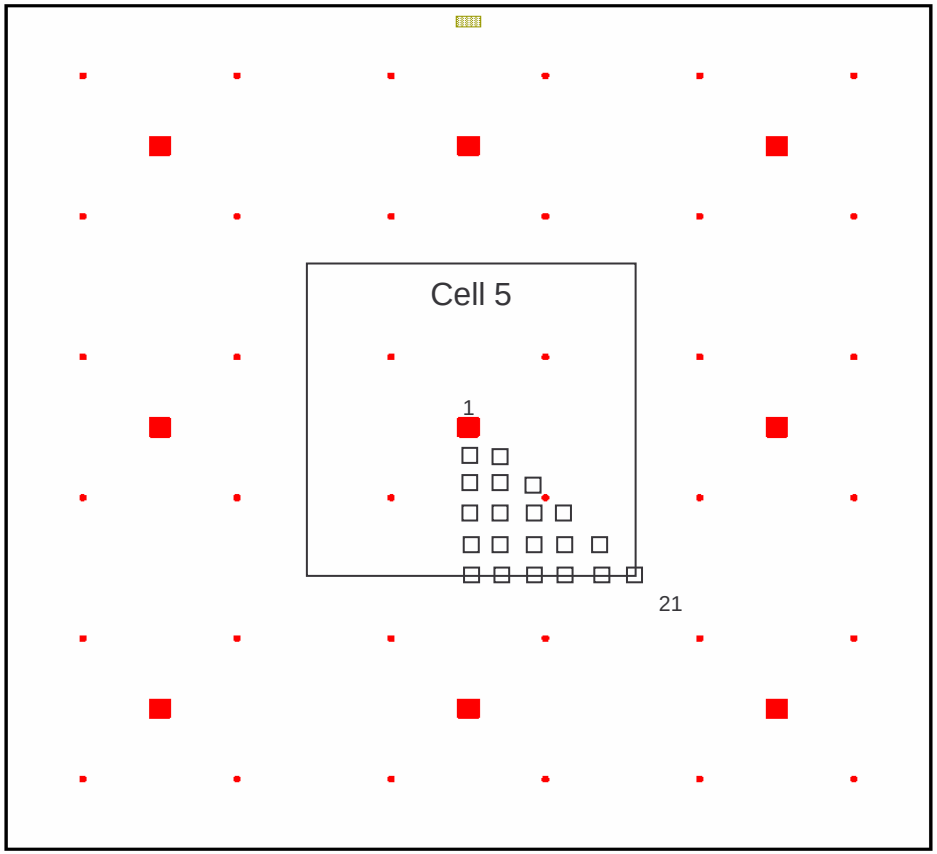
CALICE simulation results

G.Villani 06

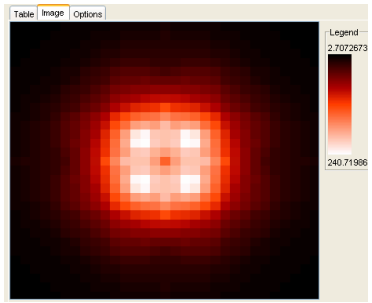


Pixel layout



Simulated cell layout

- 21 hits simulated, 5 μm pitch
- 121 extrapolated hits / pixel
- 961 extrapolated hits / cell



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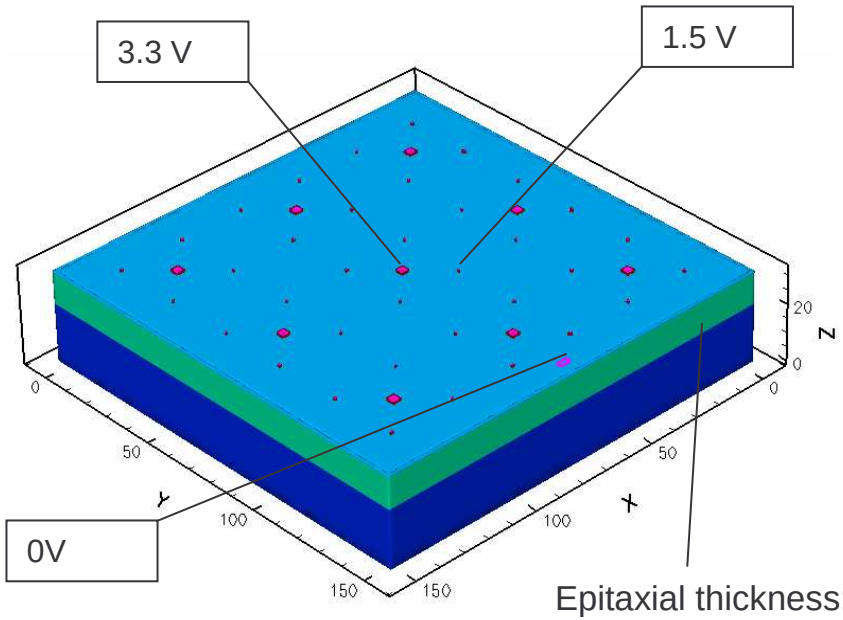

Bias

- Diode : 1.5V fixed
- Nwell: 3.3V
- Pwell: 0V
- Subs: float

- Σ diodes Collected charge vs (x,y)

CALICE simulation results

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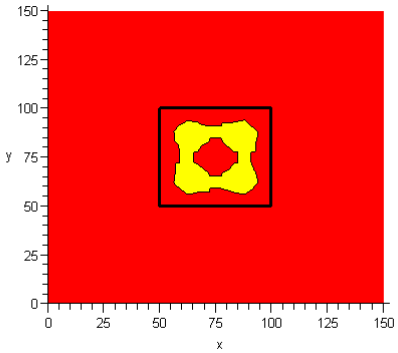
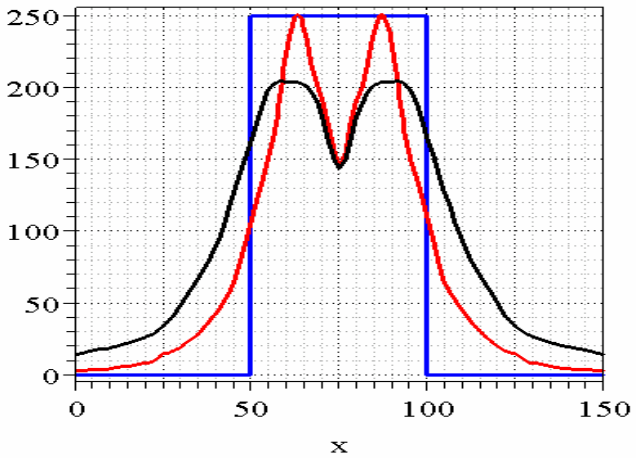
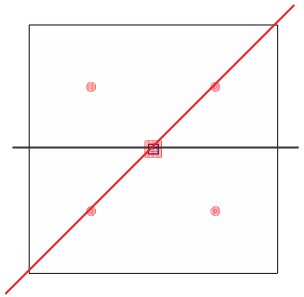
Comparator's threshold: 200 e^-



Pixel coverage (e^- threshold)

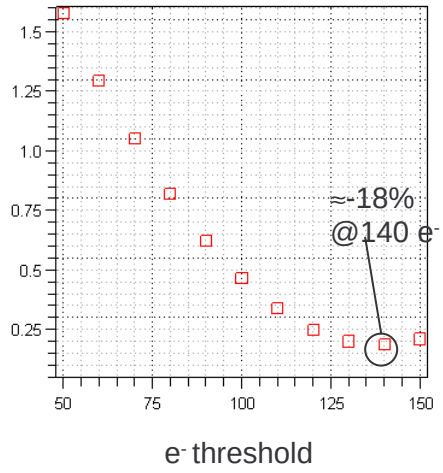
e^-





Central cell $Q_{coll}(x,y)$ sample

1/S



Error in pixel coverage

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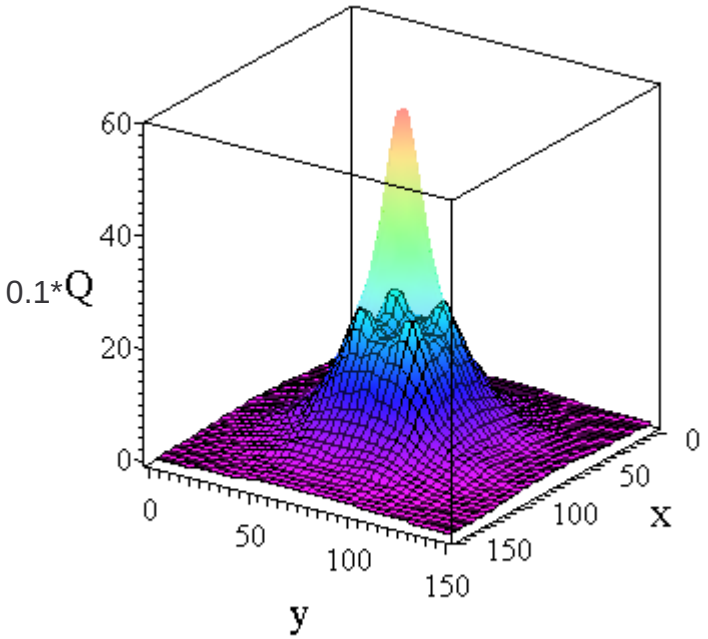

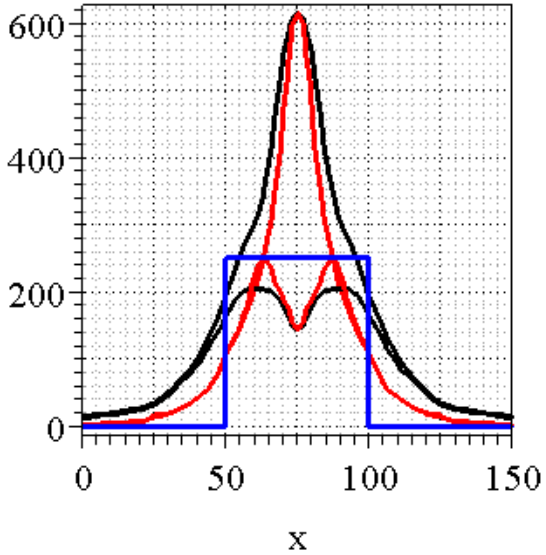

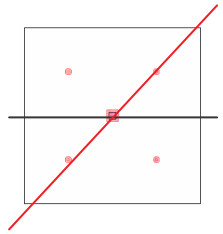

Charge collected by central Nwell

q Charge lost by central N Well around 620 e^-

CALICE simulation results

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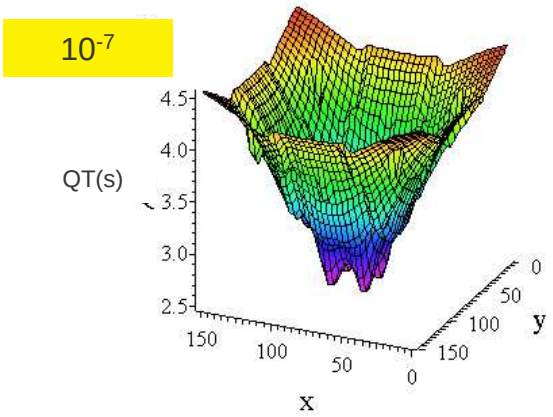
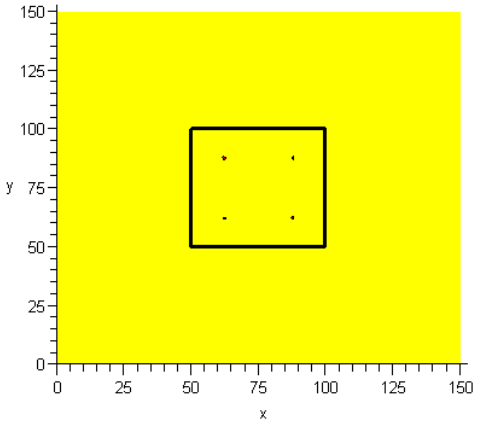


Diode charge collection time

q Collection time ≈ 300 ns for pixel coverage

q Reduction of collection time for ‘smaller’ pixels:

250 ns



CALICE simulation results

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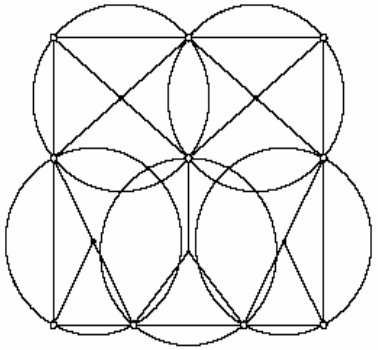
Conclusions

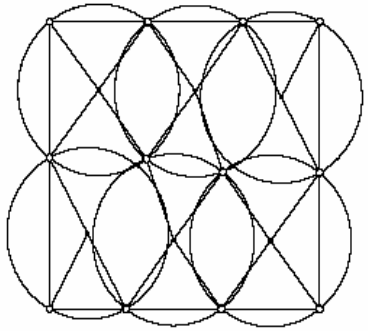
- Minimum Σ charge signal ≈ 100 e^-
- Optimal threshold ≈ 140 e-
- Collection time ≈ 300 ns for pixel coverage
- Increase in minimum collected charge requires to increase the collecting surface:

Ø Increase diode size (1.8 μm in progress)

Ø Increase the number of diodes

- Ultimately, the S/N for both approaches dictates the optimum solution
- Collection time can be decreased by reducing inter diodes distances: probably more effective with increase number of diodes rather than surfaces
- Likelihood of consecutive hits on the same pixel





Optimal coverage examples