# *Pre-Sample pixel (v1.2): Capacitor technology change*

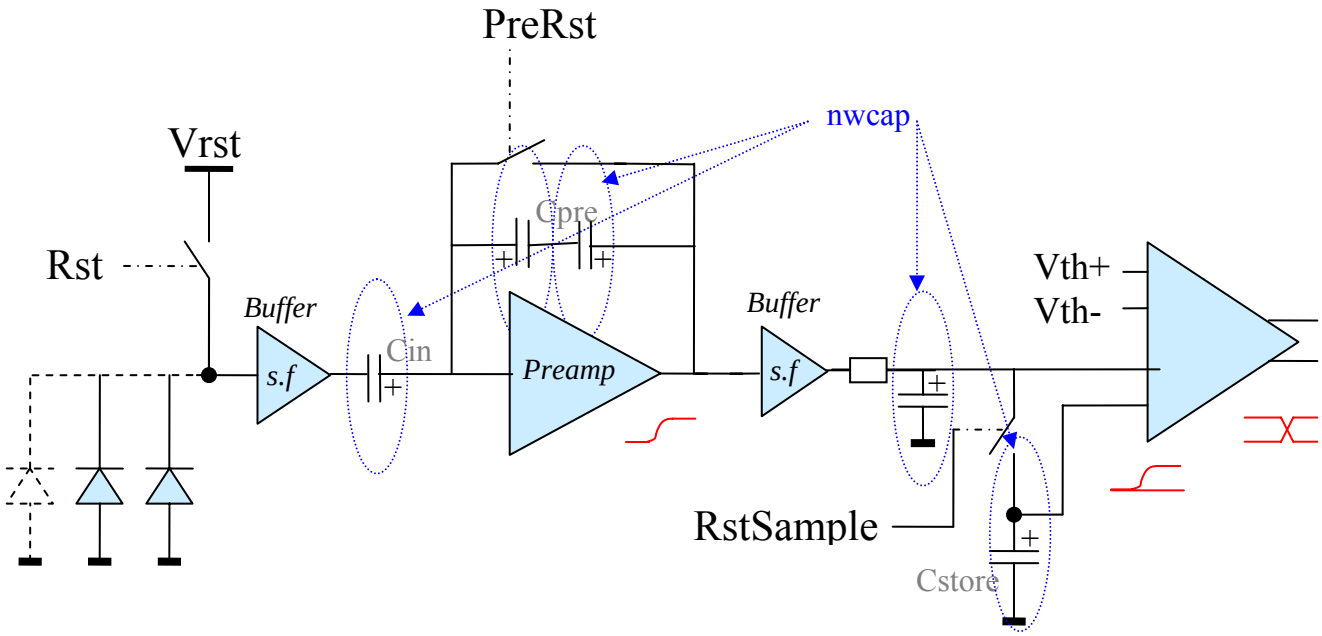
## *Summary/Dialogue*

A new capacitor is selected to improve layout and reduce parasitic capacitance. This document is intended to verify that the pixel performance that has been reviewed and approved is not compromised by the change to the capacitors. The capacitor sizes have been specifically selected to offer approximately equivalent values, hence only subtle variations in circuit performance is expected.

The pixel circuits are modified as follows:

- Cin is made from 30 unit capacitors of 1x1 microns (connected in parallel)
- Cpre is made from 2 unit capacitors of 1x1 microns (connected in series)
- Cstore is made from 1 unit capacitor of 3x3 microns
- Cfilt is made from 1 unit capacitor of 3x3 microns

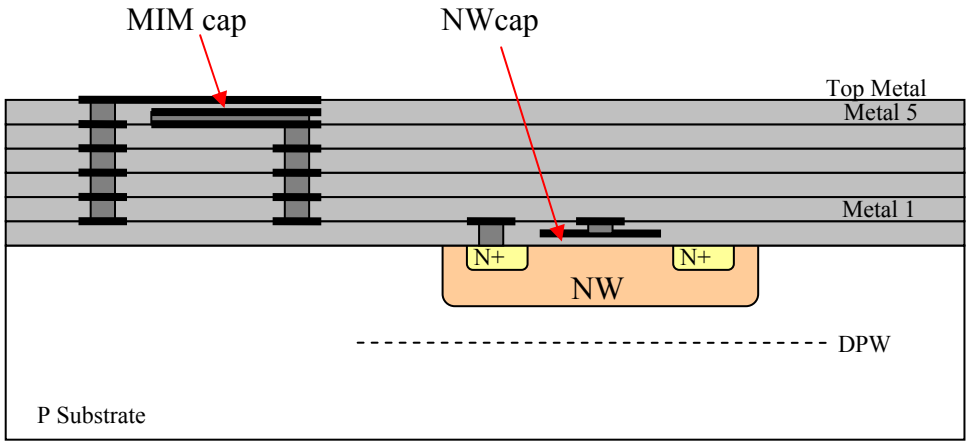
### *PreSample Pixel Overview*




## Capacitors

The original MIM (metal-iso-metal) capacitors that were used in circuit simulations are fabricated using the top metal layer, and therefore the connections to the transistors must include a stack of vias and metal on each intermediate layer which are likely to introduce extra parasitic capacitances and exposure to interference from other parts of the circuit.

The alternative capacitor technology uses an Nwell and a polysilicon gate to create the two parallel plates. The thin oxide layer provides the minimal separation and dielectric material between. The nwell can be used since the deep p-well implant provides the necessary protection from charge diffusing in the substrate.




The spice models for the NWell capacitor recommend a unit capacitor of 5x5 microns is used. This is because this is the cell size that has been used to develop the

simulation models. However, this yields a unit capacitor of 230fF which is too large for the small feedback capacitor used in the pixel circuits. We therefore propose to use a smaller unit capacitor of 1x1 microns. The design rules permit this re-sizing despite the recommendation.

The presample pixel does not rely on absolute capacitor value, but the ratio between the capacitors Cin and Cpre. Therefore model uncertainty due to sizing against the recommendations should not present a large risk to the success of the design.

The spice models quote capacitance per square micron for the 5x5um unit capacitor cell. These figures have been extrapolated below to the sizes that are used in the preSample pixel design.

| | **Low (fF)** | **Typ (fF)** | **High (fF)** |
|---|---|---|---|
| Unit 5x5 capacitor *(as recommended)* | 215 | 225.75 | 242.5 |
| Unit 1x1 capacitor | 8.6 | 9.15 | 9.70 |
| Unit 3x3 capacitor | 77.4 | 82.35 | 87.3 |
| Unit 2.8 x 2.8 capacitor | 67.42 | 71.736 | 76.0 |

The values chosen to replace the MIM capacitors achieve capacitance values that are close to the original values selected during the design of the circuits:

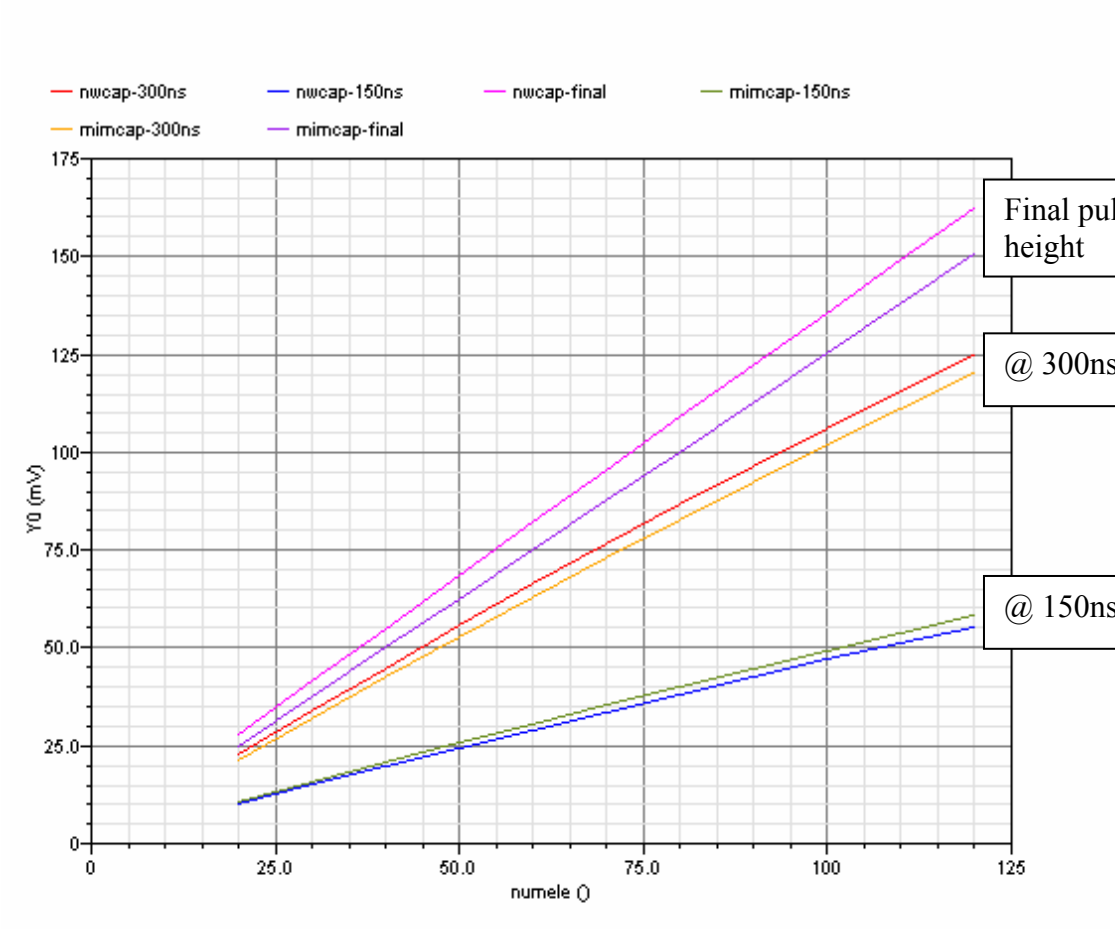
- Cin was originally specified as 250f and is now 225f in the typical case
- Cpre was originally specified as 4f and is now 4.57f in the typical case
- Cfilt was originally specified as 100f and is now 82f in the typical case
- Cstore was originally specified as 100f and is now 82f in the typical case

Circuit operation is expected to be the same as the original preSample pixel design. The simulations in the remainder of this document should demonstrate this is the case.

## *PreSample Pixel simulation: Small Signals around threshold*

The input signal (per diode) is swept from 20 to 120 electrons. The signal magnitude is plotted to check linearity and variation between capacitor technologies.

### Results Waveforms

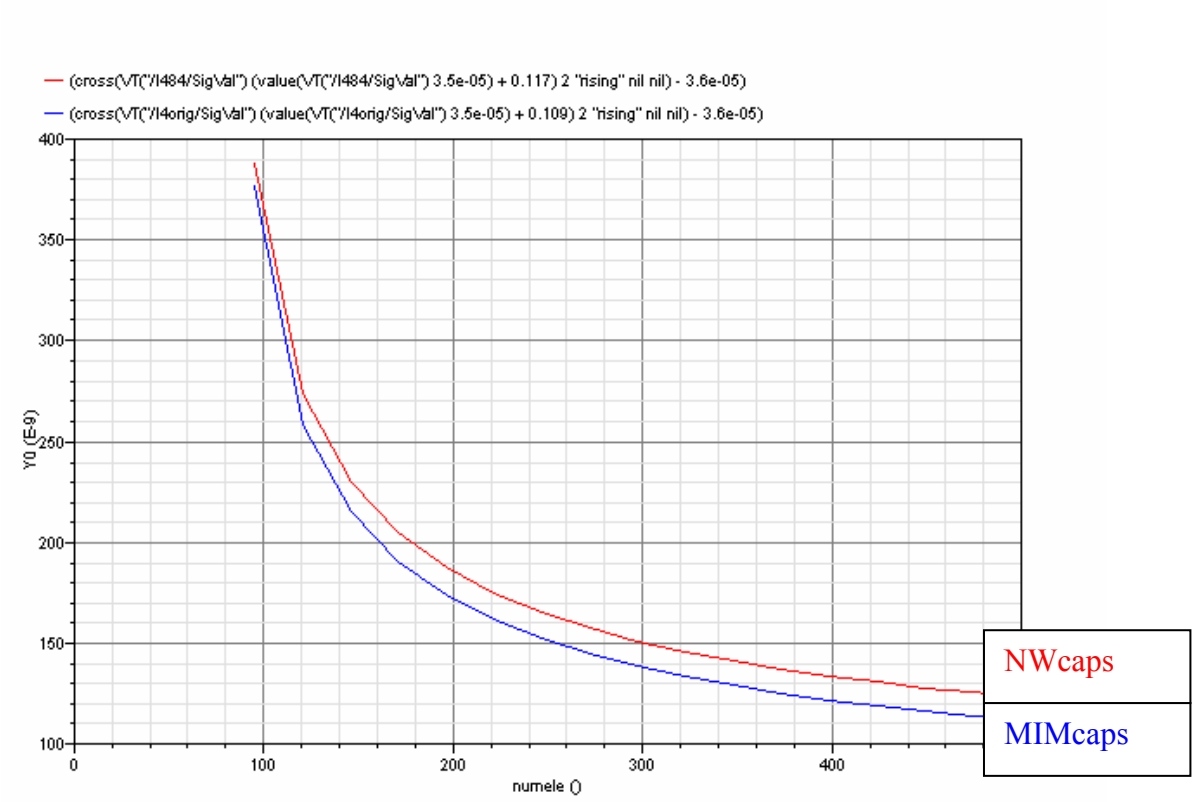



Above: The voltage at the comparator input is plotted at different times after the hit occurs for the original pixel design (mim caps) and the new pixel design (nw caps). The signal gain in this linear region is approximately 337uV/e- compared with 313uV/e- in the original design. The capacitor sizings have yielded a slight gain increase: Time-to-threshold must be checked to ensure the higher gain has not compromised circuit response time.

The “numele” variable represents the charge on each diode.

## Time to Threshold

A range of signals are applied to the original and new pixel circuits:  The threshold (for these calculations) is assumed to be 350e-.



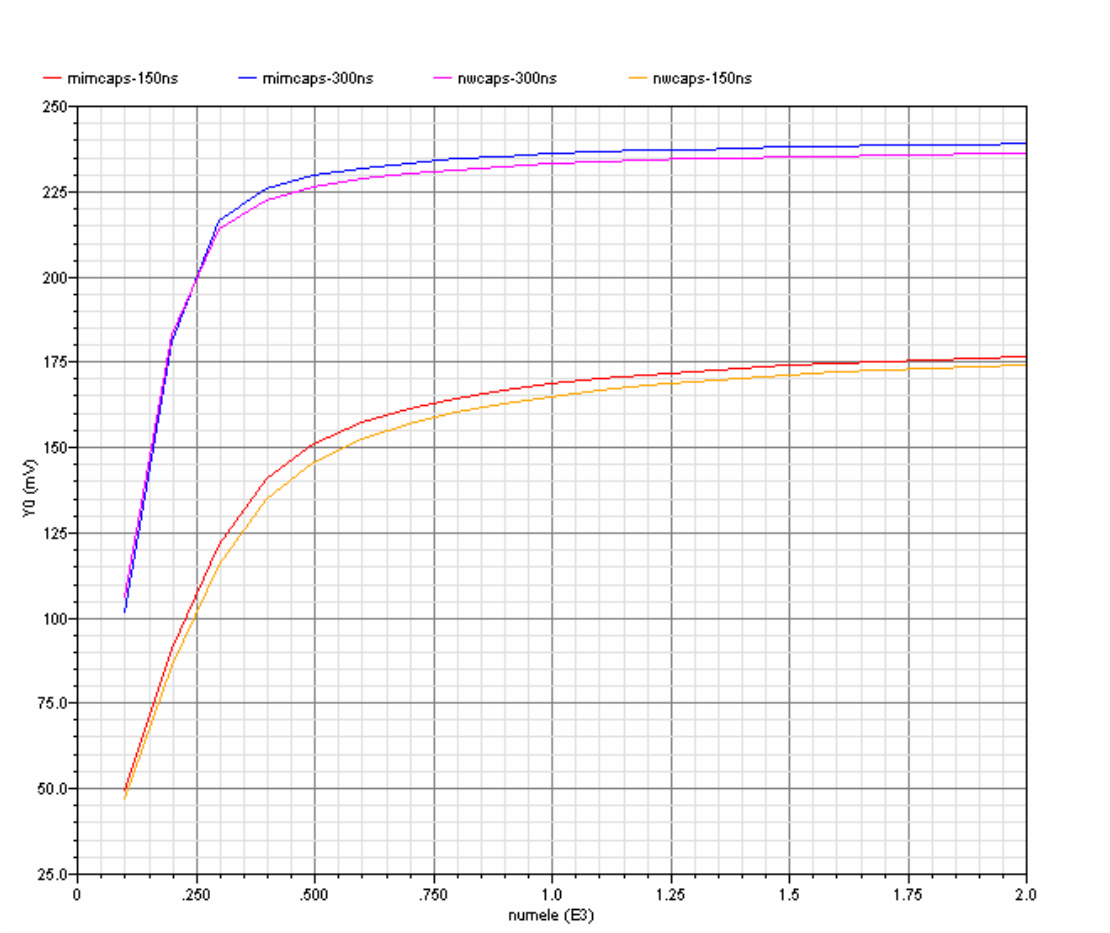

Above: The curves are simply a measure of the time taken for the voltage at the comparator input to reach the equivalent level of 350 electrons.

The time-to-threshold has increased slightly but is close enough not to be of concern. This is most likely due to the effective trade-off between speed and gain.

## *PreSample Pixel simulation: Typical Signals (400→8000e-)*

The input signal (per diode) is swept from 400 to 8000 electrons. The signal magnitude is plotted to check linearity.

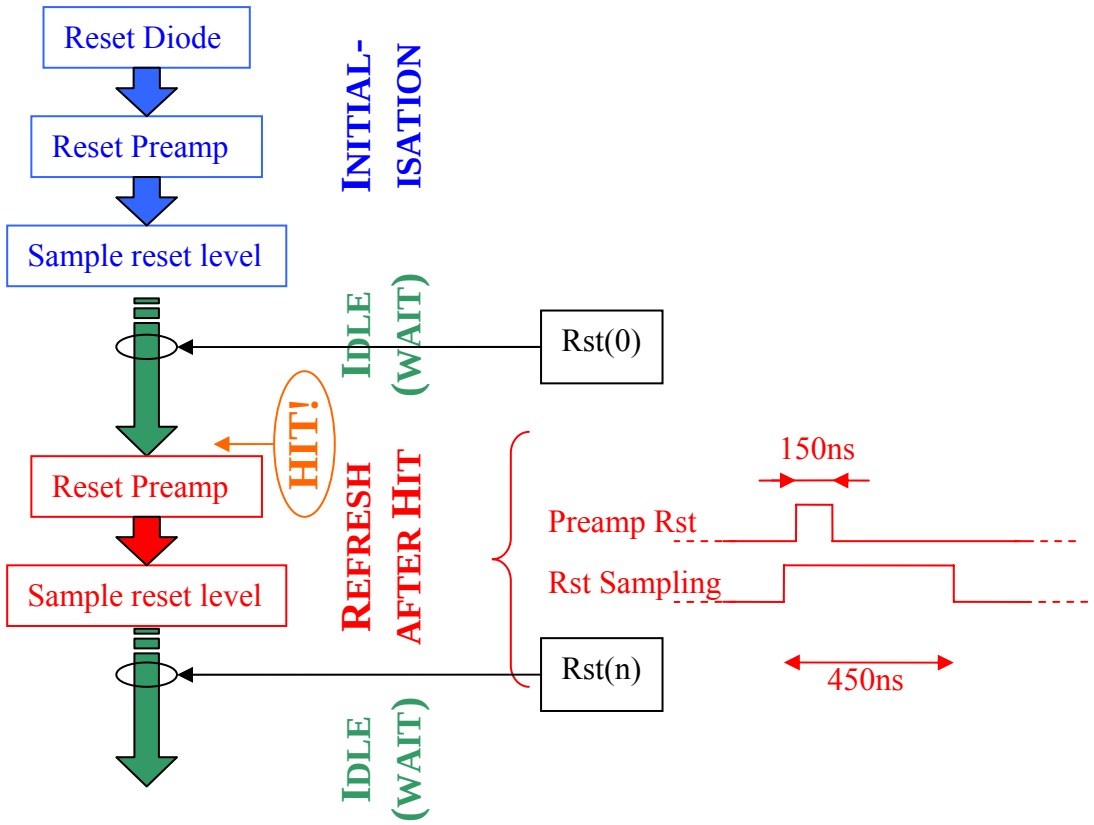
### Results Waveforms

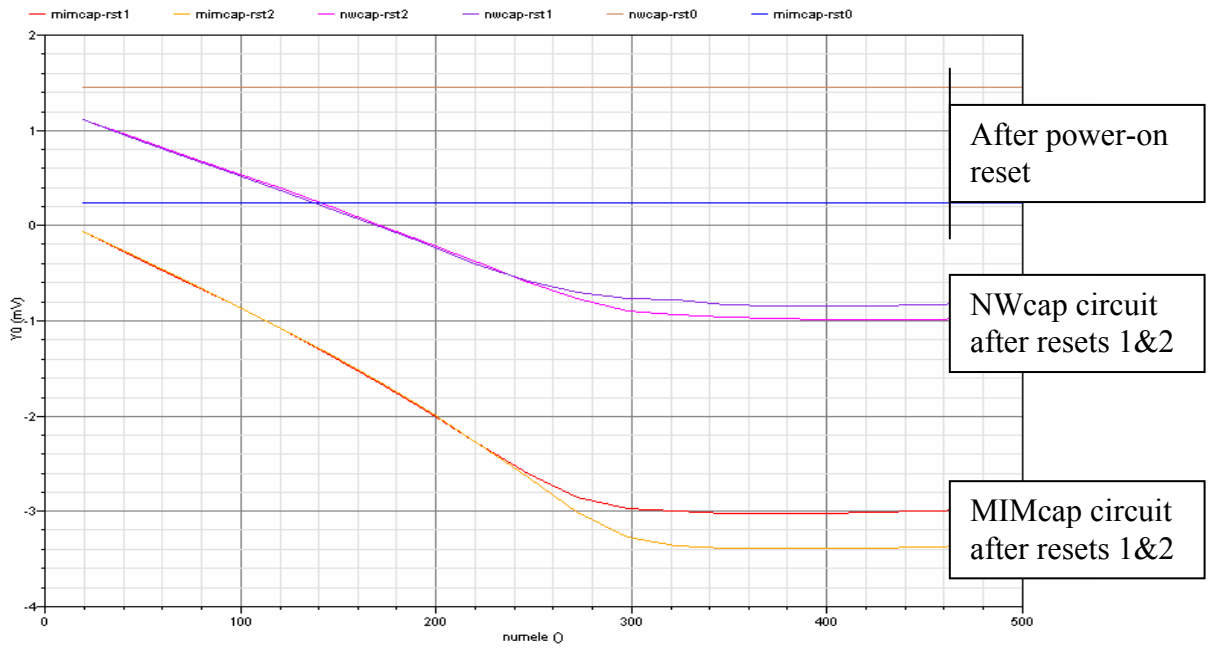



Above: Signal magnitude is presented at 150ns and 300ns delay from hit time where the reset has been omitted – in normal operation the channel reset would be applied thus preventing the full signal magnitude to develop. The pixel performance with MIM and NW capacitors is shown to demonstrate their equivalent behaviour.

The "numele" variable represents the charge on <u>each</u> diode.

## *PreSample Pixel simulation: Reset Sampling Errors*




Above: Error between reset and signal value taken 2us after reset has occurred. The original and new circuit configurations are seen to demonstrate different but similar performance during reset.

## *PreSample Pixel simulation: Noise Analysis*

MIM caps

```
/I4orig/M1      fn        0.00300831              28.72
/I4orig/M3      id        0.00280573              24.98
/I4orig/M1      id        0.00259437              21.36
/I4orig/M3      fn        0.00180369              10.33
/I4orig/M2      id        0.00144082              6.59
/I4orig/R0      rn        0.000804504             2.05
/I4orig/M5      fn        0.000630488             1.26
/I4orig/M5      id        0.000629623             1.26
/I461/M110      id        0.000480986             0.73
/I461/M33       id        0.000432606             0.59
/I4orig/M2      fn        0.000406598             0.52
/I4orig/M8      id        0.000190777             0.12
/I461/M110      fn        0.000167653             0.09

Integrated Noise Summary (in V) Sorted By Noise
Contributors
Total Output Noise = 0.00561325
Total Input Referred Noise = 0.0536571
The above noise summary info is for noise data
```

8mV

NW caps

```
Device          Param     Noise Contribution    % Of Total
/I484/M1        fn        0.00306184            28.45
/I484/M3        id        0.00290777            25.66
/I484/M1        id        0.00259347            20.41
/I484/M3        fn        0.00187072            10.62
/I484/M2        id        0.00144032            6.30
/I484/R0        rn        0.000906133           2.49
/I484/M5        fn        0.000655331           1.30
/I484/M5        id        0.000652525           1.29
/I461/M110      id        0.000498515           0.75
/I461/M33       id        0.00043282            0.57
/I484/M2        fn        0.000413832           0.52
/I484/M8        id        0.000210268           0.13
/I461/M110      fn        0.000173886           0.09

Integrated Noise Summary (in V) Sorted By Noise
Contributors
Total Output Noise = 0.00574041
Total Input Referred Noise = 0.0531078
The above noise summary info is for noise data
```

8.1mV

The dominant noise sources and totals are seen to be consistent between the two cases.

MIM caps

Applying the √2 factor and referring to the input assuming 313µV/e- gives:

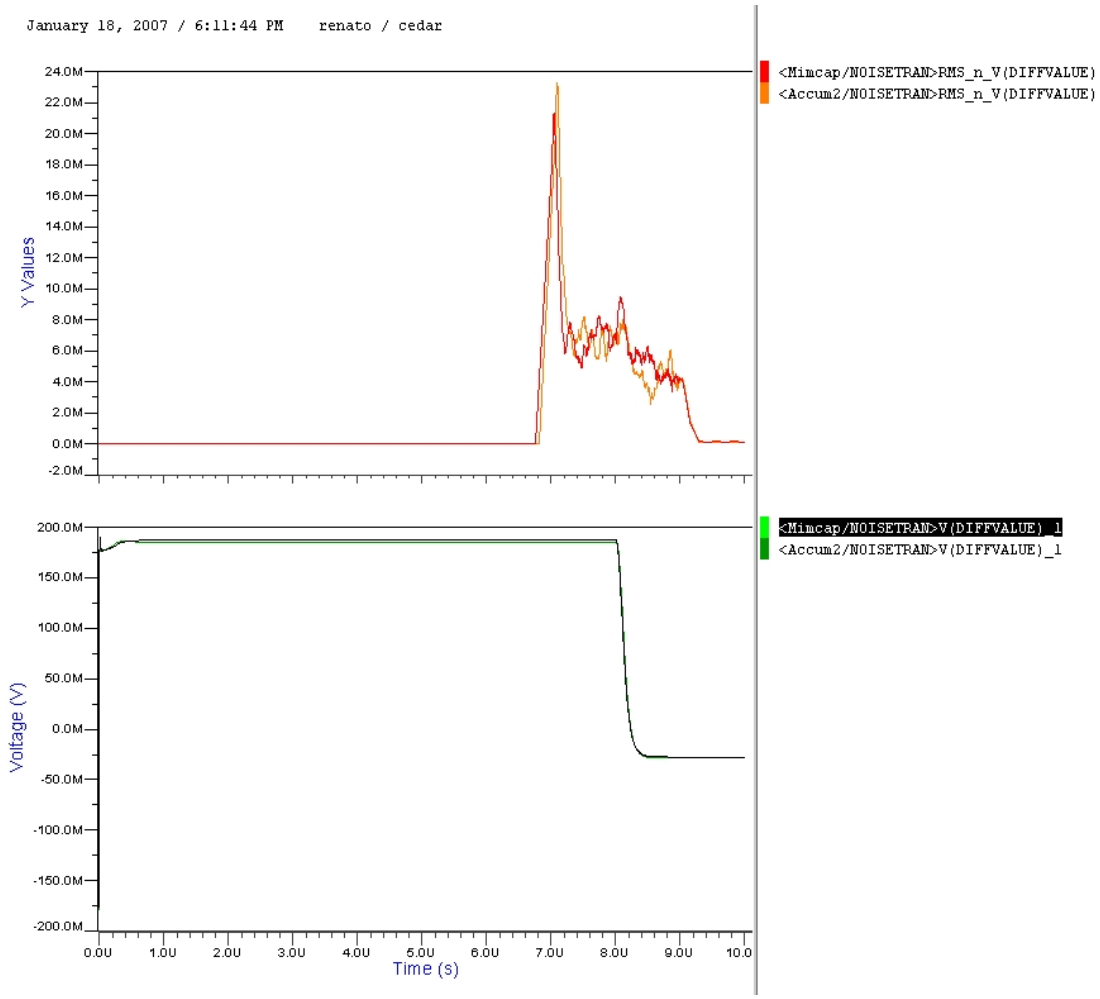
**25.6e- equivalent noise charge.**

NW caps

Applying the √2 factor and referring to the input assuming 337µV/e- gives:

**24.1e- equivalent noise charge.**

## Eldo Results




Above : The Eldo noise simulation results for the mimcap and nwcap circuit configurations show consistent noise performance.