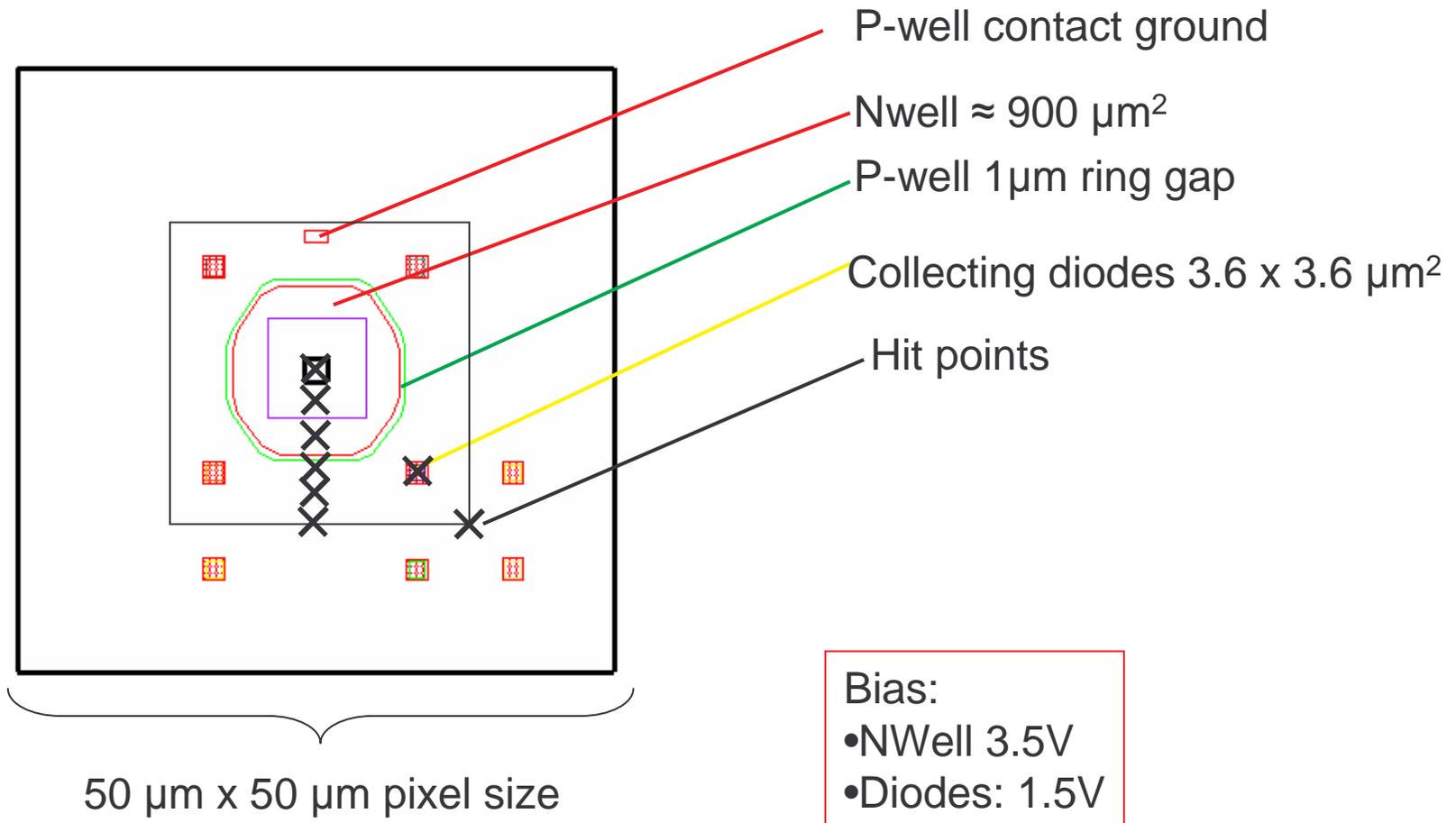
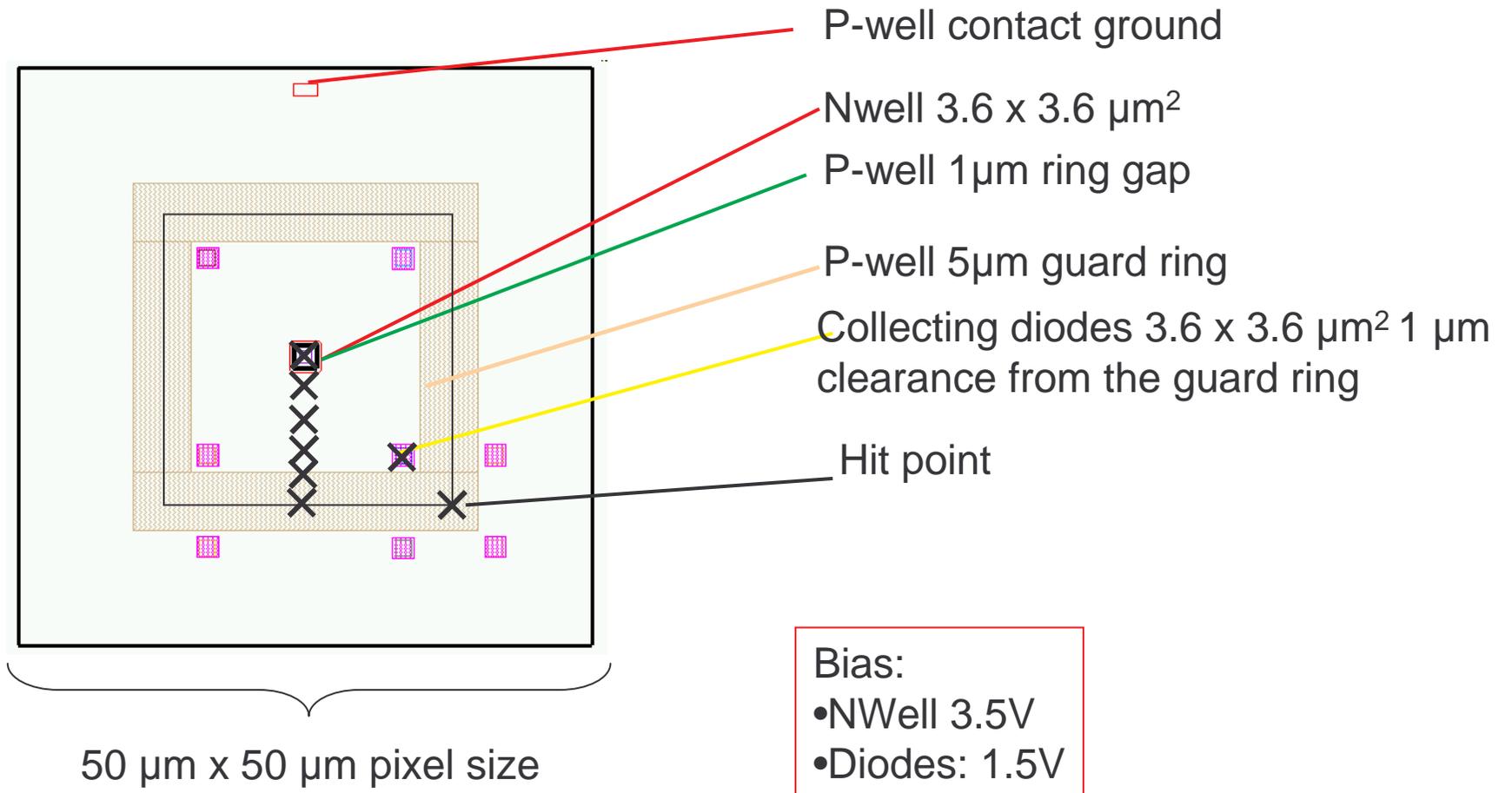


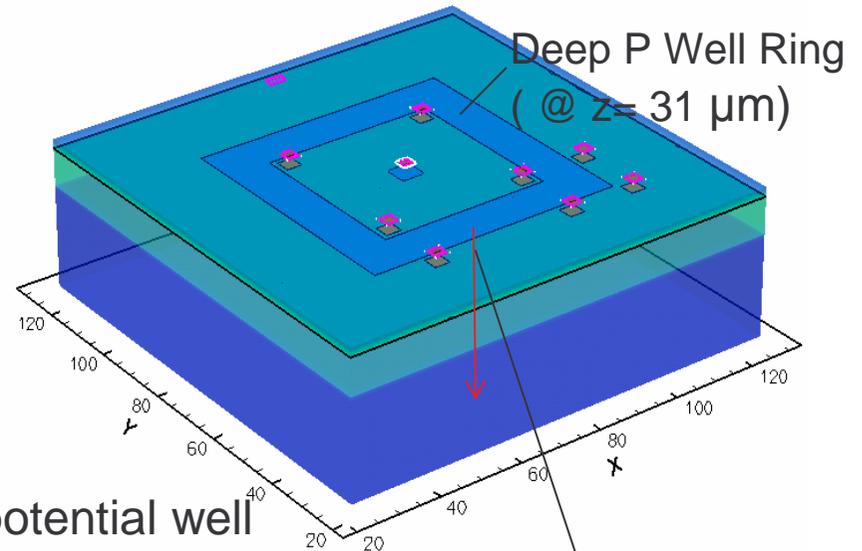
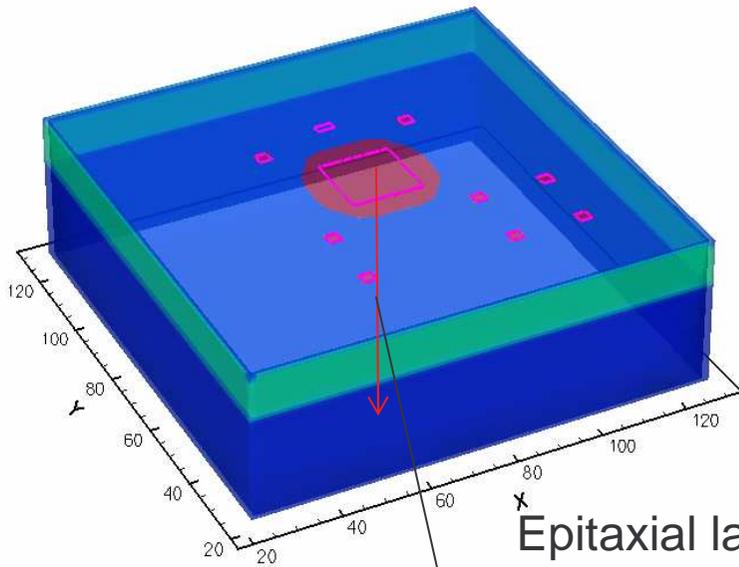
CALICE pixel Deep P-Well results



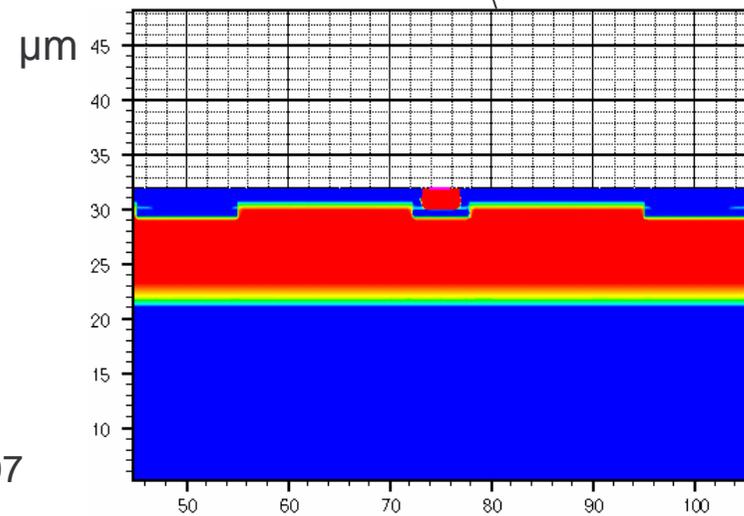
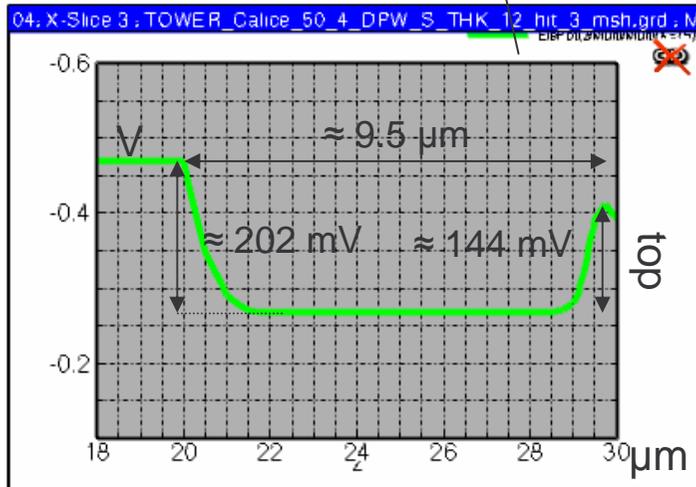
CALICE pixel Deep P-Well results



CALICE pixel Deep P-Well results



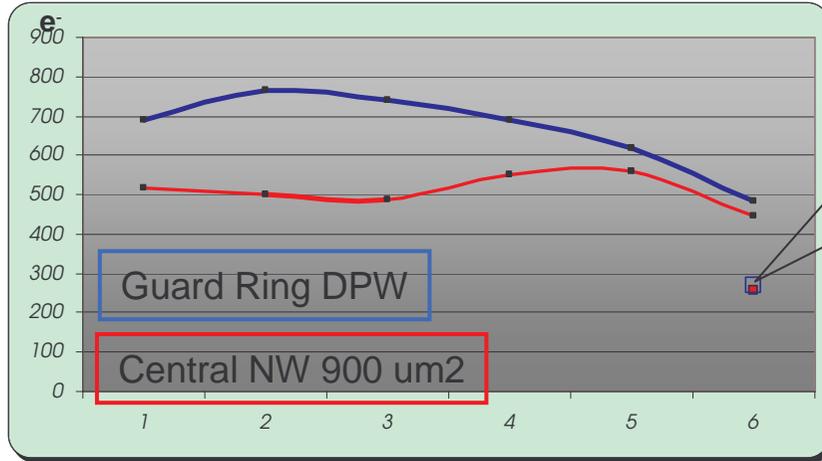
Epitaxial layer potential well



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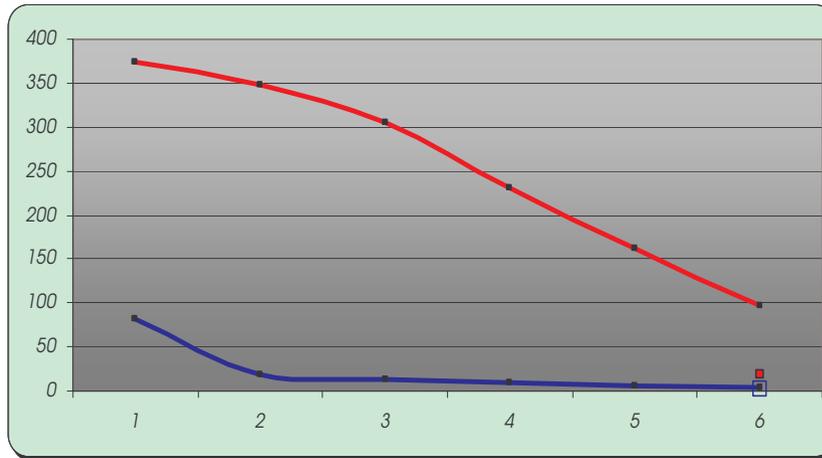
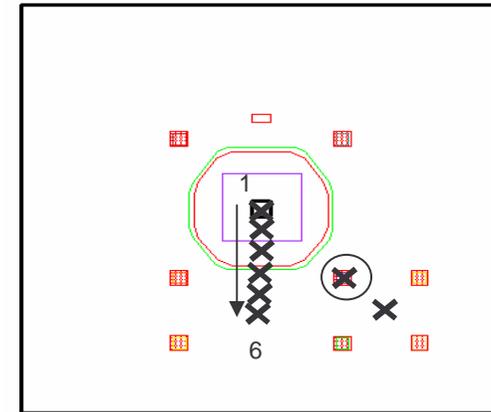
CALICE pixel Deep P-Well simulation results

Single pixel results Pwell Guard ring and CNW comparison

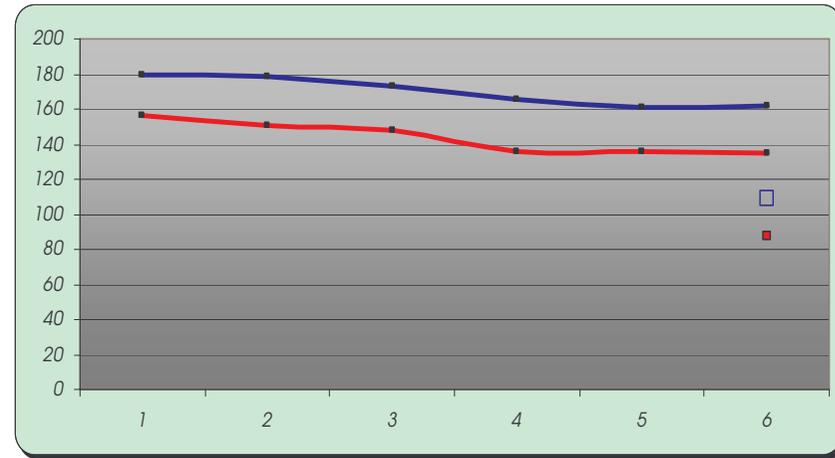


Diodes Charge collected (e⁻)

CNW: 257 (e⁻)
GR: 268 (e⁻)



CNW Charge collected (e⁻)



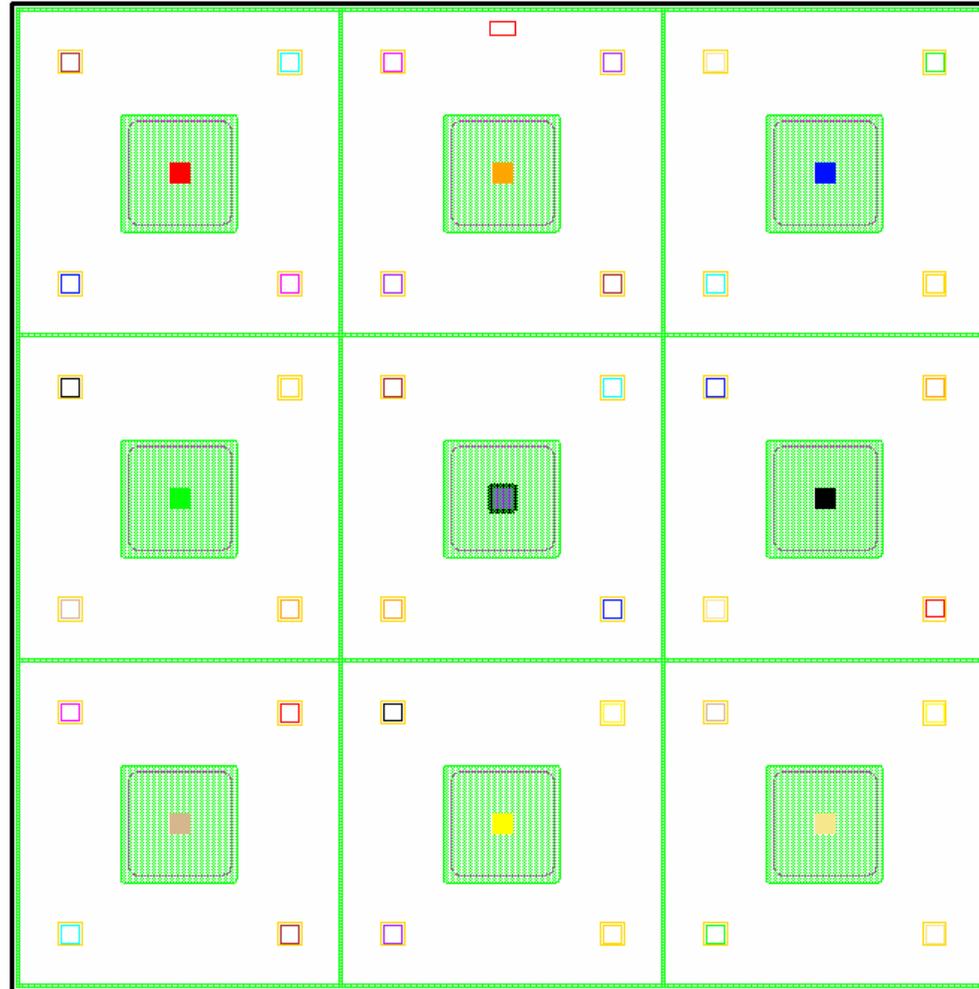
Collection time (ns)

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CALICE pixel Deep P-Well results

- **Conclusions**
- The layout with central well size $900 \mu\text{m}^2$ clearly shows worse performances in terms of charge collection compared to the guard ring PW: however the worst cases seem comparable, suggesting a S/N_{min} exceeding 10 in both cases
- Collection time still well below 200 ns in both cases, with central NW $900 \mu\text{m}^2$ faster than the guard ring PW.
- Shielding effect P Well Guard ring has to be assessed with reference to similar layouts: no NW strips WERE present in the $5 \mu\text{m}$ guard ring layout, that might affect charge collection by the diodes.
- **Next step:**
- Final layout simulation with and without $3 \mu\text{m}$ PW guard ring and proper biasing
- Different size diodes simulations ($7.6 / 1.8 \mu\text{m}$)

CALICE pixel Deep P-Well results



Narrow (3 μm ?) P-Well guard ring around each pixel

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