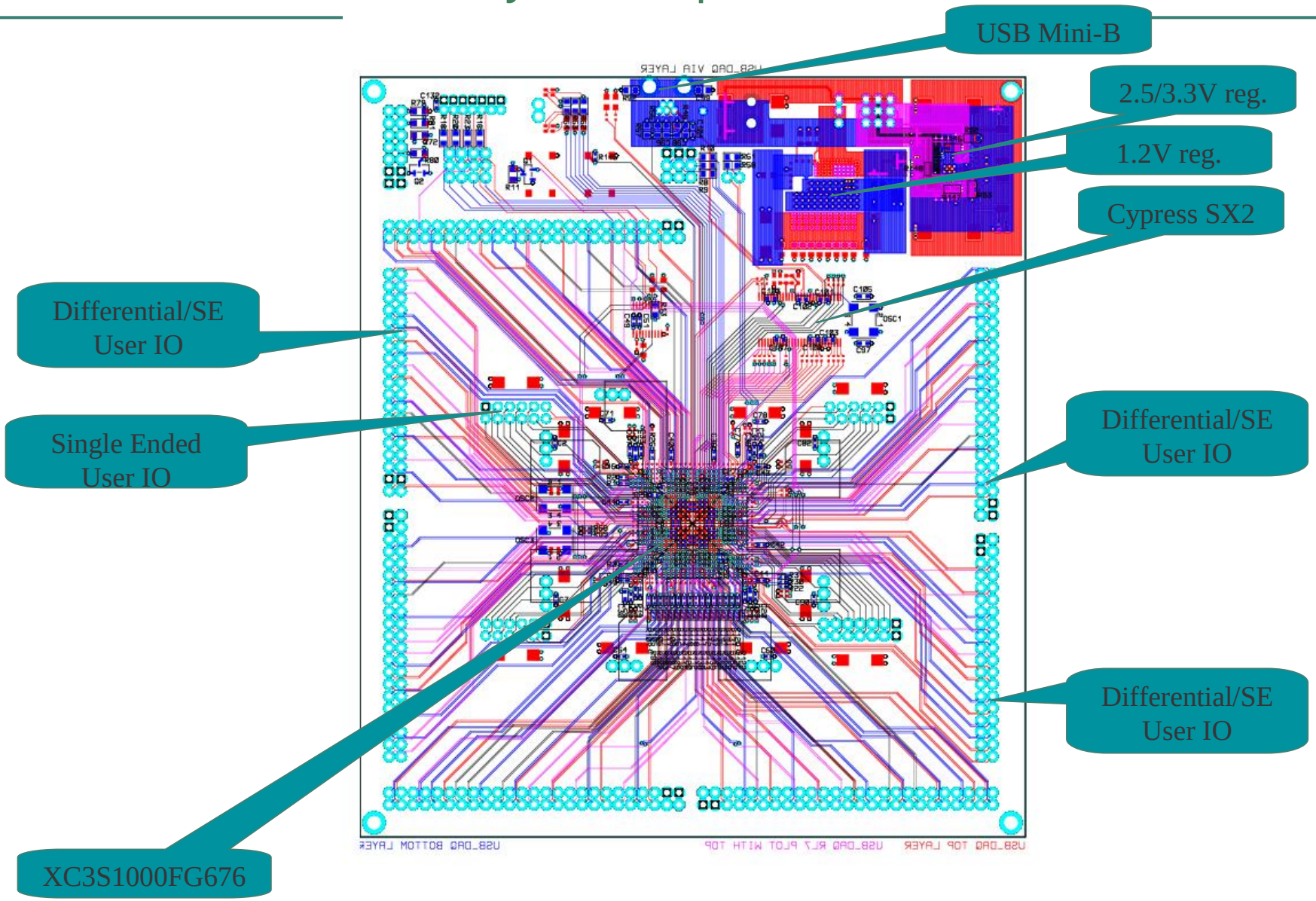
# CALICE MAPS DAQ Project Summary

# USB DAQ

- Generic Lab. Tool/DAQ board
  - Purely Digital
  - USB 2.0 interface
  - Digital Power
    - 1.2v, 2.5v (VCCAUX is separate),3.3v
  - 40MHz and 100MHz Oscillators on board
  - Xilinx Spartan 3 xc3s1000 fg676 –5
    - In use already in IC HEP (I-ImaS, CMS GCT, T2K)
  - IO: All Spare IO tracked to 0.1” IDC headers
    - Differential pairs tracked
      - 138 Pairs (=276 pins), 3 pairs are GCLK
    - Single ended IO separate
      - 41 pins
    - Total: 317 user IO
  - Bank VCCO individually jumper controlled
- PCB here now
  - 5 have been manufactured
- 2 have been sent for assembly
  - should be back by the end of next week
- Sensor Mount Card being handled by Birmingham
  - Sensor mount card interface will probably be done through cables initially
- Development of a memory card with ~2MBytes for bulk storage
- Also need a NIM -> cmos conversion

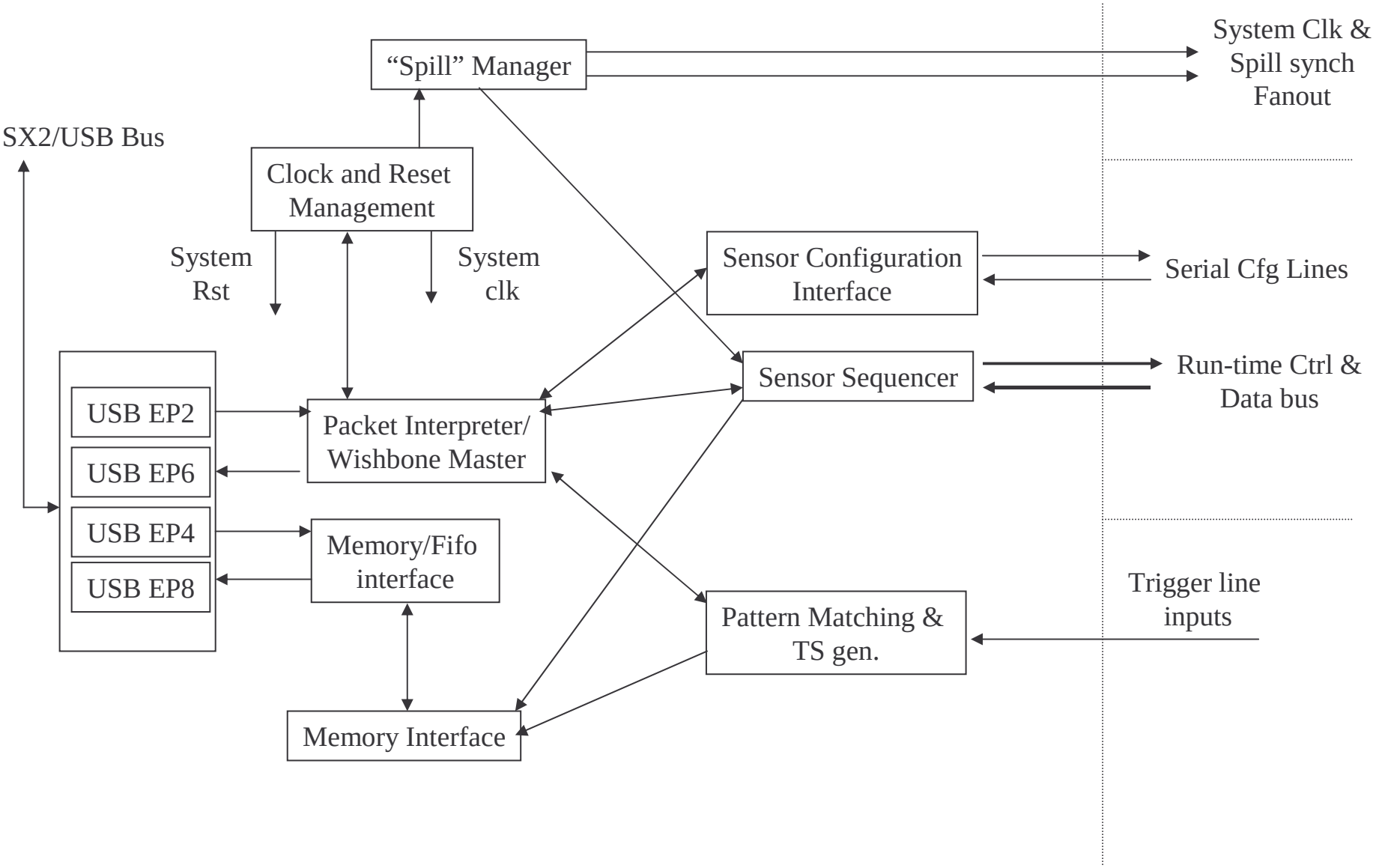
# Layout Snapshot



# Firmware

- HW design draws on existing IC experience
  - Have interface firmware for the SX2
    - Corresponding software also exists (more in a moment)
  - 4 end points; 2 in, 2 out
  - Logically divided into 2 pairs
    - 1 pair raw data block transfer
    - 1 pair has packet structured that maps to 16 bit R/W address space over a wishbone bus.
  - Wishbone bus forms configuration, trigger and status framework
  - Raw pipes do bulk DAQ.
  - This is already in use in IImaS, CMS GCT, T2K
- Will develop sensor CFG interface module, run-time controller and data capture
- Additionally, a trigger pattern matching module and time-stamp generation system.

# Firmware


"Spill" Manager
System Clk & Spill synch Fanout
SX2/USB Bus
Clock and Reset Management
System Rst
System clk
Sensor Configuration Interface
Serial Cfg Lines
Sensor Sequencer
Run-time Ctrl & Data bus
USB EP2
USB EP6
USB EP4
USB EP8
Packet Interpreter/ Wishbone Master
Memory/Fifo interface
Trigger line inputs
Pattern Matching & TS gen.
Memory Interface

# Software

- Lowest layer is HW access
  - Set of c++ classes that access the EPs as discussed before
  - Closely matches the FW
  - Already in use in IImaS, CMS GCT, T2K
- Next layer up will match the project-specific FW
  - This will be developed/debugged alongside the FW
- Above this there will be operation control, monitoring and display
  - Will use either QT or ROOT
- This system will run on Linux
- Data management
  - Probably develop custom binary format to remain independent of ROOT/LCIO etc.
- External system interfaces done through the network
  - Define some protocol for control and status monitoring