Tera-Pixel APS for CALICE

Progress meeting, 31st August 2007

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Test progress

(predicted)

ID	Task Name	% Work Complete	Duration
1			
2	Power-on PCB with no chip	100%	4 days
3	Bonding ü	100%	5 days
4	Power-on PCB with bonded chip ü	90%	2 days
5	**Verify Shfit Registers** ü	**0%**	**3 days**
6	Fast shift reg top	100%	1 day
7	Slow shift reg (pix)	95%	1 day
8	Fast shift reg bott	100%	1 day
9	Verify Monostables !	75%	1 day
10	Verify pixel comparator ü	60%	2 days
11	Operate & verify test pixels	35%	3 days
12	Set up system for PPD	20%	5 days
13	Viable system ready for Marcel & Giulio	0%	0 days
14	Verify Configuration Programming ü	90%	4 days
15	Blind test (prove logic with pixels masked)	5%	5 days
16	Single column tests	0%	5 days
17	Full frame tests: Single shot	0%	3 days
18	Full frame test: N shot	0%	4 days
19	Full frame tests: Continuous run	0%	2 days
20	Set up systems for IC & Birmingham	0%	5 days
21	Viable systems ready for IC & Birmingham	0%	0 days
22			
23	Owen available	100%	9.53 days?
24	Michael (student) available	0%	25.53 days?
25	TWEPP Conference (1st results pub?)	0%	5.27 days?
26	Vertex 2007 (alt. results pub?)	0%	5.27 days?

turn on 13th Aug

â ~1 days

â ~1 day

Æ ~8 days

~1 day

~1 day

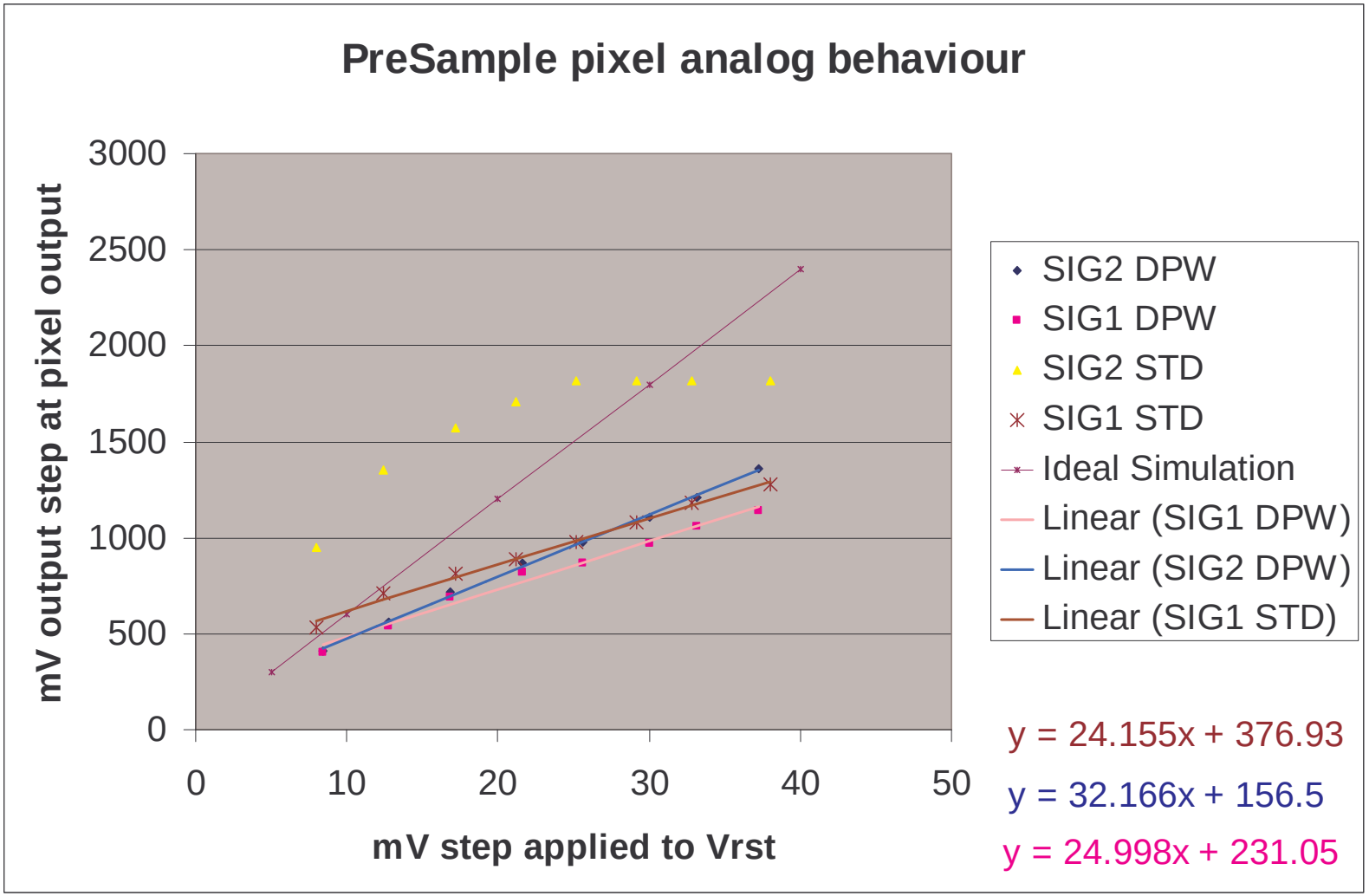
today 31st Aug

ß 4th September in my plan

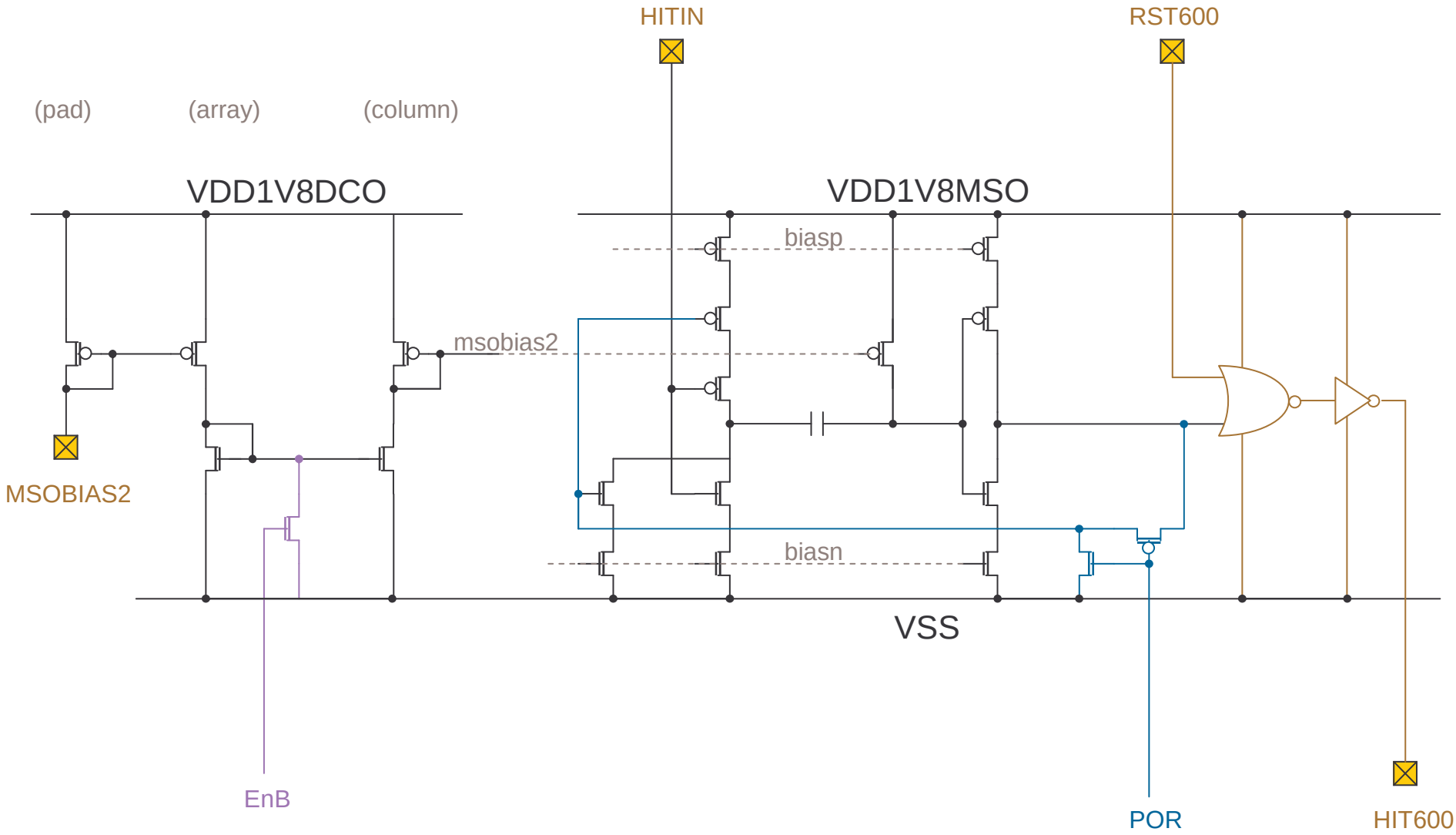
â ~1 day

~1 day

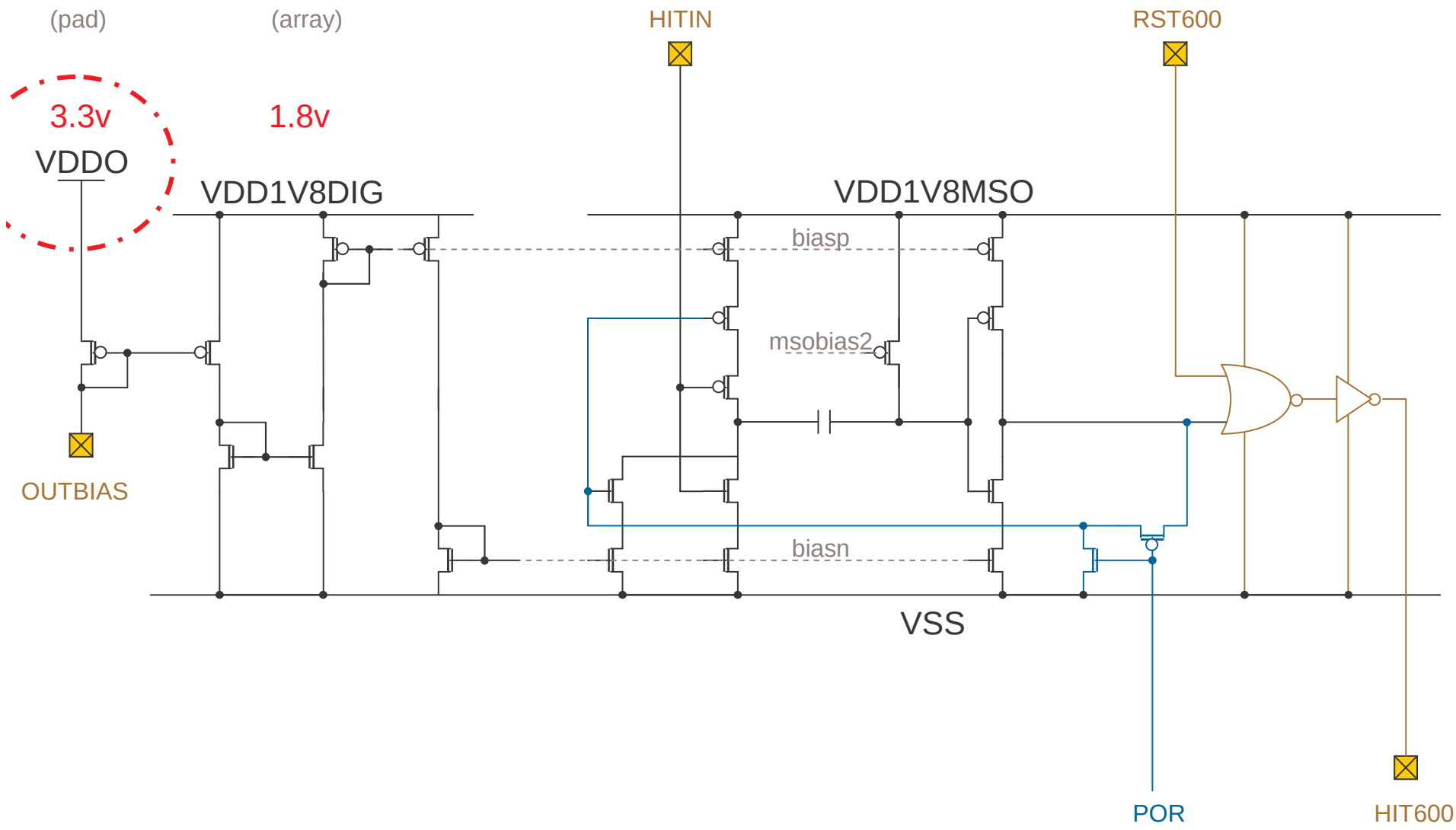
Pixel results: Very preliminary!



Monostable + bias

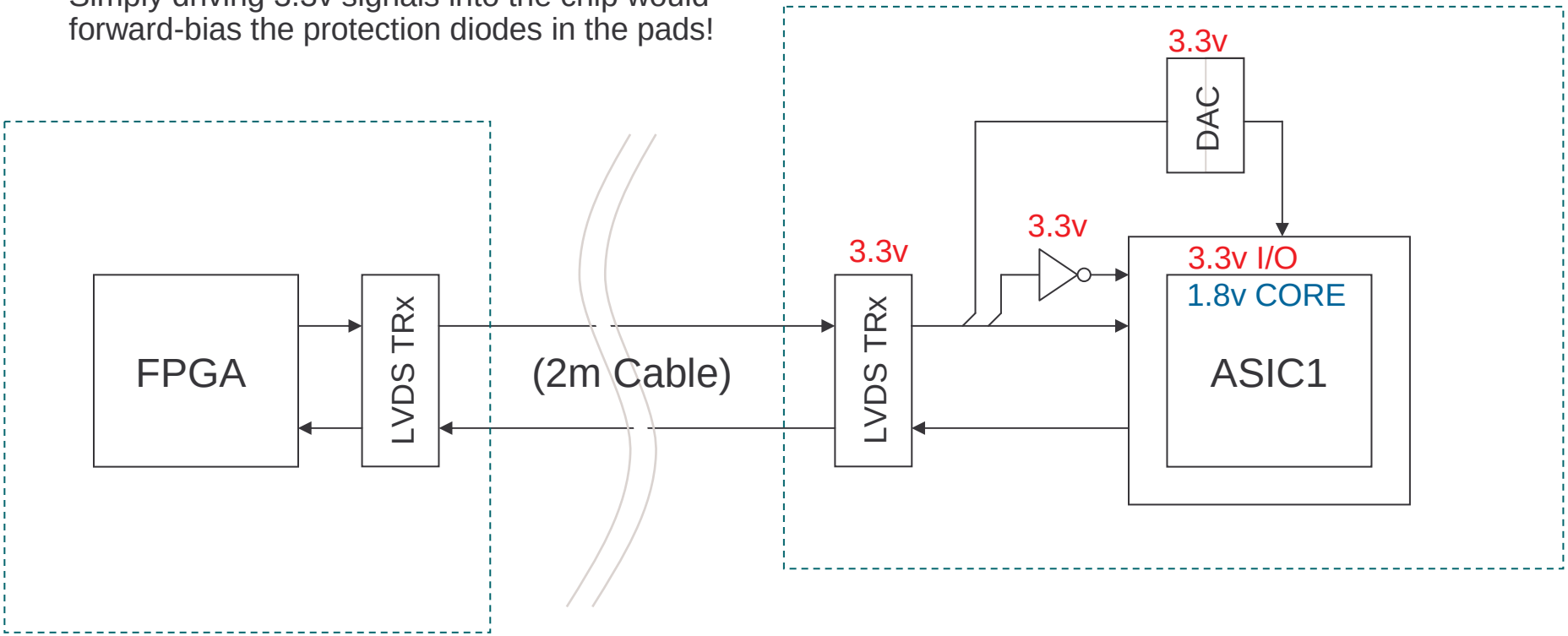


Monostable + current limit bias



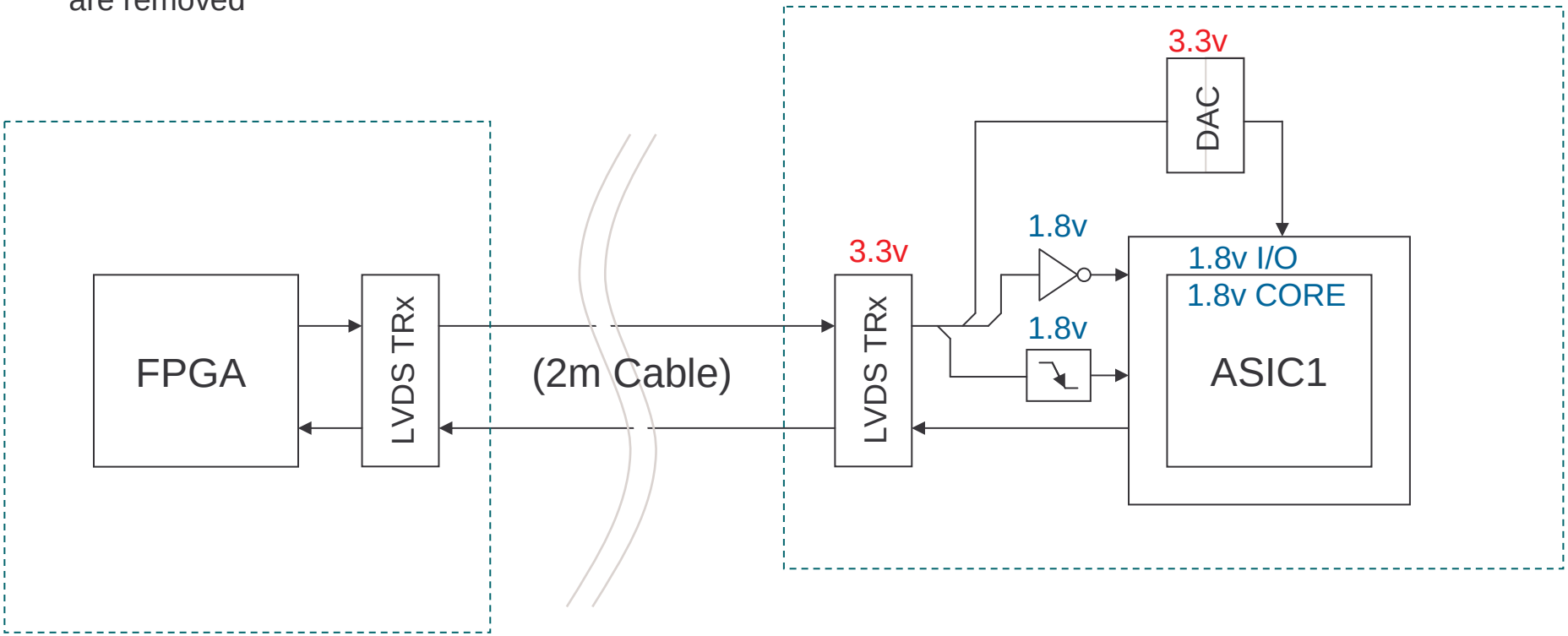
System overview

- Need to either
  - run chip I/O at ~1.8v
  - Correct the design so the I/O can be run at 3.3v and the bias chain still operated correctly
- Simply driving 3.3v signals into the chip would forward-bias the protection diodes in the pads!



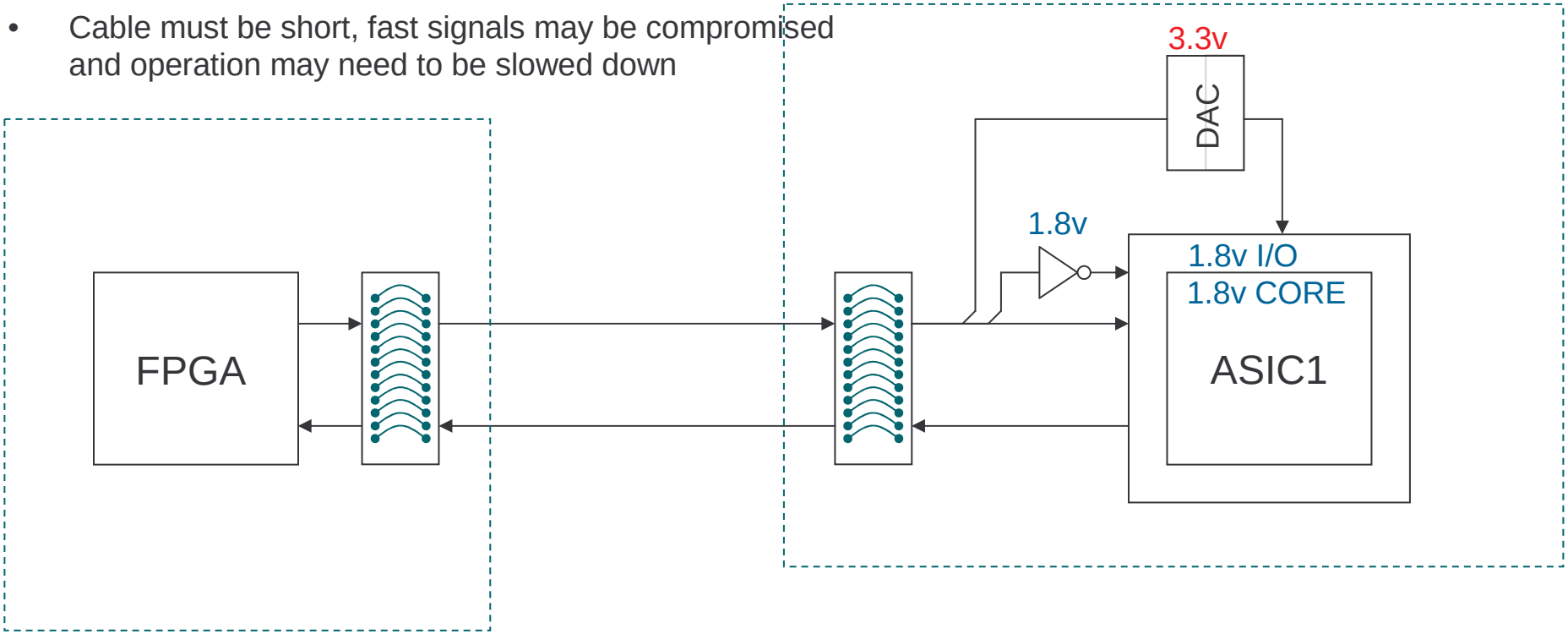
Option 1: Level Shifters

- Re-spin sensor card adding level shifting circuits,
  - Active
  - Passive (resistor divider)
- Card footprint can remain the same if LA connectors are removed



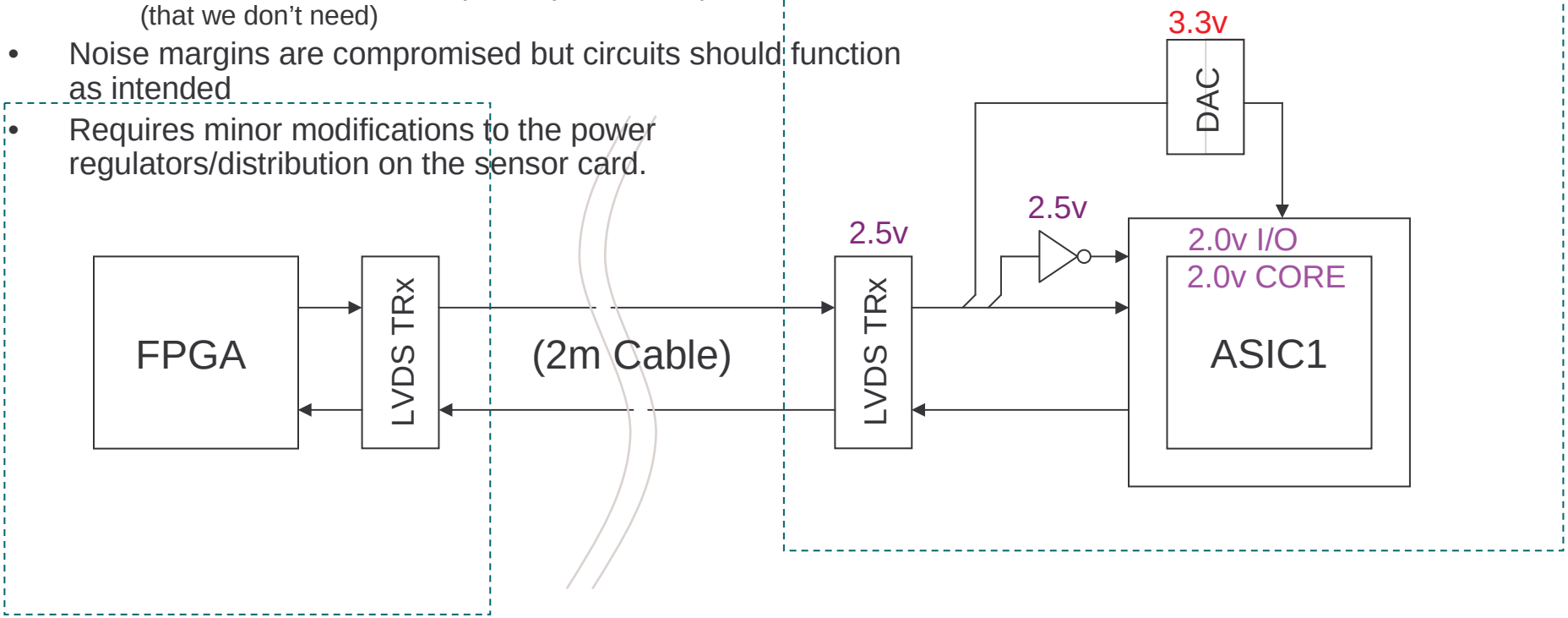
Option 2: Direct connection

- Remove LVDS transceivers on both boards
- Bond/solder across the footprint
- FPGA can work with single-ended outputs/inputs at 1.8v
- Cable must be short, fast signals may be compromised and operation may need to be slowed down



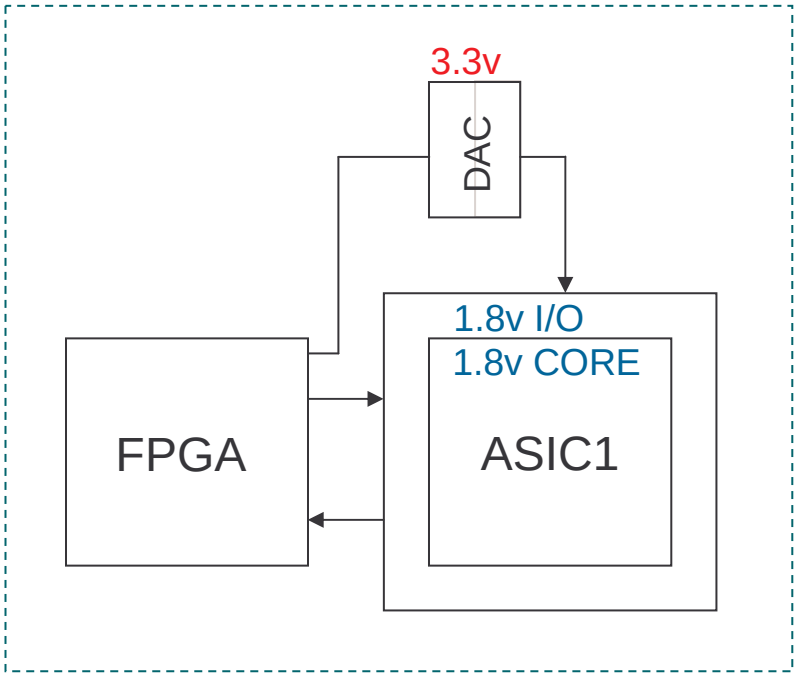
Option 3: Adjust power supplies

- Run the chip at 2v
  - Possible degradation to lifetime/reliability
- Run the LVDS and inverters at 2.5v
  - This is below the minimum supply (3v) stated in datasheet
  - Parts do work at >2.1v but probably not at full quoted data-rate (that we don't need)
- Noise margins are compromised but circuits should function as intended
- Requires minor modifications to the power regulators/distribution on the sensor card.



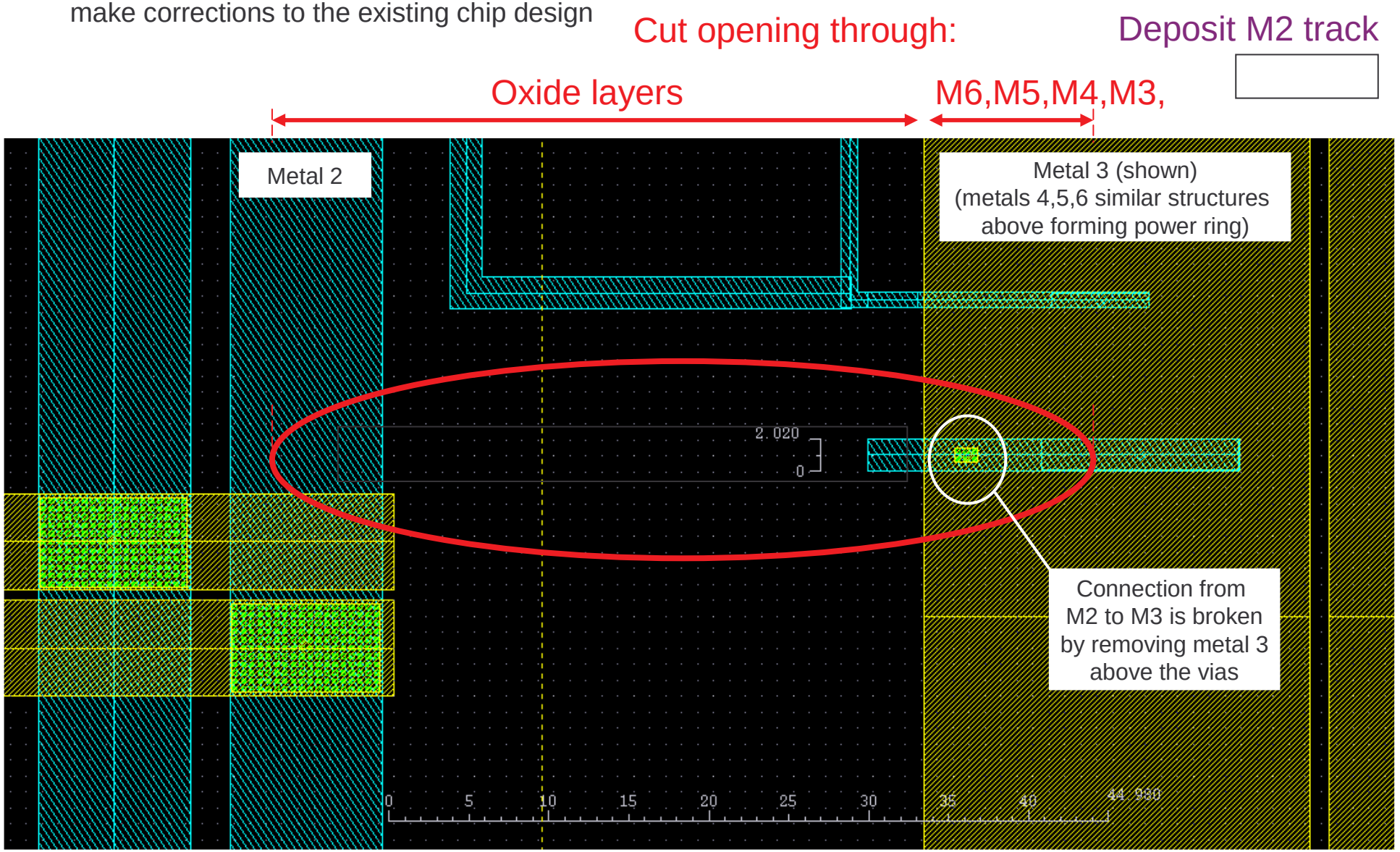
Option 4: Combined cards

- Re-spin FPGA daughter card to include the sensor footprint



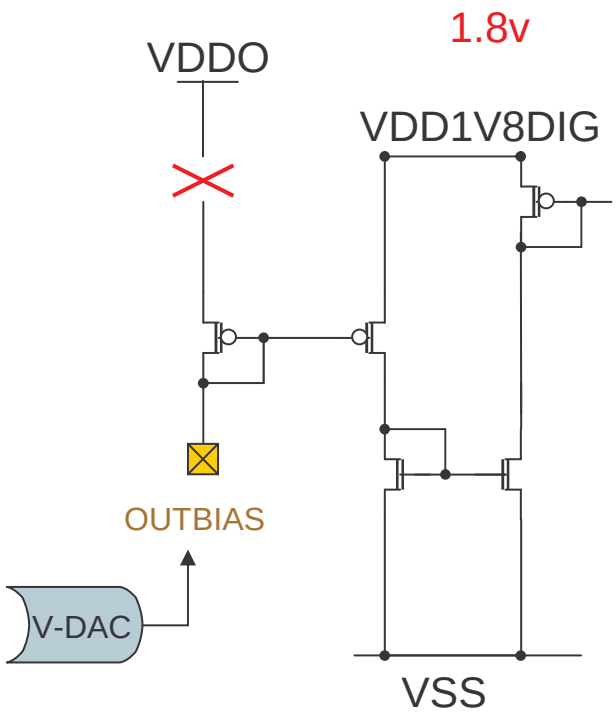
Option 5a: Die Modification

- Use laser or focussed ion beam (FIB) techniques to make corrections to the existing chip design



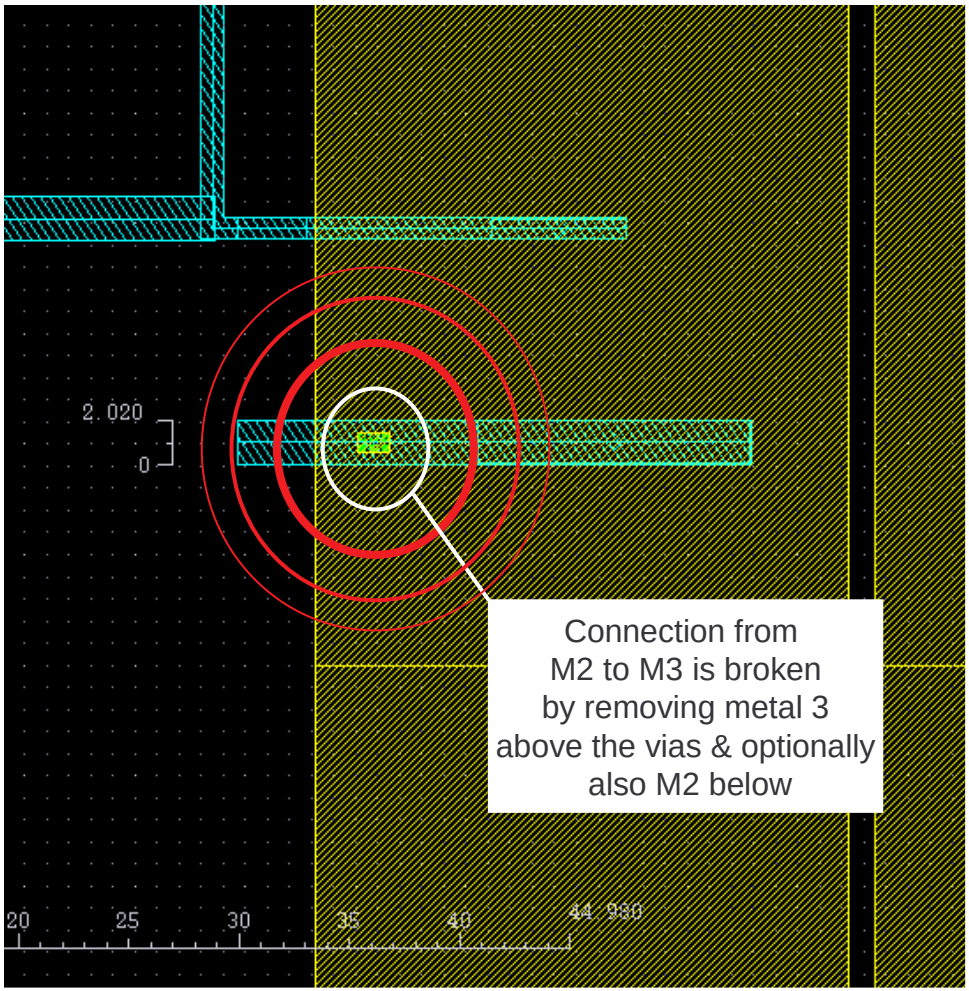
Option 5b: Die Modification

- Use laser or focussed ion beam (FIB) techniques to make corrections to the existing chip design
  - Remove connection to VDDO
  - Drive OUTBIAS with voltage DAC to give crude control of current flow – should be sufficient for this bias as it only limits current flow in logic cells.



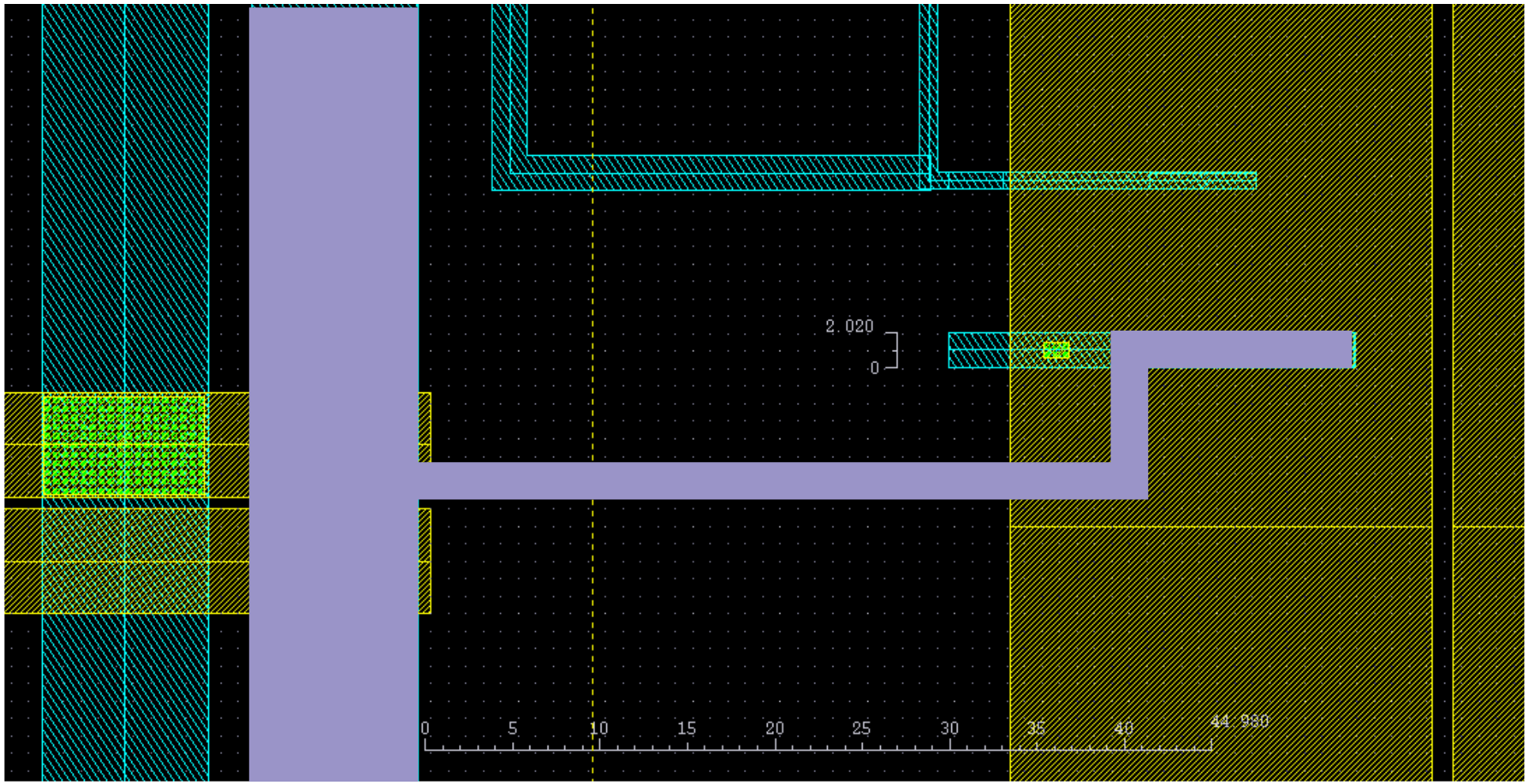
Cut ~10 micron access holes through M6, M5, M4, M3

(Cut ~5 micron dia. hole through M2)



Option 6: Design Modification

- Make changes to the design and re-fabricate
  - Single mask (M2) change



Summary of Options

		Sensor card	DAQ card	Cable	Timesacle	Cost
1	Level shifters	Re-design	No change	2m ok	~4 weeks?	
2	Direct connect	Modify existing	Modify existing	Minimum lengths only	~1 week?	
3	Adjust power supplies	Modify existing	No change	2m ok	~instant	
4	New FPGA+Sensor card	Abandon	Re-design	None	~4 weeks?	
5	Die modifications	No change	No change		~2 weeks?	(a) Quote requested (b) Giulio?
6	Design modify + re-fab	No change	No change		~8 weeks?	~$25K