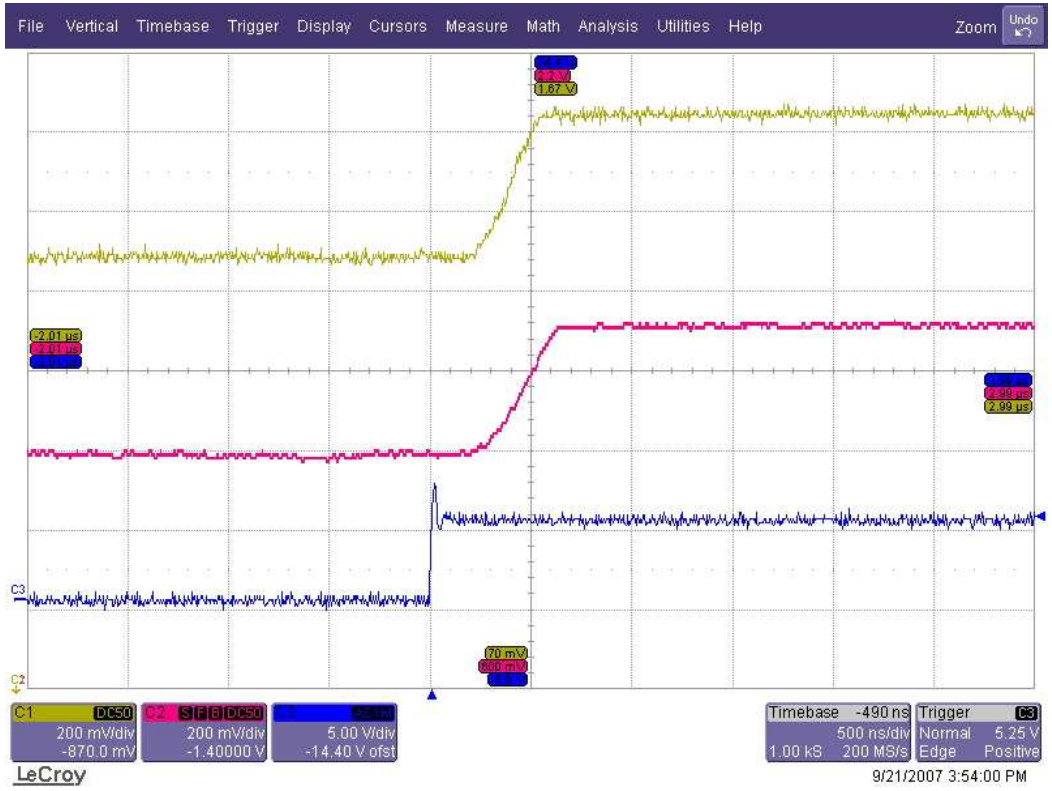
Tera-Pixel APS for CALICE

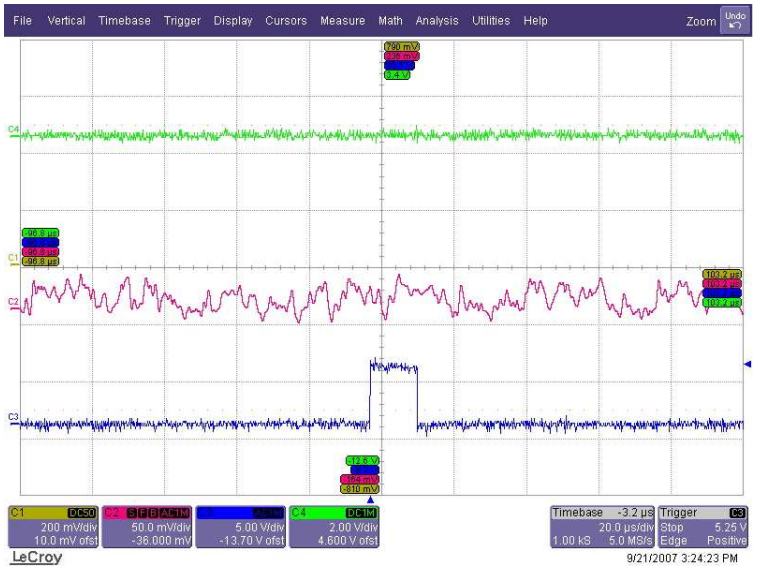
Progress meeting, 17th September 2007

Jamie Crooks, Microelectronics/RAL

Laser Testing



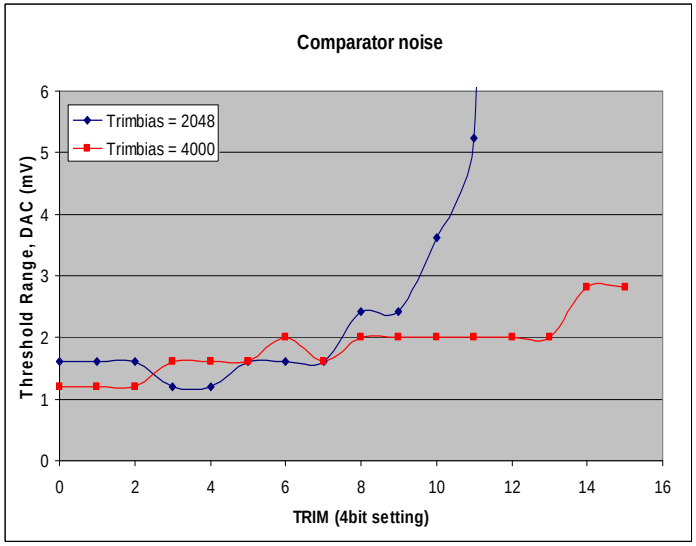
- Proof of life from both test pixels
- No obvious injection from laser itself

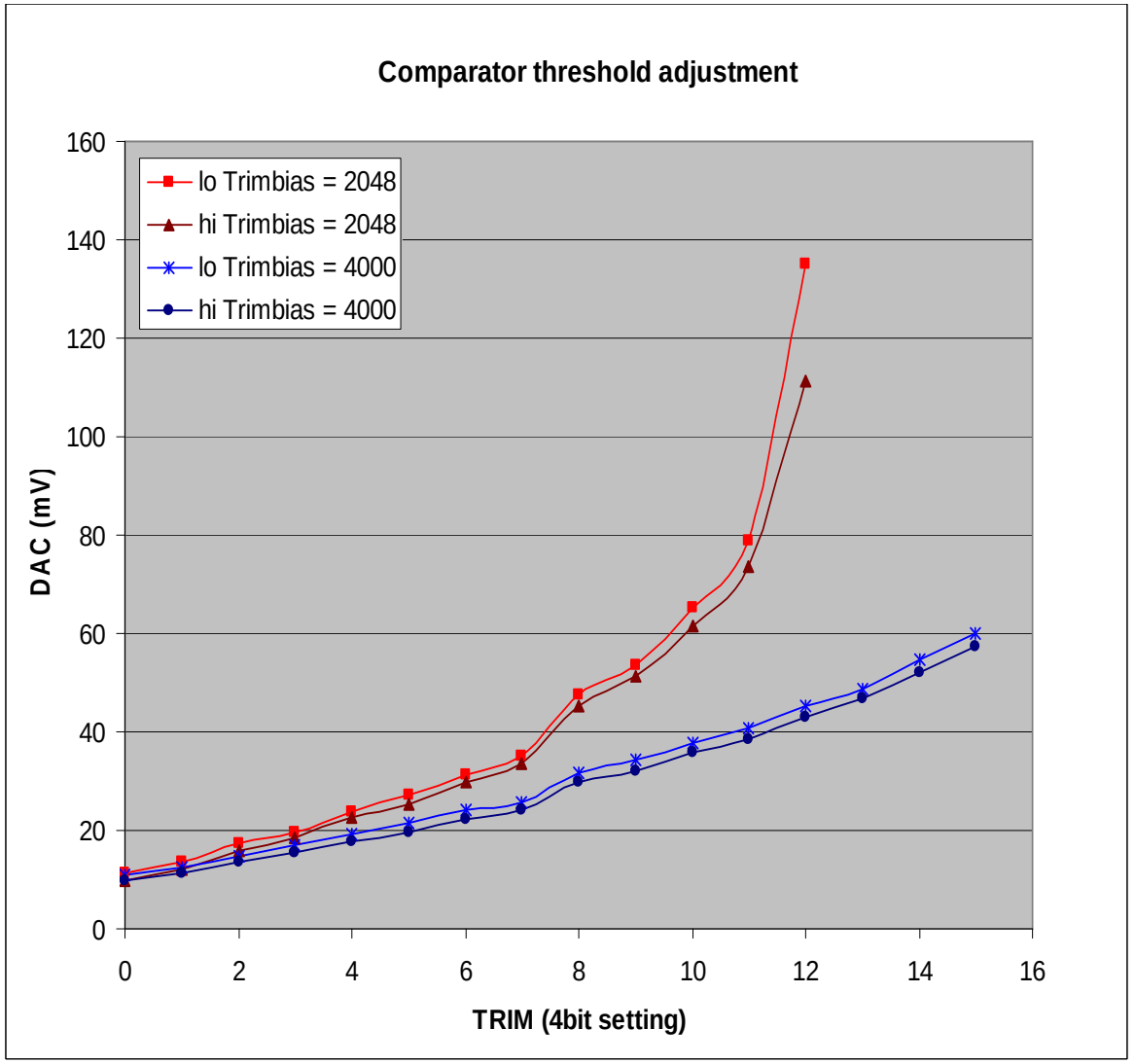


Comparator & Trim

- Comparator trim biases adjusted to give sensible step size
- Holding test pixel in reset (ie zero input), record switching threshold for each trim setting
- Upper and lower limit of switching point recorded:

NB: One DAC step ~0.4mV





Digital Logic

- SRAM problem reported last week is now understood
  - Sense biases adjusted (again) to properly operate sense amplifiers (read)
  - SRAM write is reliable at VDD2V5dig > 2.6v
    - 20mA -- 40mA static current in digital ground on-chip
- Noted useful characteristic
  - SRAM write of 1s requires 2.6v, write of 0s requires ~2.3v

- Workaround possibilities:

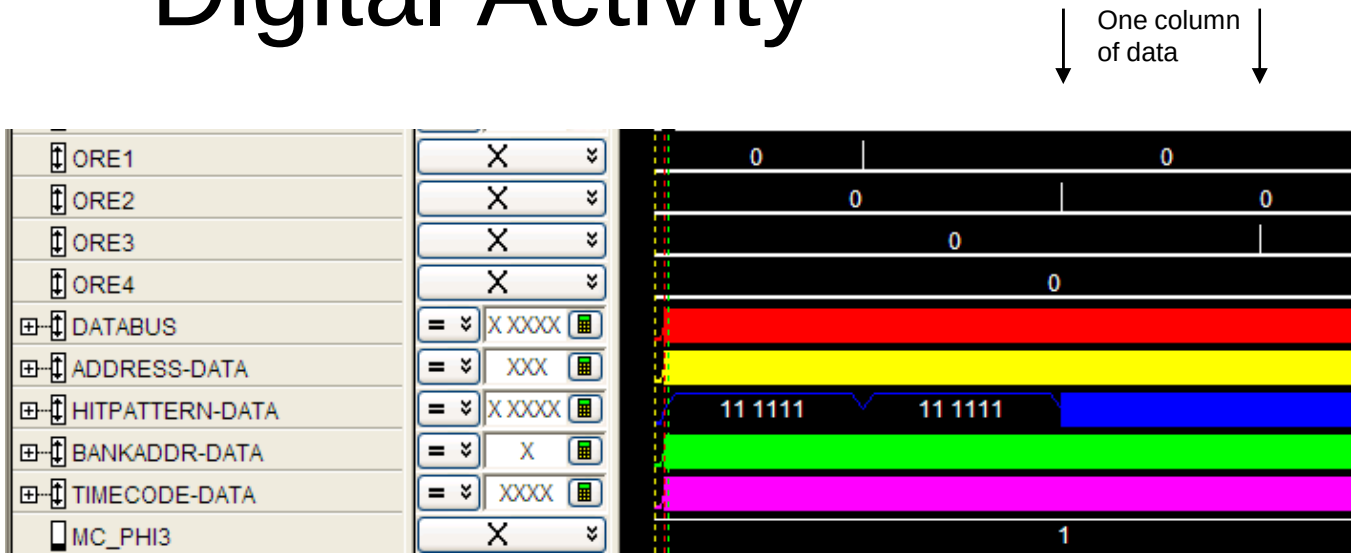
Run the sensor at 2.6v

- Does work
  - No software yet to evaluate performance
- Not ideal
  - Evidence that this raises the internal digital ground

"Reset" the SRAMs at 2.6v then switch to lower supply for normal operation

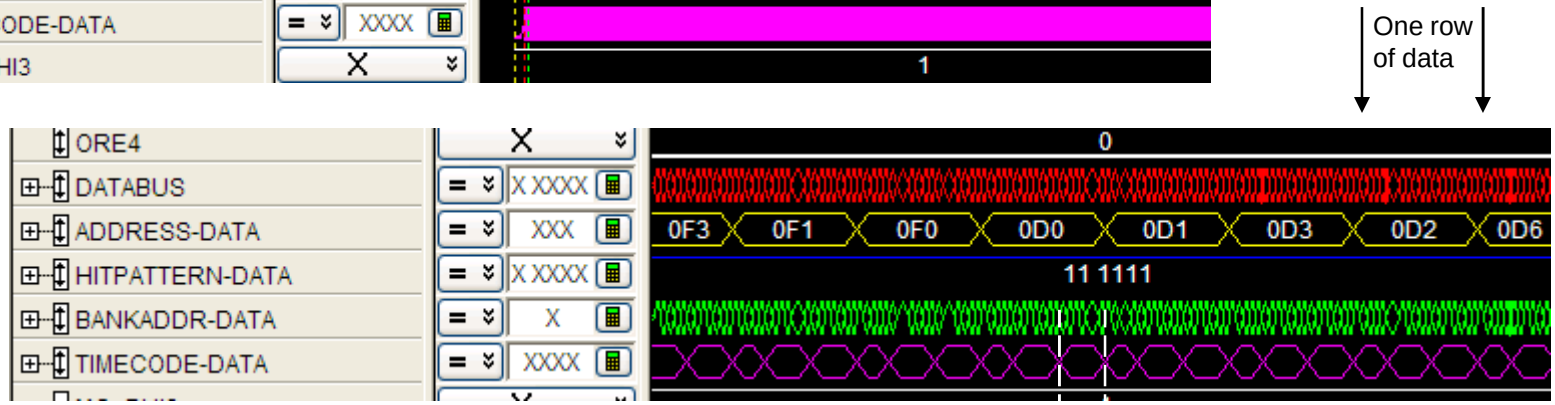
- Can use the spare DAC channel and transistor to supply current: Board mod TBC.
- Slow (software controlled DAC serial write) but only required once between each bunch train
- Requires longer in-spill timing (separation of MUX & clock signals) TBC

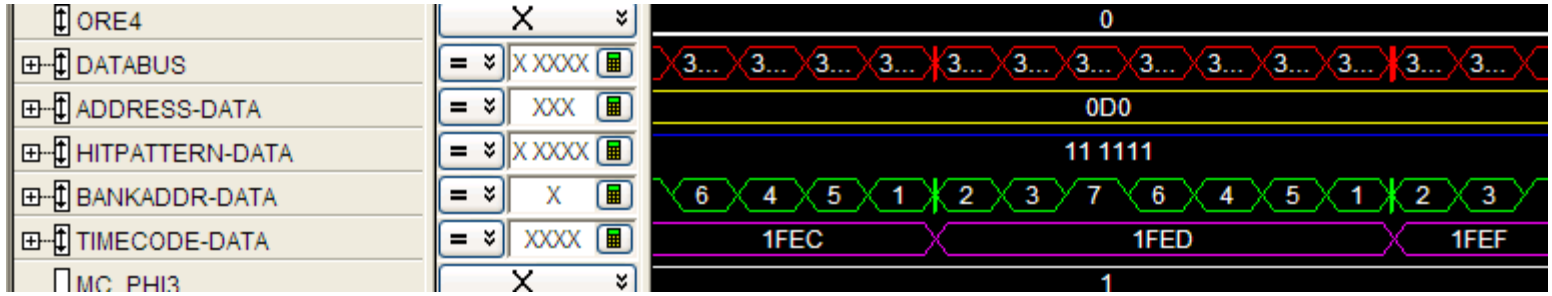
Digital Activity



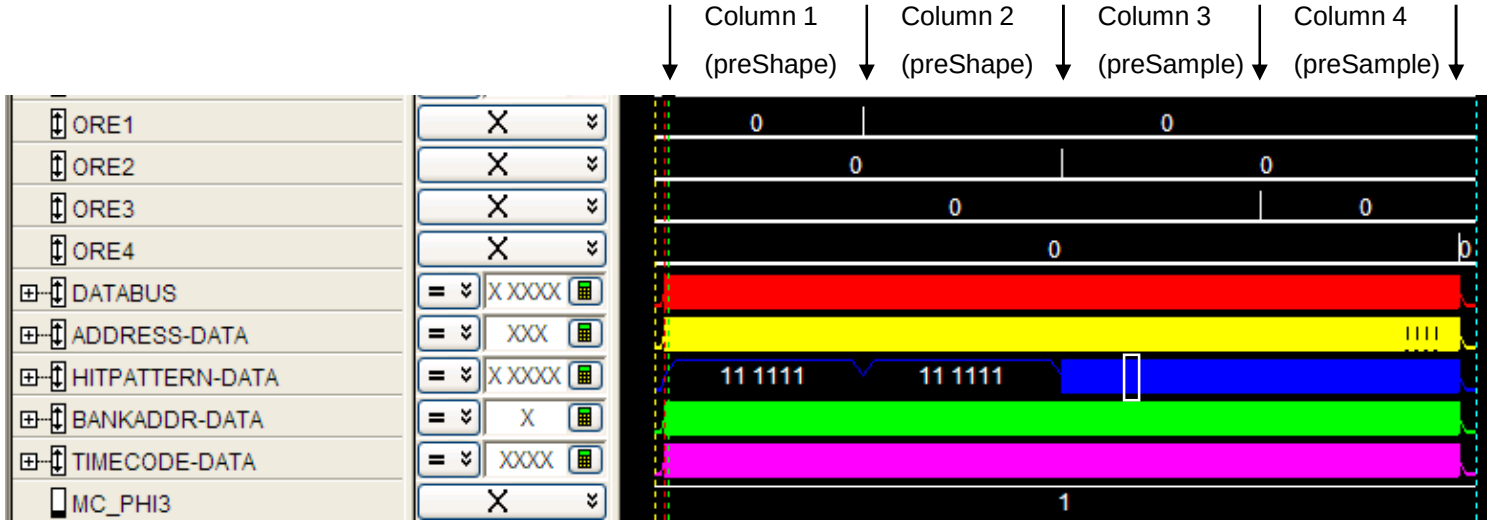
- Override mode generates a full memory of hits

(to be understood à next slide)

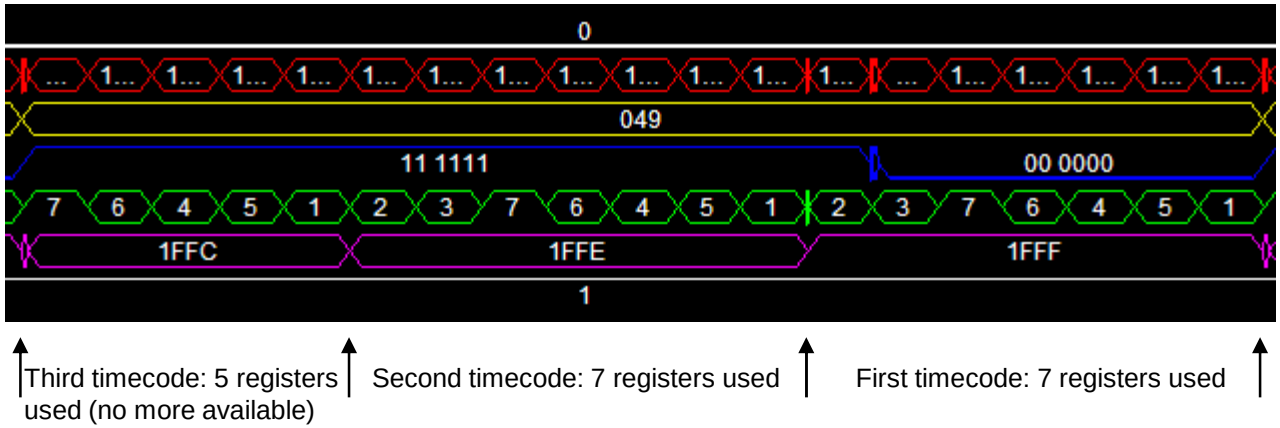




Digital: Odd behaviour



Override mode generates a full memory of hits



First 6 registers in each row incorrectly read 000000 in the hit field!?

- Not yet understood – suspect some internal timing/propagation delay might be affecting memory controller
- Could workaround by effectively disabling those registers (would reduce memory capacity in those columns)

Testing Status

- Sensor basic functionality: working!
  - Known design errors with workarounds:

1	Current limiting inverter (monostables)	Remove transistor, add resistor to ground on PCB
2	Sense amplifier bias chain	Resistor value change on PCB
3	SRAM write (3.3v not possible)	Run sensor at 2.6v, or SRAM reset, variable power supply and change to in-spill timing

  - One remaining “feature” to be investigated in the digital logic (SRAM)
    - (Some additional firmware/software features to aid diagnosis)
- Sensor design evaluation
  - Now need higher level software to facilitate
    - Noise rate/distribution
    - Threshold sweeps etc
    - Per [row/col/pixel] mask and trim verification
  - Analog performance
    - New boards & system for Giulio & Marcel

Additional CALICE test structures

CfI grant "IMAPS" for development/exploration of sensors on INMAPS process (this FY) – some possible spare silicon available for us…

- preShape pixel (in its current form) with analog outputs
  - Not time to include on original design
  - Will further our understanding of analog performance of this process
  - Very little design effort required
- preSample pixel (in its current form) with analog outputs
  - Simply for reference/comparison

With neighbouring inactive pixels

- Bump bond trial pads
  - Second CALICE ASIC will need to be tiled to make a 15x15cm sensing area for beam test
  - Most area efficient way to to this will be to bump bond the chips
  - Solder bump preferred solution
  - Some large pads suitable for bump bonding trials ahead of the second CALICE sensor
  - Small design effort

Would be sent on multi-project run submission mid Jan 2008