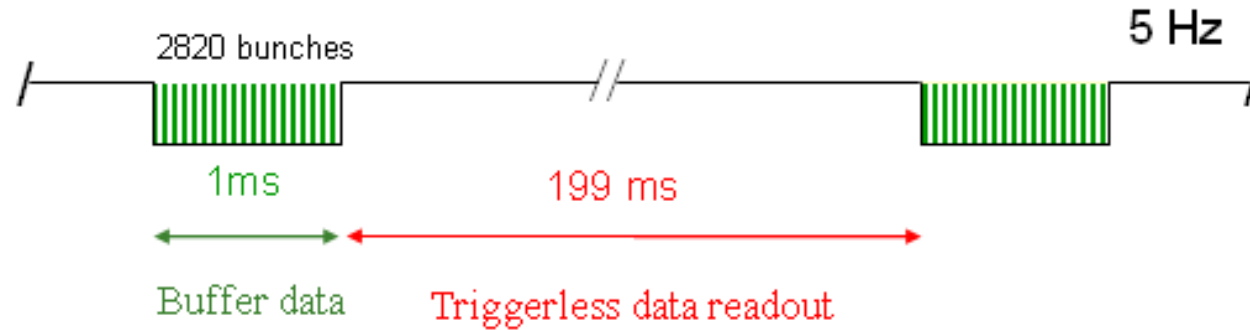# A Tera-Pixel Calorimeter for the ILC

IEEE NSS-MIC 2007
Honolulu,HI

Y. Mikami, O. Miller, V. Rajovic, N.K. Watson, J.A. Wilson
University of Birmingham
J.A. Ballin, P.D. Dauncey, A.-M. Magnan, M. Noy
Imperial College London
J.P. Crooks, M. Stanitzki, K.D. Stefanov, R. Turchetta, M. Tyndel, E.G. Villani
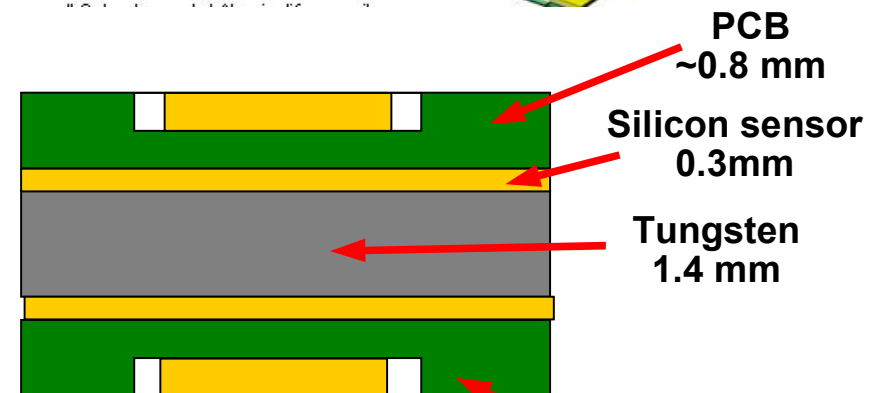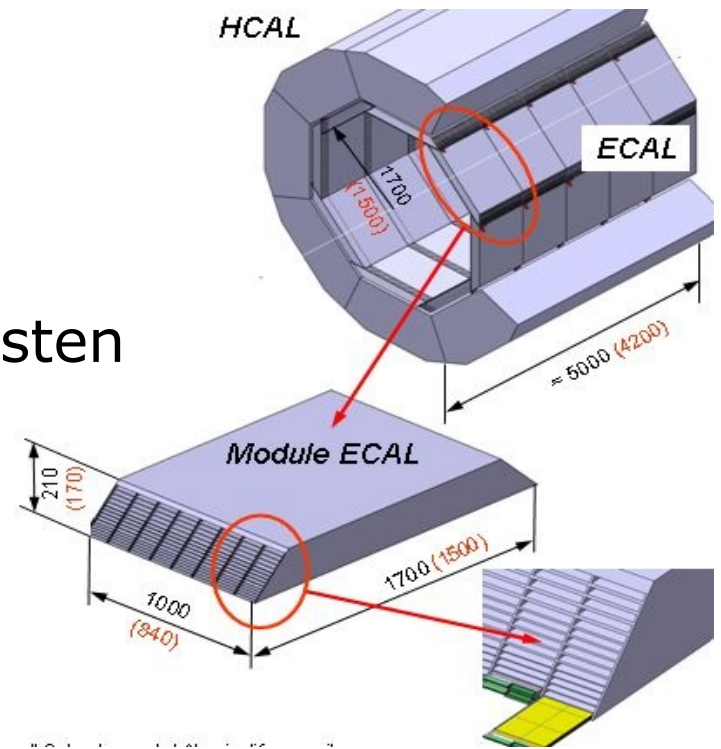*STFC-Rutherford Appleton Laboratory*

Calorimetry for the ILC

- ILC calorimetry focused on Particle Flow Approach (PFA)

  - Requirement of highly granular calorimeters

- ILC is different to LHC

  - Bunch spacing of 300 ns

  - 2820 bunches in 1ms

  - 199 ms quiet time

- Occupancy dominated by beam background & noise

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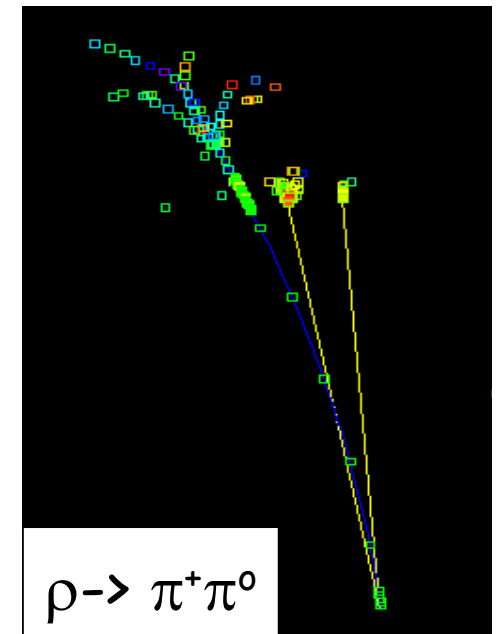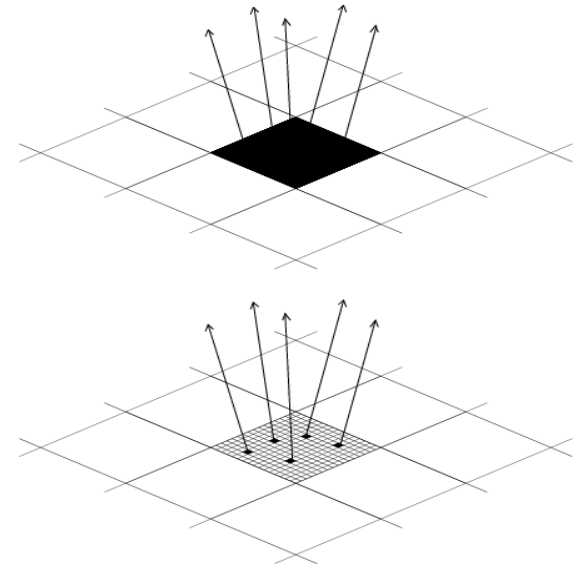
SiW for the ECAL

- The baseline from CALICE

- Sampling Calorimeter

  - Silicon sensors embedded in tungsten sheets

- 30 layers deep

- 1.7 meters radius

- 2000 m^2 silicon area

- Silicon pad size 10x10 mm

Is the granularity sufficient ?

PCB ~0.8 mm

Silicon sensor 0.3mm

Tungsten 1.4 mm

Embedded VFE ASIC

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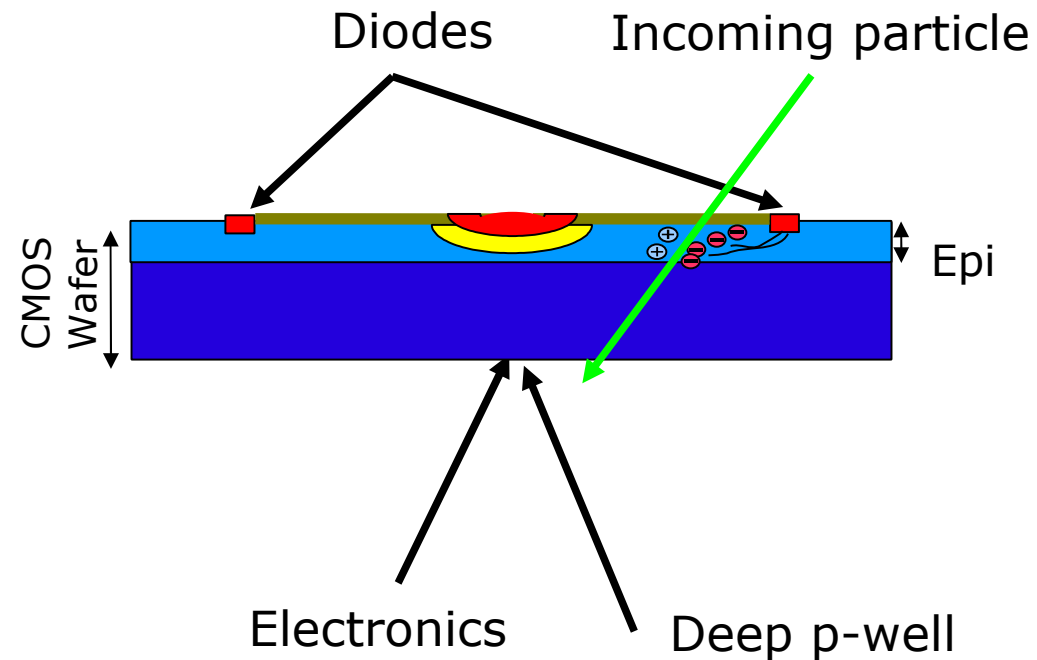Rutherford Appleton Laboratory

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Increasing the granularity

- PFA based on
  - track-shower matching
  - clear shower separation

- Granularity of 10x10 mm may not be sufficient for
  - e.g. π^0 separation
  - clearer shower separation

- Digital Pixels with 50x50 microns
  - basically a Particle Counter
  - ideal for MAPS sensors

$\rho \to \pi^+\pi^0$

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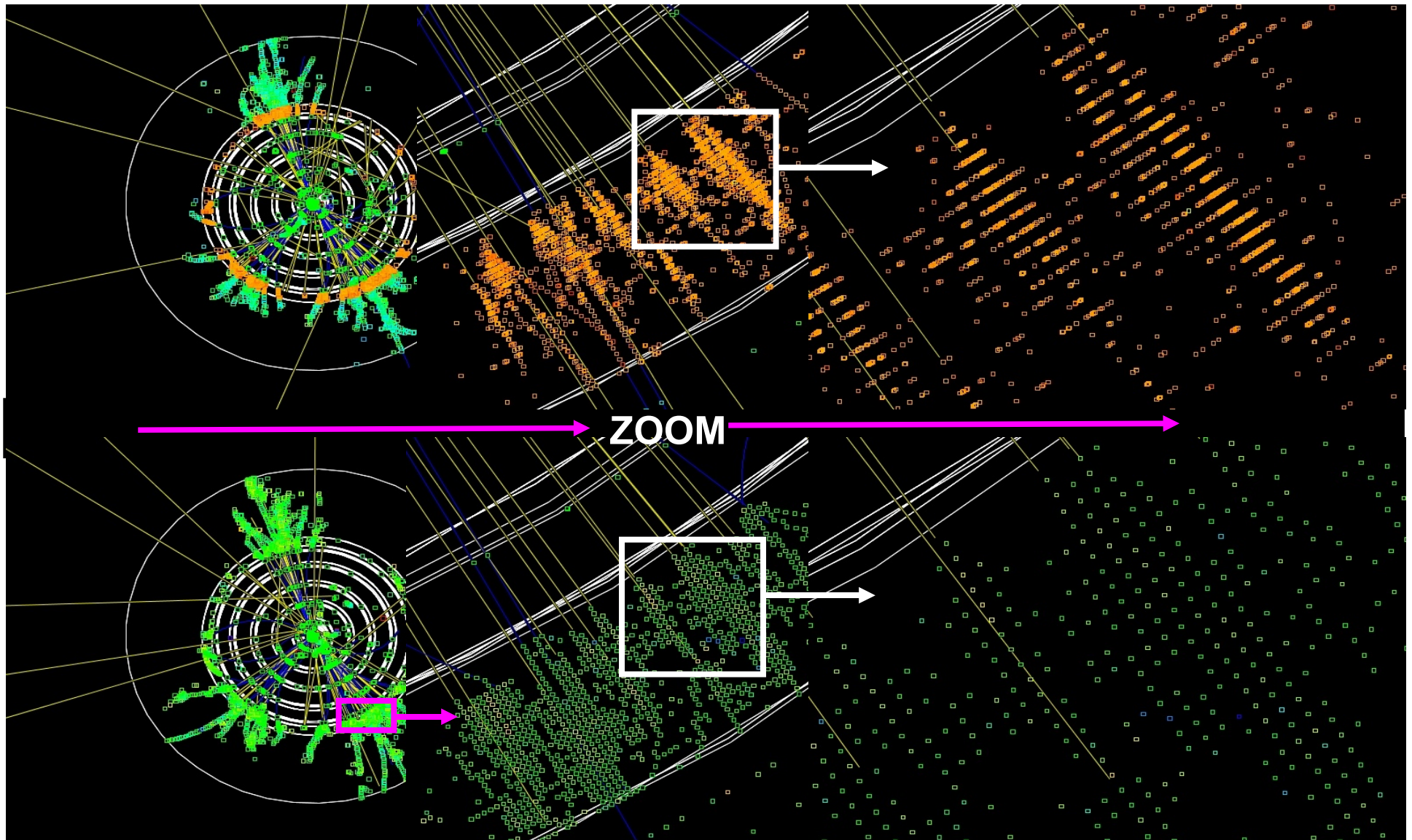Rutherford Appleton Laboratory

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What are MAPS ?

- **M**onolithic **A**ctive **P**ixel **S**ensor

- Integration of Sensor and Readout Electronics

- Manufactured in Standard CMOS process

- Collects charge mainly by diffusion

- Development started in the mid-nineties, now a mature technology

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Comparison

ZOOM

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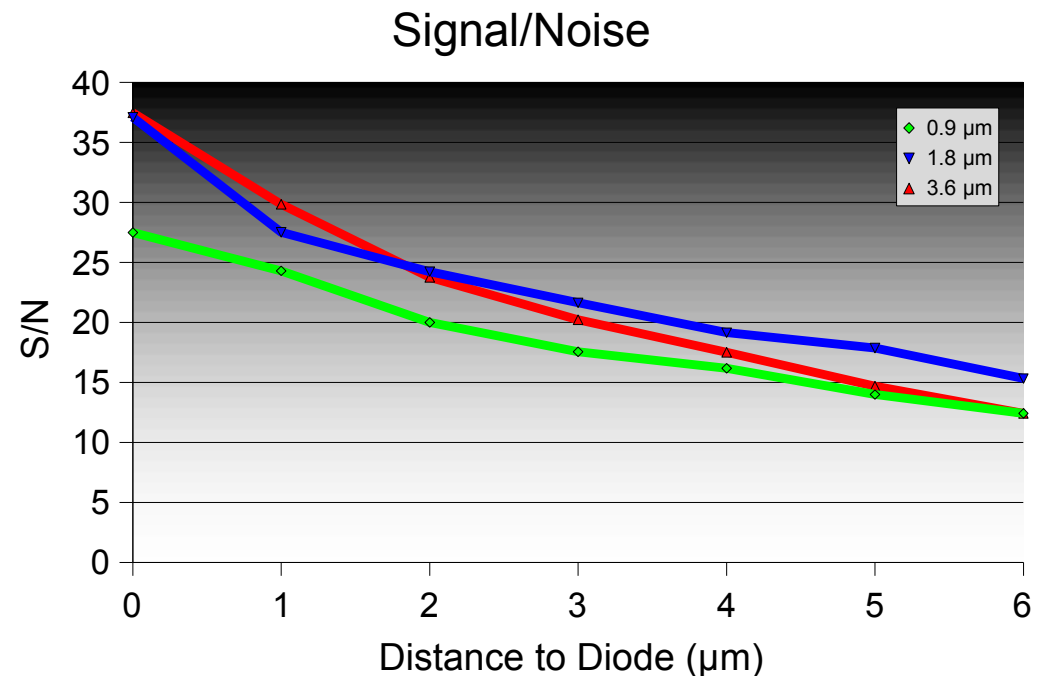Rutherford Appleton Laboratory

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Sensor specifications

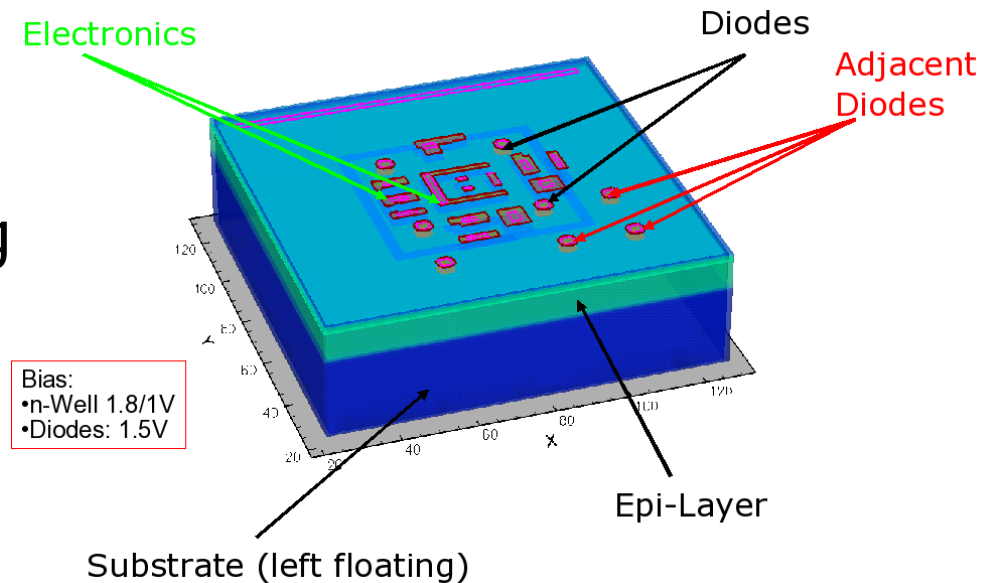- 50x50 micron cell size

- Binary Readout (1 bit ADC realized as Comparator)

- 4 Diodes for Charge Collection

- Time Stamping with 13 bits (8192 bunches)

- Hit buffering for entire bunch train

- Capability to mask individual pixels

- Threshold adjustment for each pixel

- Usage of INMAPS (deep-p well) process

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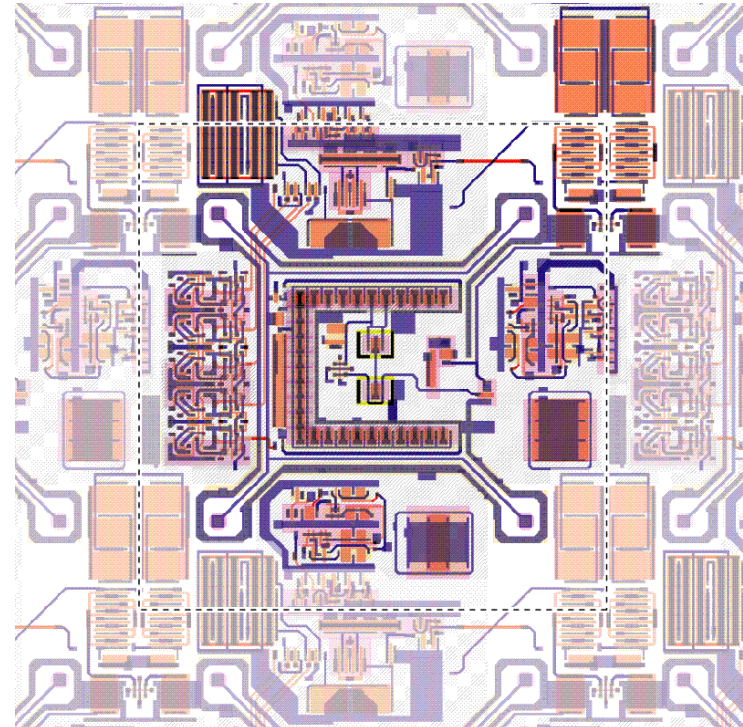
Sensor simulation

- Extensive Simulations using Sentaurus TCAD

- Allows to test many configurations

- Optimize Design parameters

  - Charge collection

  - Number of Diodes

  - Diode Size

  - Epilayer thickness

Signal/Noise

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The ASIC1 sensor

- Received in late July

- 0.18 microns INMAPS Process

- 168x168 Pixels

- two pixel flavors

- test structures
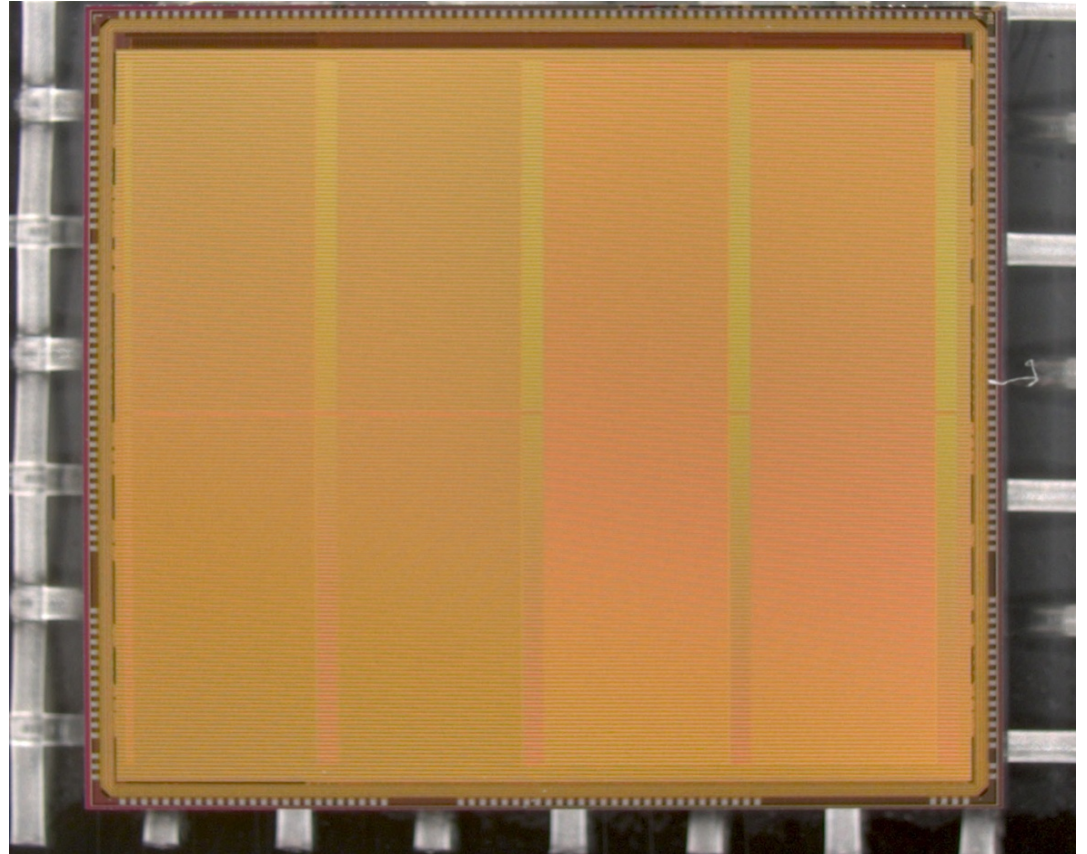
More details on ASIC1 and the INMAPS process in the talk by Jamie Crooks **Tuesday N16-4: 14:15**
A Novel CMOS Monolithic Active Pixel Sensor with Analog Signal Processing and 100% Fill Factor
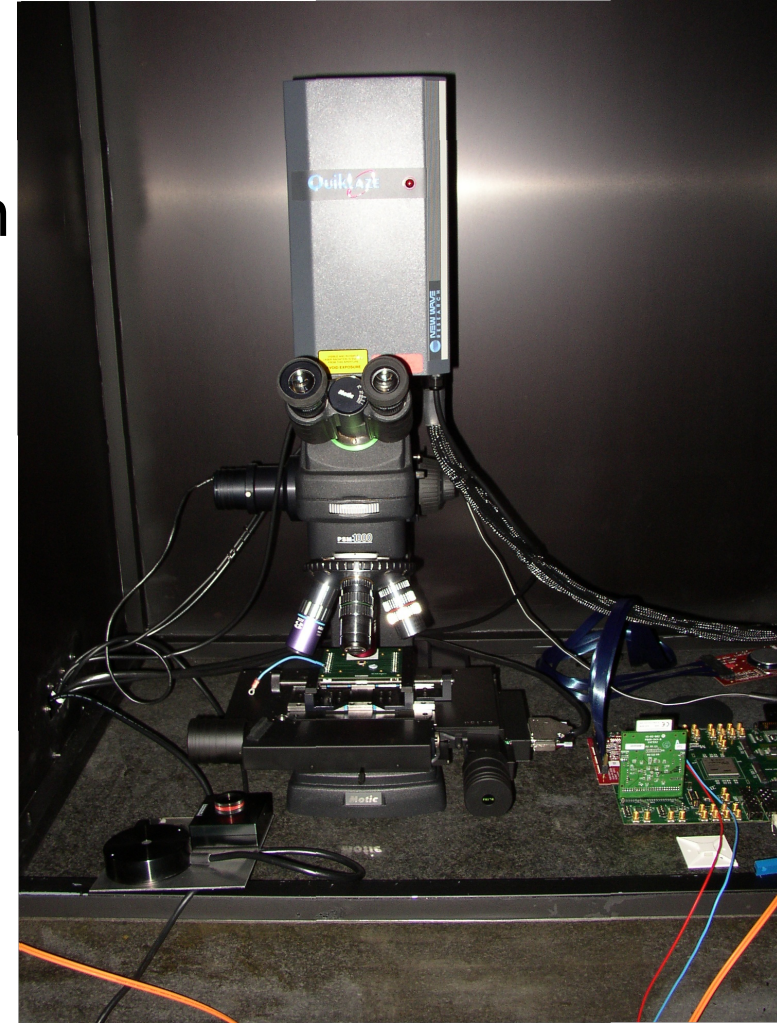
Sensor testing

- Testing delayed by late arrival of PCB boards

- Started testing program using several set-ups

  - Laser for analog characteristics

  - Source runs

  - Cosmics

  - Test beam (December 2007)

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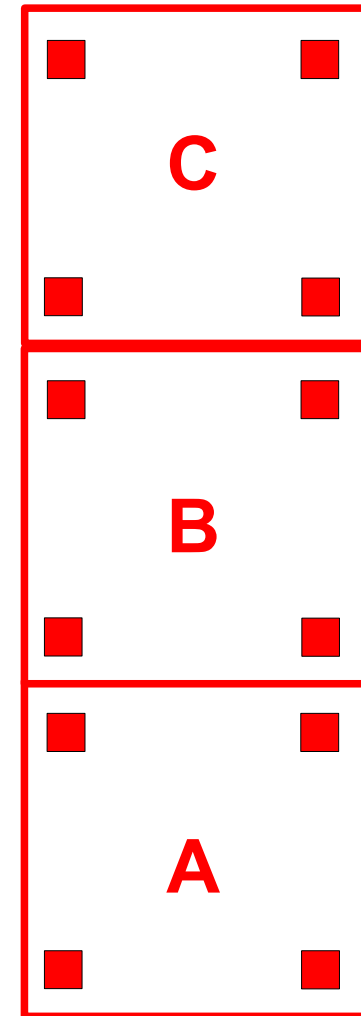
Laser setup

- Powerful Laser setup

- 1064, 532 and 355 nm Wavelength

- Accurate focusing

- (<2 µm at longest wavelength)

- Pulse Width 4 ns

- 50 Hz Repetition rate

- Fully automatized

- Will be used to test the MAPS

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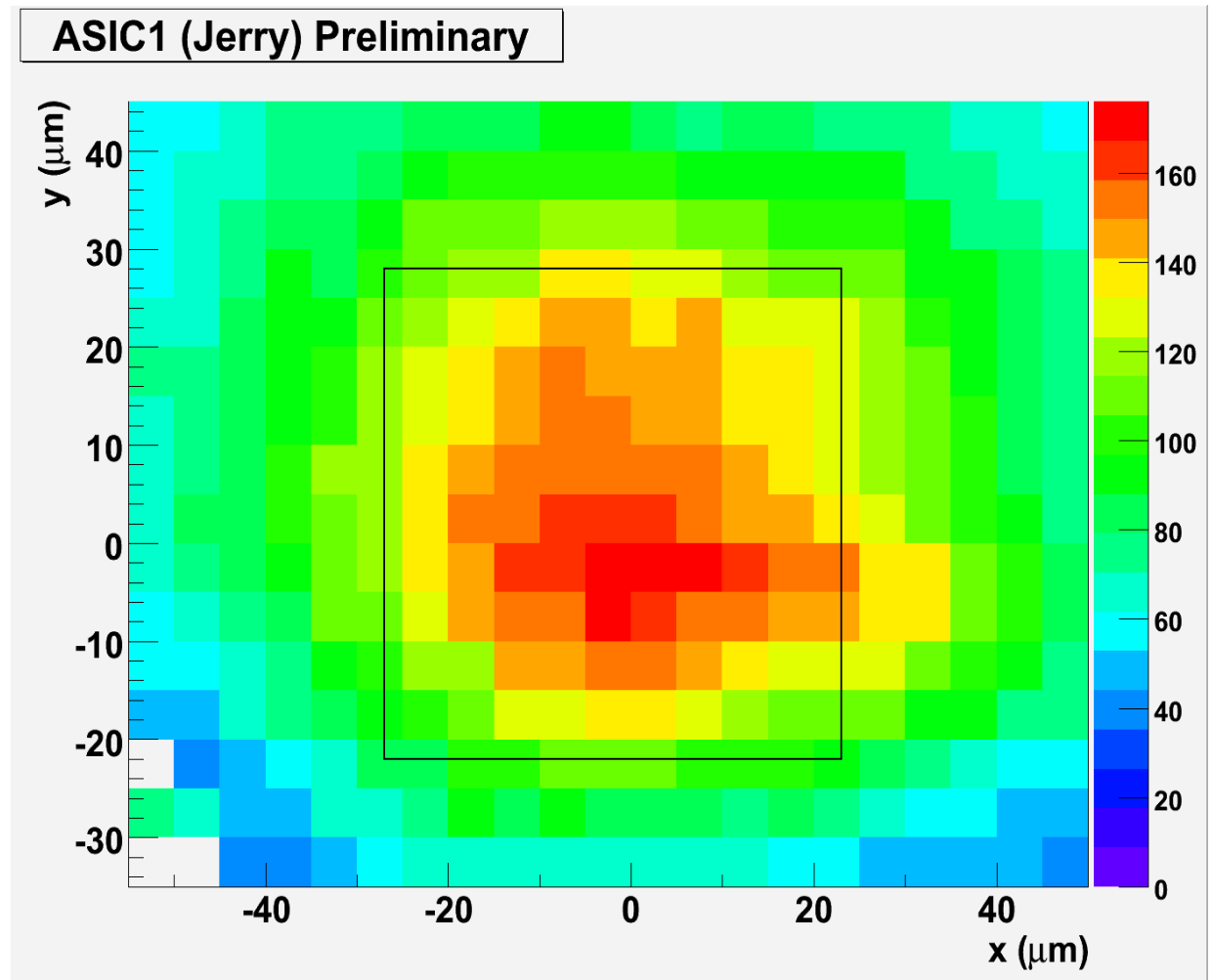Rutherford Appleton Laboratory

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The pixel test structures

- 2 pixels with analog output (A & B)

- 1 Pixel not read out (C)

- Used for

  - process characterization

  - Analog front-end testing

  - Gain calibration (to be done)

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Pixel results (I)

Area scanned by Laser

ASIC1 (Jerry) Preliminary

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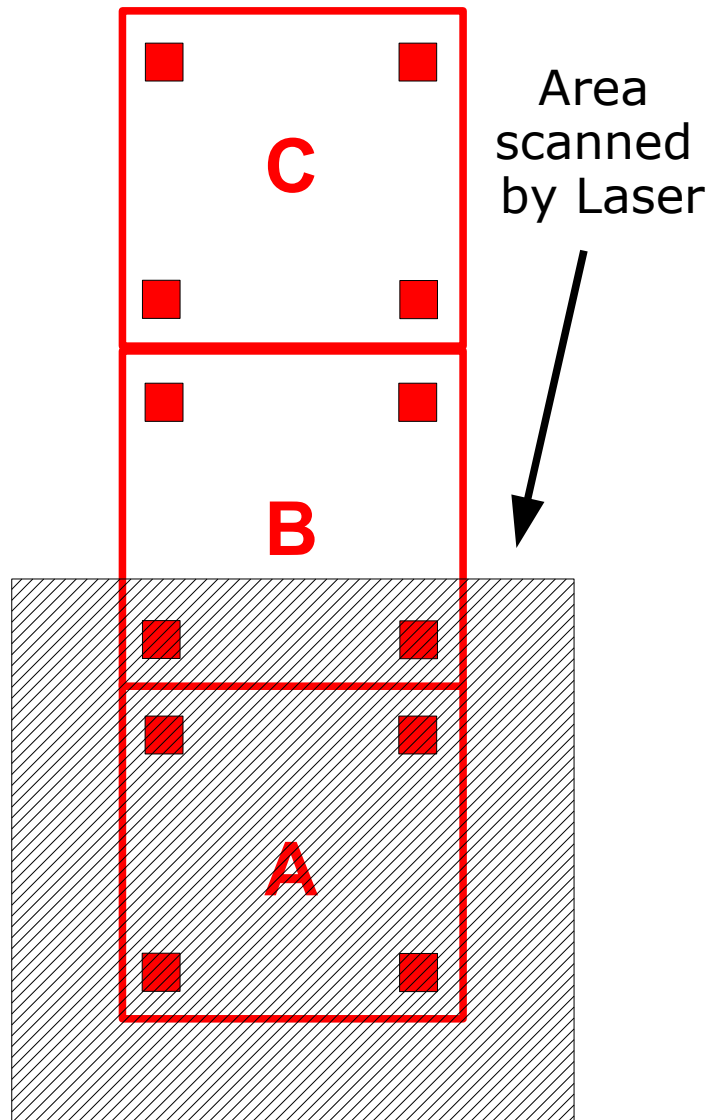
Pixel results (II)

Area scanned by Laser

ASIC1 (Jerry) Preliminary Pixel A

ASIC1 (Jerry) Preliminary Pixel A

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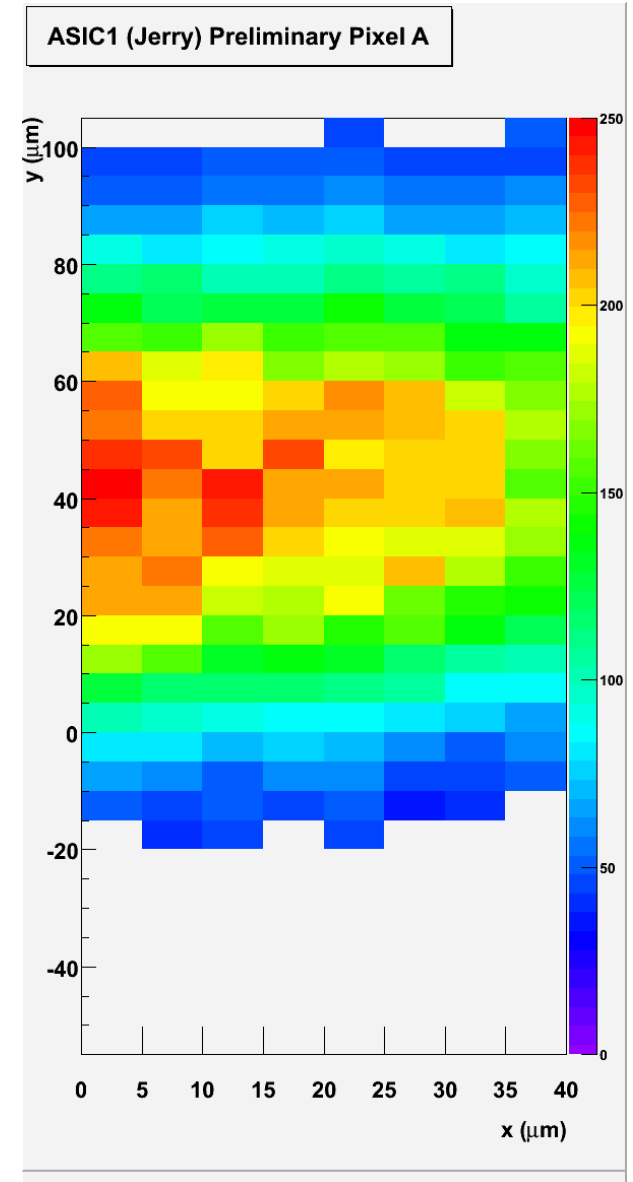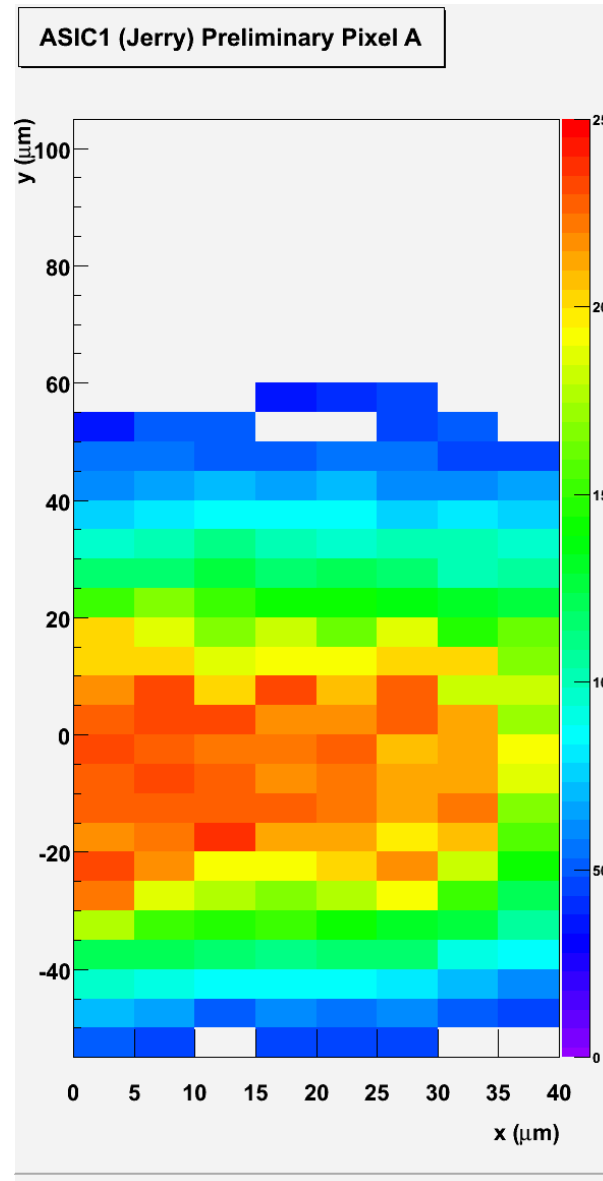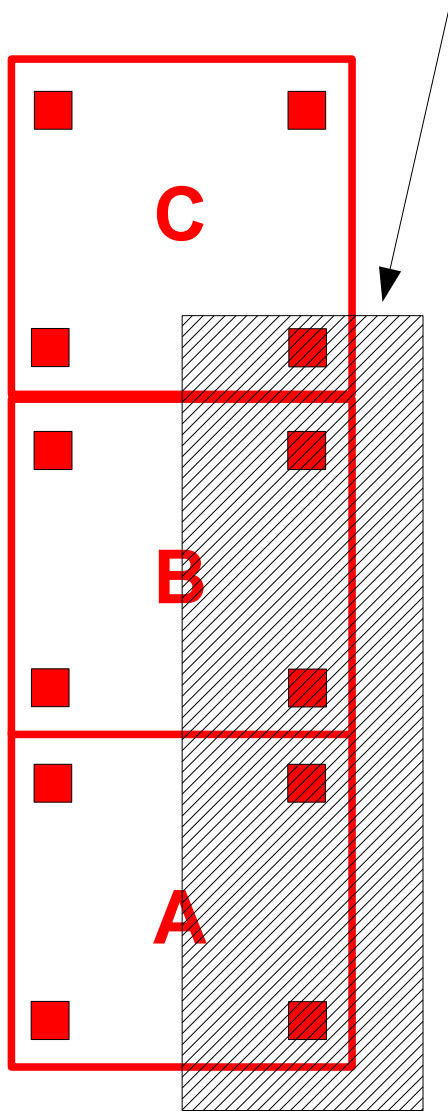
Comparison with simulations

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System issues

- A Tera-Pixel ECAL is challenging

- Benefits

    - No readout chips

    - CMOS is well-know and readily available

    - Ability to make thin layers

- Current sources of concern

    - Power consumption/Cooling

    - DAQ needs

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Power

- Cooling for the ECAL is a general issue

- Power Savings due to Duty Cycle (1%)

- Target Value for baseline ECAL 4 µW/mm^2 (CALICE)

- Current Consumption of MAPS

- ECAL: 40 µW/mm^2 depending on pixel architecture

- Compared to analog pad ECAL

- Factor 1000 more Channels

- Factor 10 more power

- Advantage: Heat load is spread evenly

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DAQ needs

- 10^{12} channels are a lot …

- Physics rate is not the limiting factor

- Beam background and Noise will dominate

- Assuming 2880 bunches and 32 bits per Hit

  - 10^6 Noise hits per bunch

  - ~O(1000) Hits from Beam background per bunch (estimated from GuineaPIG)

- Per bunch train

  - ~88 Gigabit / 11 Gigabyte

  - Readout speed required 440 Gigabit/s

  - CDF SVX-II can do 144 Gigabit/s already

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Power prospects

- **ASIC1 has not been optimized for power consumption**

- Proof of Concept and Technology

- Not the final product

- Options to be explored

  - Larger pixel (50 µm->100 µm) Factor 4 less

  - Longer integrations times if pile-up acceptable, possible factor of 2

  - Smaller feature size (~30-50 %)

  - Lowering Operating Voltages (~10%)

- ASIC1 will allow us to explore some of these

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Summary & Outlook

- A Tera-Pixel ECAL is an interesting option for the ILC:

  - Granularity & Physics possibilities

  - Construction & Cost

- ASIC1 has been manufactured and already gives a proof of principle

  - Test beam data in December 2007

- Larger ASIC2 to be designed and submitted in June 2008

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