A Novel CMOS Monolithic Active Pixel Sensor with Analog Signal Processing and 100% Fill Factor

J.P. Crooks, J.A. Ballin, P.D. Dauncey, A.-M. Magnan, Y. Mikami , O. Miller ,M. Noy, V. Rajovic , M. Stanitzki, K.D. Stefanov, R. Turchetta, *Member, IEEE*, M. Tyndel, E.G. Villani, N.K. Watson , J.A. Wilson

***Abstract*–We have designed and fabricated a CMOS Monolithic Active Pixel Sensor (MAPS) in a novel 0.18 micrometer image-sensor technology (INMAPS) which has a 100% fill factor for charged particle detection and full CMOS electronics in the pixel. The first test sensor using this technology was received from manufacture in July 2007. The key component of the INMAPS process is the implementation of a deep p-well beneath the active circuits. A conventional MAPS design for charged-particle imaging will experience charge sharing between the collection diodes and any PMOS active devices in the pixel which can dramatically reduce the efficiency of the pixel. By implementing a deep p-well, the charge deposited in the epitaxial layer is reflected and conserved for collection at only the exposed collection diode nodes. We have implemented two pixel architectures for charged particle detection. The target application for these pixels is for the ECAL readout in an ILC detector. Both pixels contain four N-well diodes for charge-collection; analog front-end circuits for signal pulse shaping; comparator for threshold discrimination; digital logic for threshold trim adjustment and pixel masking. Pixels are served by shared row-logic which stores the location and time-stamp of pixel hits in local SRAM, at the target 189ns bunch crossing rate of the ILC beam. The sparse hit data is read out from the columns of logic after the bunch train. Here we present design details and preliminary results.**

I. Introduction

In the two leading experiment concepts for the International Linear Collider (ILC) a silicon-tungsten (SiW) electromagnetic calorimeter (ECAL) is proposed [1],[2]. The purpose of this project is to evaluate the suitability of CMOS monolithic active pixel sensor (MAPS) as the silicon in such a machine. Suitability of such MAPS devices for high energy physics applications has been previously demonstrated [3],[4] and so this sensor concept offers the opportunity to implement fine pixel size and integrated readout and timing electronics in a single silicon die at a competitive cost.

This first sensor has been designed to operate at the baseline machine parameters for ILC: Bunch trains of 2625 bunch crossings occur at a minimum spacing of 189ns with 199ms inter-bunch spacing. The requirement of this sensor is to detect and store the timestamp and location of minimum-ionizing particle (MIP) events that occur during the bunch train. Sufficient memory capacity is required to buffer both genuine hit and noise hit data for the duration of the bunch train, which are then read out between bunch trains.

Device and physics simulations [5],[6] suggest that a 50 micrometer pixel pitch with binary pixel operation provides the granularity required for shower reconstruction and energy measurement at the ILC. Small MIP signals and a target noise rate of $10e^{-6}$ dictate that each pixel must include some analog signal processing and adjustable threshold discrimination, which requires many transistors, both PMOS and NMOS in a small pixel. As the collecting junction is formed by an N-well and the P-doped substrate, the N-wells which form the substrate of PMOS transistors would also collect charge, significantly reducing the efficiency of the pixel. In order to avoid this charge losses, we developed a new advanced 0.18 micrometer CMOS process, called the *INMAPS* process, which features an extra deep P-well implant to shield unrelated N-wells from collecting charge.

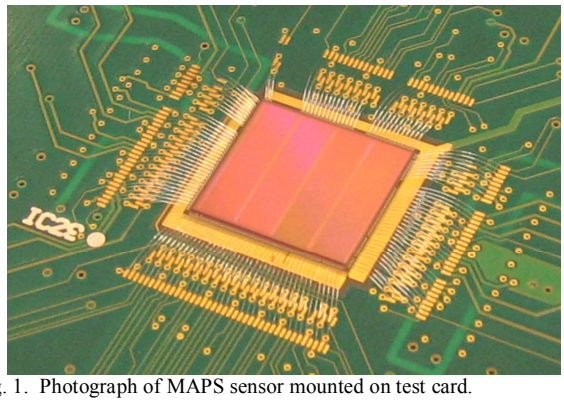

Fig. 1. Photograph of MAPS sensor mounted on test card.

The first sensor in this project, shown in Fig.1 has been designed and fabricated in the new *INPAMPS* process and is currently under test.

In section II we introduce the *INMAPS* process technology. In section III we introduce the two pixel architectures that have been implemented in this first test sensor and show the implementation of the deep p-well. Section IV describes the operation of the sensor, and some preliminary results are reported in section V.

Manuscript received November 21, 2007. This work was supported by a grant from the Science & Technology Facilities Council (STFC).

J.P.Crooks, R.Turchetta, M. Stanitzki, K.D. Stefanov, M. Tyndel and E.G. Villani are with the Rutherford Appleton Laboratory, Chilton, Oxfordshire, OX11 0QX, UK. (telephone: +44 1235 446392, e-mail: j.p.crooks@rl.ac.uk)

J.A. Ballin, P.D. Dauncey, A.-M. Magnan and M. Noy are with Imperial College London, Blacket Laboratoy, South Kensington, London SW7 2AZ, UK.

Y. Mikami , O. Miller , V. Rajovic , N.K. Watson and J.A. Wilson are with the University of Birmingham, School of Physics and Astronomy, UK

II. Technology

The *INMAPS* process was specifically developed for this project: The process is a standard 0.18 micrometer CMOS technology but with an additional processing step that deposits a high energy *deep-P-Well* implant. Locating this implant beneath all active circuits in the pixel (Fig. 2) creates a barrier to charge diffusing in the epitaxial layer, preventing it from being collected by the positively charged N-Wells of in-pixel circuits. The result is a pixel design that offers 100% charge collection efficiency, and is therefore ideal for applications where complex circuits are present in the pixel. Sensors were fabricated with and without the deep p-well processing step for evaluation of this new technology.

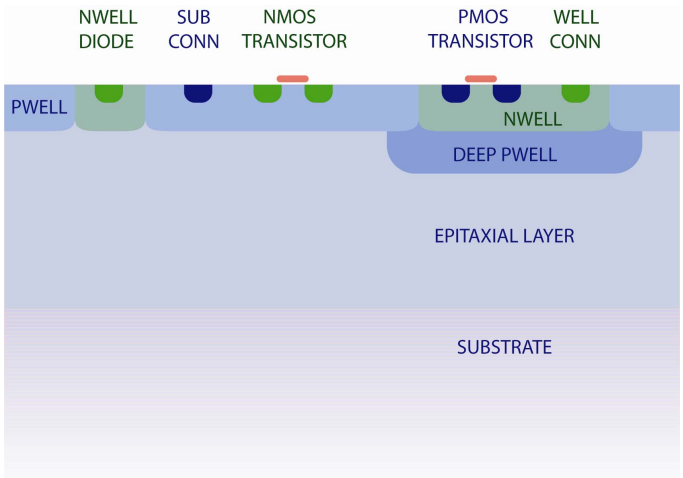

Fig.2. Sketch of the *INMAPS* process cross section illustrating the implementation of a deep P-Well beneath a pmos transistor in the pixel: Only the N-Well of the charge-sensitive diode node is exposed in the epitaxial layer for charge collection.

III. Design Detail

A. Pixel Design

The test sensor design incorporates sub-arrays of four different pixels, of which there are two primary architectures: *preShape* and *preSample*. All pixels contain four small N-Well diodes for charge collection, whose size has been optimized for signal-to-noise ratio.

The *preShape* pixel pre-amplifies the collected charge and uses a CR-RC shaper circuit to generate a shaped signal pulse with peak and decay time proportional to the input. A pseudo-differential signal is achieved by using the input to the shaper circuit as a reference level. From the simulation, the pseudo-differential signal gain at the input to the comparator is 94 uV/e- and the Equivalent Noise Charge (ENC) is 23 e- rms.

A two-stage comparator, common to both pixel architectures, generates an asynchronous local *hit* decision, using a differential global threshold and applying per-pixel trim adjustment that is configured and stored prior to bunch train operation. A monostable circuit is used to generate an output pulse of a controlled length to ensure a minimum or maximum input signal is recorded as a single hit by the logic. The shaper circuit naturally recovers after a signal pulse and is therefore ready for a subsequent hit event after a short delay time proportional to previous signal magnitude.

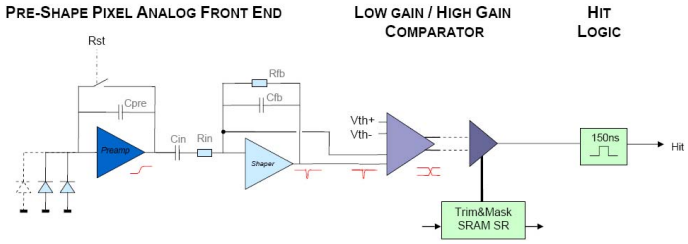

Fig. 3. PreShape pixel block diagram showing the analog signal path from collecting diodes to binary *hit* output.

The *preSample* pixel pre-amplifies the voltage drop on the diode node, similar to a conventional MAPS device [7], and then uses a charge amplifier to generate a voltage step proportional to the input. The charge amplifier has been previously reset and a voltage sample stored on a local capacitor: This forms the reference for the pseudo-differential signal. From the simulation, the signal gain at the input to the comparator is 440uV/e- and the ENC is 22 e- rms. Two monostable circuits generate a hit output and the necessary signals to reset the charge amplifier and take a new reference sample. After this short *self-reset* the pixel is then active and will respond to a subsequent hit event.

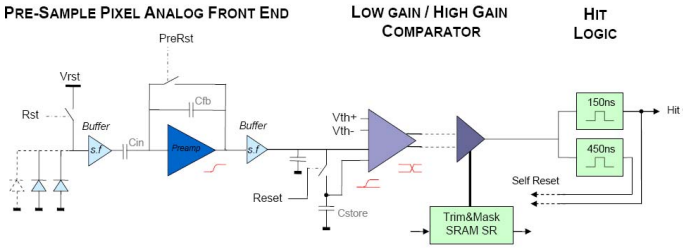

Fig. 4. PreShape pixel block diagram showing the analog signal path from collecting diodes to binary *hit* output.

Two variants of both pixel architectures were implemented: In each case the difference lies only with subtle changes to the capacitors in the circuit to optimize signal gain based on circuit simulations. The pixel variants (numbered by 1,2,3,4 are identified in Fig. 6.

B. Pixel Layout

The *preShape* and *preSample* pixels comprise 160 and 189 transistors respectively, and are laid out on a 50 micrometer pitch. The implementation of the deep p-well implant in the pixel can be seen in figure 5. The complex pixel circuits have been arranged such that N-Wells can be protected with a single symmetrical deep p-well. The four n-well diodes in each pixel remain exposed to the substrate, and have been pushed towards the corners to help reduce pixel crosstalk.

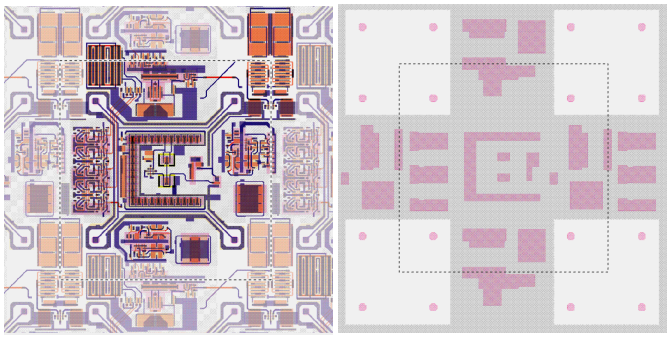

Fig. 5: Example PreSample pixel layouts: The diagram on the left shows design layers up to metal 1 showing the complexity of circuits implemented in the 50 micrometer pixel boundary that is indicated by the dotted line. The diagram on the right shows the same region for layers N-Well and Deep P-well only, which shows how the deep p-well is placed to leave only the charge-collecting diodes exposed.

C. *Sensor Architecture*

The four pixel variants occupy quadrants of the sensitive area, which contains 28,224 pixels and covers 79.4mm^2. A sub-row of 42 pixels is served by logic containing SRAM registers, which form 250 micrometer wide columns that are insensitive to any charge deposits; a single row of dead pixels across the centre of the sensor is used to distribute bias and reference voltages, and to re-buffer control signals. These logic and bias regions account for an 11.1% dead space in the sensing area: Charge arising from particles that pass through these regions will be collected by local N-Wells associated with PMOS transistors.

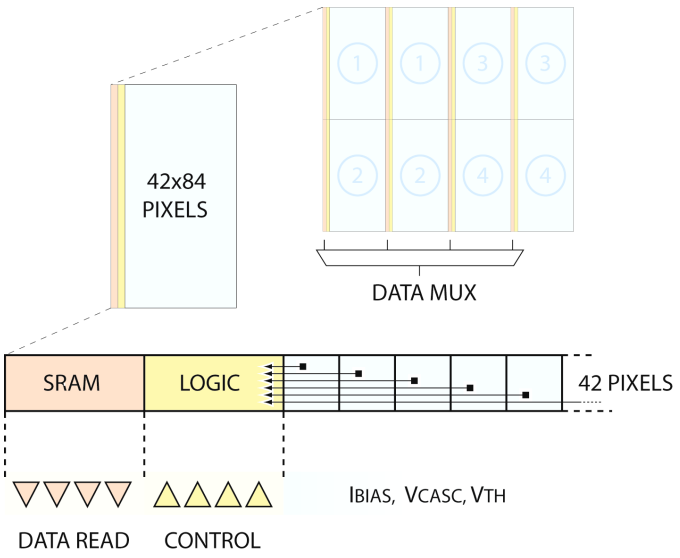

Fig. 6: Test sensor architecture. Pixels are grouped in rows with dedicated control logic and SRAM, which form sub-arrays of 42x84 pixels. These sub-arrays are tiled together implementing several pixel architectures in the full array of 168x168 pixels.

D. *Row Control Logic*

The *hit* outputs from 42 pixels are wired across to each section of row logic. The row logic can latch the state of these asynchronous inputs by external control for synchronization with the beam crossing rate, and then begins the processing sequence depicted in Fig. 7.

The principle of the hit data storage is to make optimal use of the finite amount of local memory available in each row. Rather than storing each individual hit separately, the row is divided into 7 parts. Each of the 7 sub-sections of the row is interrogated in turn, and the pattern of hits is stored if any are present. This offers a reduction in the number of memory locations used for a high density of co-incident hits, such as a dense particle shower, whilst only using single memory location for noise hits.

The row logic contains 19 SRAM registers which store the global timestamp code, the pattern of hits and the multiplex address that identifies their location within the full row of 42 pixels. Row addresses are generated by a local ROM such that they appear as part of the readout parallel data word.

The memory manager facilitates data write to each register in turn, and selects each of the valid registers during readout. An overflow flag is raised if more than 19 hits are generated in the row, in which case the first 19 hits that occurred are retained and any subsequent hit data discarded on a row by row basis. The memory manager is implemented as a bi-directional SRAM shift register which selects a single register with one-hot coding.

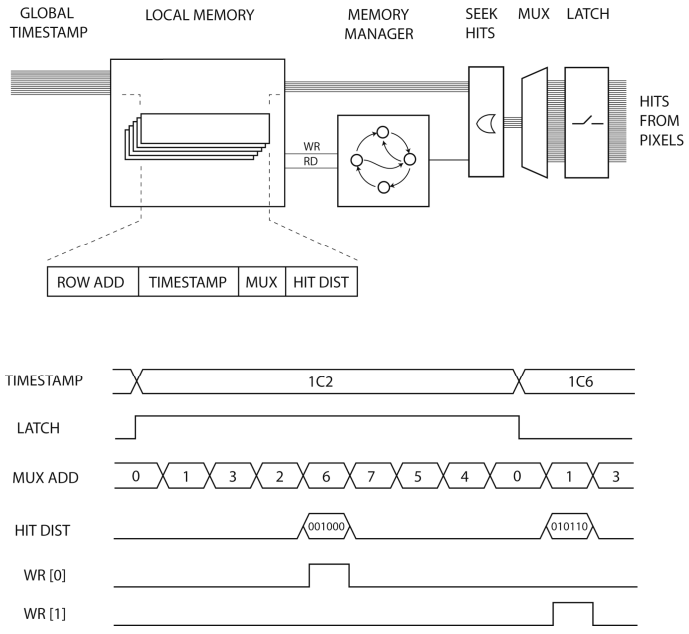

Fig. 7: Row control logic operation: block diagram and typical timing operation for a bunch crossing.

E. *Test Features*

In addition to the main design presented in section II, three test pixels are provided with access to internal nodes for evaluation. These include facility to evaluate performance of monostable circuits, comparator, trim adjustment of threshold, and the analog front end circuits for the preSample pixel architecture.

The row control logic can be operated in an *override* mode which stores the hit output from every pixel regardless of

status. The 13 bit timestamp is generated off chip so arbitrary values can be driven during override operation to verify correct SRAM read and write. Pixel configuration data, mask and trim setting, can be read back from the array for error rate evaluation.

IV. Sensor Operation

A. Test Hardware

The sensor is mounted on a printed circuit card comprising voltage regulators, programmable DACs for voltage and current biases, temperature sensor and LVDS transceivers for inter-board communication. A 2-meter ribbon cable link connects the sensor card to a second card that hosts a Xilinx FPGA with USB2 interface to PC.

The test system includes provision for master/slave interface with other identical systems for synchronized operation of several sensors at once, input from scintillator and PMT for triggered source tests, and control interface for the laser instrumentation described in the next section.

B. Laser Test

A 1064nm wavelength laser is focused and positioned with sub 1 micrometer precision to inject charge as a 4ns pulse delivered to the back side of the sensor. The wavelength was chosen so that the silicon is near-transparent, with absorption length of several hundred micrometers. The amount of charge that is deposited has not been calibrated at this time, so results from these tests are intended to show relative charge collection versus position.

The laser is focused to 4x4 micrometer and 5x5 micrometer square regions of exposure and pulsed at 25 Hz. The position is stepped in increments of 5 micrometers in x and y to scan a region in and around test pixels. The signal step amplitude is measured and histogrammed on a LeCroy oscilloscope, with the most probable value recorded for each laser position.

C. Planned Further Testing

Planned tests for this sensor include Fe55 and Sr90 radioactive sources for absolute MIP characterization. Four devices stacked at 5mm separation will be used for cosmic ray tests, and also for a possible beam in December 2007.

The laser test setup offers much opportunity for further characterization of the sensor, including per-pixel scanning for identification of dead pixels, evaluation of gain uniformity, crosstalk, and for comparison of charge collection against device simulation.

V. Preliminary Results

Some preliminary results and observations are presented from the early stages of testing.

A. Proof of Life

In-pixel SRAM configuration data for the full sensor array can be written and read back without error. The pixel test structures have been exercised to show correct operation of in-pixel monostables and comparator circuits, including threshold adjustment by 4 bit trim setting. Furthermore, the analog nodes of the preSample circuits show that the pixel signal node can be saturated with integration of light, as expected.

The row logic has been exercised in *override* mode to generate false hits in the local SRAM memories that contain timestamp, bank and hit patterns. Overflow flags are generated at the expected time. The SRAM memories can be read back, showing correct timing of each column and verifying the operation of the data sense amplifiers and full data chain back to the host PC. Switching off the *override* mode allows real *noise* hits from pixels to be observed in the data with threshold scan.

B. Charge Collection

Signal pulse amplitude for pulsed laser stimulus of a 4x4 micrometer spot is mapped in and around a test pixel. Charge collection is demonstrated, including charge spread effects resulting partly from the absence of any neighboring pixels in the horizontal plane.

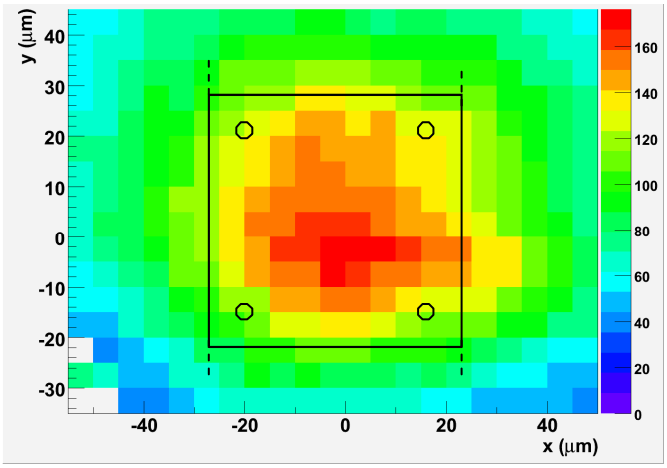

Fig. 8. Signal pulse amplitude versus laser position. The pixel outline is annotated for scale reference only, and is only an estimate of pixel location since the rear of the sensor has no facility to identify exact position.

C. Deep P-Well evaluation

Signal pulse amplitude for pulsed laser stimulus of a 5x5 micrometer spot is mapped in and around a test pixel on two sensors, with and without deep P-well processing. In the sensor with no deep p-well, the footprint of the diodes is clearly visible. This is expected because when the laser hits an offset location, a significant amount of charge is more likely to be collected by the N-well where the PMOS transistors sit and is therefore lost as signal. On the contrary, the response of the sensor with deep p-well is much more uniform in the region scanned. The amplitude is also higher, as the lowest signal within the pixel boundary for the sensor with deep p-well is higher than the highest signal in the sensor without deep p-well.

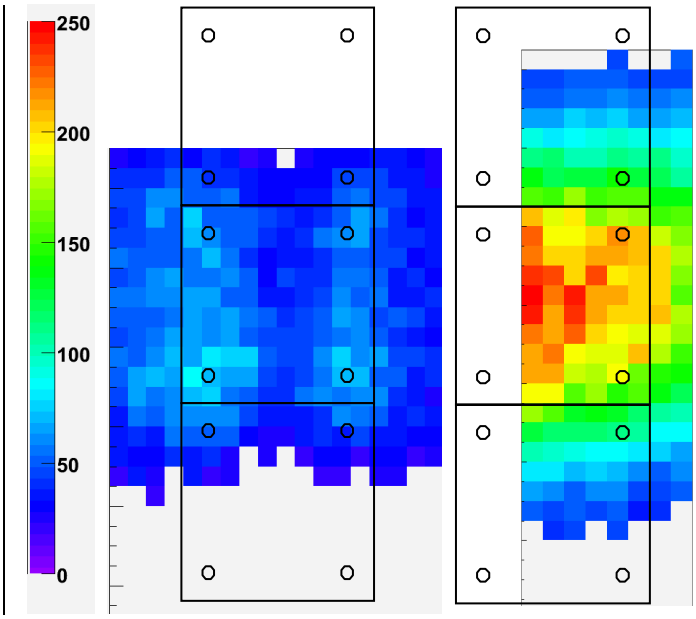

Fig. 9. Signal pulse amplitude versus laser position for sensors with (right) and without (left) the deep p-well processing, otherwise identical processing and bias conditions. The pixel outlines are annotated for scale reference only, and are only an estimate of pixel location since the rear of the sensor has no facility to identify exact position.

VI. Conclusion

We have successfully designed a novel sensor with in – pixel processing. In order to maintain the 100% fill factor for charged particle detection, the sensor was manufactured in a new advanced 0.18 micrometer CMOS technology, called *INMAPS*. This technology features an extra deep p-well implant to prevent the substrate of the PMOS transistors in the design from collecting charge. Preliminary tests of the sensor are very promising. The design is performing satisfactorily and we are currently preparing the ancillary system for the full detailed evaluation of the sensor.

Sensors were fabricated with and without the extra deep p-well implant. While no significant difference was found in their functionality, the first results about the charge collection efficiency are very interesting: As expected, the non-deep p-well sensor shows much smaller and less uniform response compared to the sensor with deep p-well. The charge collection in the pixel area for the sensor manufactured with the deep-p-well layer is fairly uniform and therefore a "hit" should have low dependence on the exact location of an incident particle. A cut through results from two adjacent test pixels show that pixel crosstalk should not extend beyond one additional pixel in the worst case.

The test pixels are not surrounded by neighbor pixels for collection of charge, and so although indicative, do not perfectly represent charge diffusion and collection in the main body of pixels.

The thorough evaluation of this sensor planned for the next few months will influence the design of a second sensor commencing in early 2008. This second sensor will implement a single pixel design, selected from one of those currently under test, to cover a much larger sensor up to reticle size. The second sensor will minimize dead area and pad count so that sensors can be tiled in a bump-bonded arrangement for beam test in 2009.

References

[1] "LDC outline", http://www.ilcldc.org/documents/dod/outline.pdf
[2] "SiD detector outline", http://hep.uchicago.edu/~oreglia/siddod.pdf
[3] R. Turchetta, "CMOS Sensors for the detection of Minimum Ionising Particles", in *Proceedings of the 2001 IEEE Workshop on Charge-Coupled Devices and Image Sensors*, Lake Tahoe, Nevada, USA, 7-9 June 2001, 180-183
[4] P. Allport et al, "CMOS Sensors for High Energy Physics", *Extended programme of the 2005 IEEE Workshop on CCD and Advanced Image Sensors*, Nagano, Japan
[5] P.D. Dauncey, Concept for a Si-W ECAL for the ILC based on MAPS. http://www.hep.ph.ic.ac.uk/calice/maps/mapscd/mapscd.pdf
[6] M.Stanitzki et al, "A Tera-Pixel Calorimeter for the ILC" in *Proceedings for 2007 IEEE NSS conference*
[7] E.R. Fossum, "CMOS image sensors: Electronic Camera-On-A-Chip", *IEEE Trans. Electron Devices,* vol 44, no.10 pp. 1689-1698, Oct 1997