ASIC1 à ASIC2

Things still to learn from ASIC1

Options for ASIC 1.01à 1.1 à 1.2

Logic test structure for ASIC2

Things still to learn from ASIC1

Test beam

a) Check labelling & operating conditions of hits-per-BT plot (back/red)
b) Threshold scans of all sensors shown together, one plot for each of the four pixel architectures
c) Spatial info – locations of noisy pixels
d) Statistics of hits – beam profile?
e) Per-pixel efficiency?

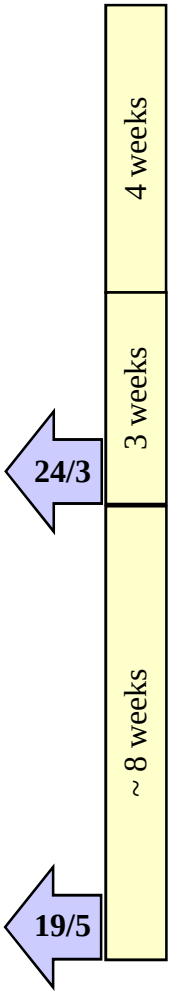
Laser

e) Bias optimisation for signal/noise
f) Automated scan of every pixel to compare gain/noise
g) Crosstalk analysis –scan around a 9x9 block of pixels – vs threshold
h) Linearity

Bench

i) Threshold scan with VTH signals buffered / externally driven
j) Full speed operation (189ns bunch crossing rate)
k) Noise vs temperature

Possible next sensors



Sensor 1.01 *(4 seats silicon)* **PCB 1.0**

a) bug fix SRAM write with full 3.3v level-shifting
b) bug fix monostables (IOUTBIAS mirror transistors)
c) bug fix ISENSEBIAS mirror transistor
d) add nwell diodes around test structure pixels
e) larger bond pads?

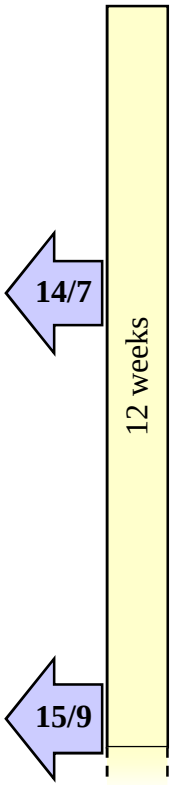
Sensor 1.1 *(4 seats silicon)* **PCB 1.1**

f) add preShape test structures — 2nd hole for laser
g) extra pads?

Sensor 1.2 *(4 seats silicon)* **PCB 1.X**

h) add analog buffers for VTH and VRST signals?
i) reduce / change pixel variants?
j) tweak pixel design for noise/gain performance?
k) …

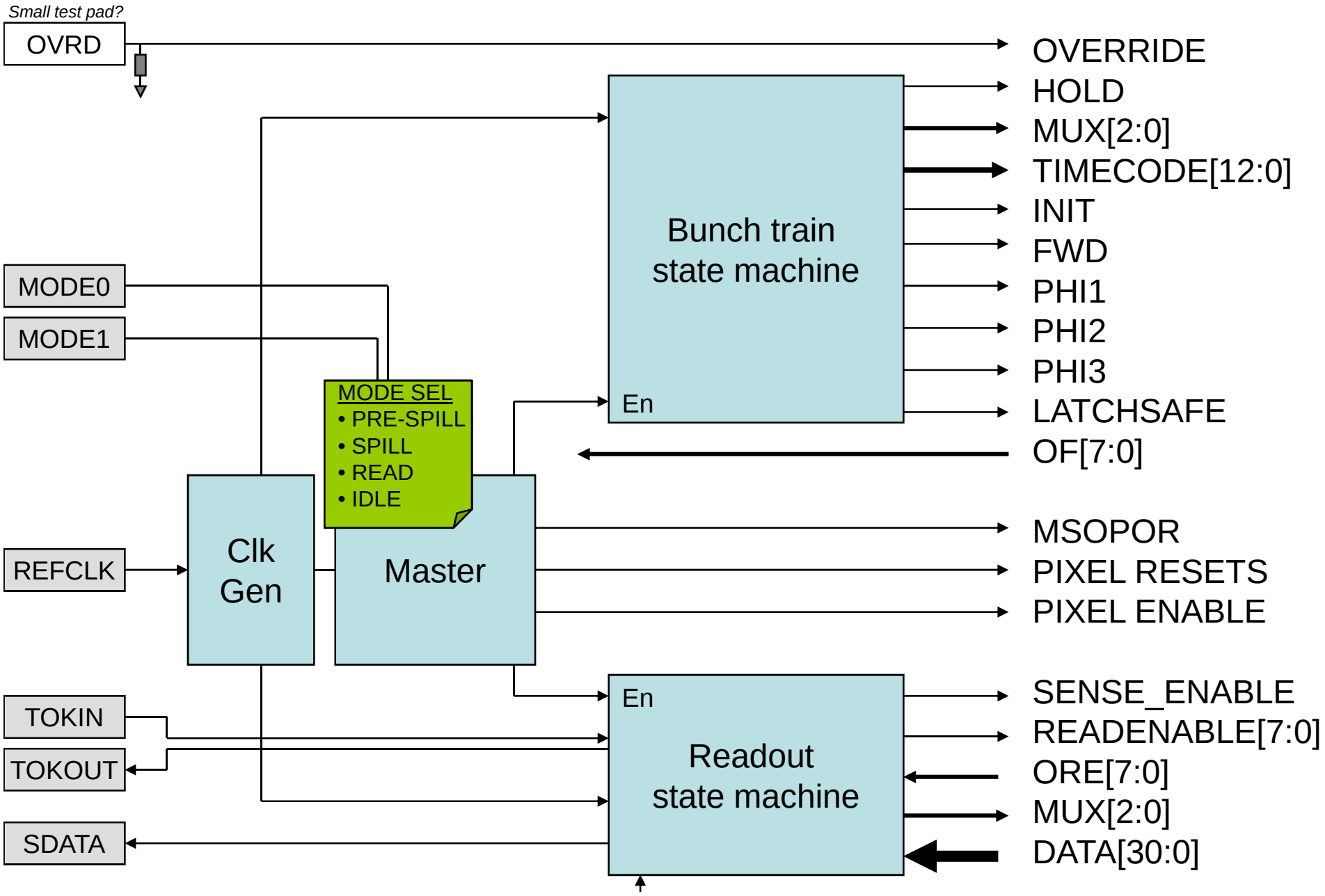
Possible next sensors



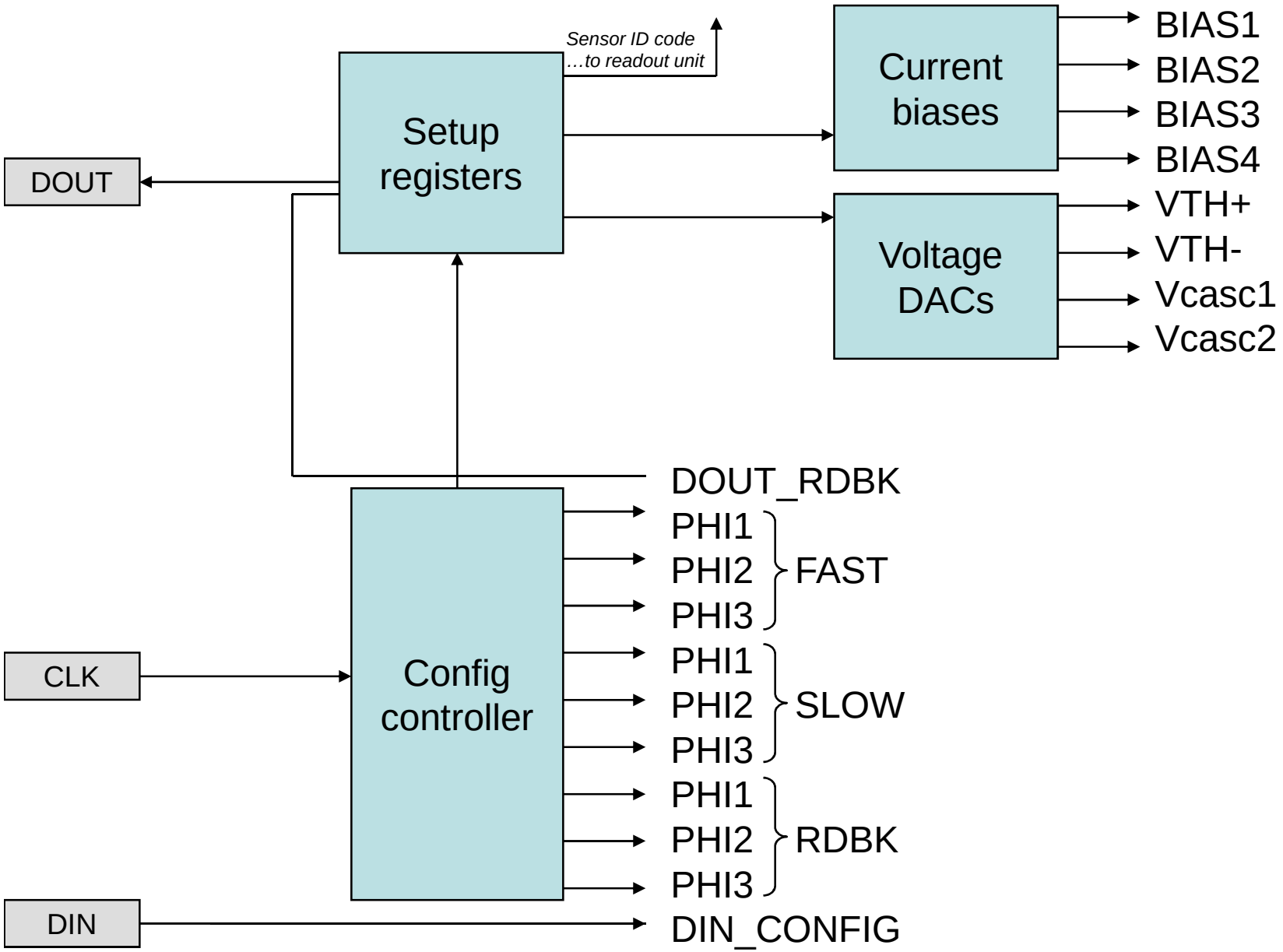
Logic/Support Test Structure ***(+1 seat silicon)*** ***New test PCB(s) required***

a) Large pad-over-logic pad cells for bump-bond tests
b) LVDS receiver and transmitter pad circuits
c) Gray code counter for timestamp generation
d) Clock generator (makes all sensor internal clocks from one external clock)
e) Bunch train state machine
f) Readout state machine
g) Master controller (co-ordinates preceding logic blocks, resets, power-on safe states)
h) Configuration controller (co-ordinates mask & trim programming, adding on-chip registers for current/voltage DACs etc.
i) Current DAC circuits
j) Voltage DAC circuits
k) …

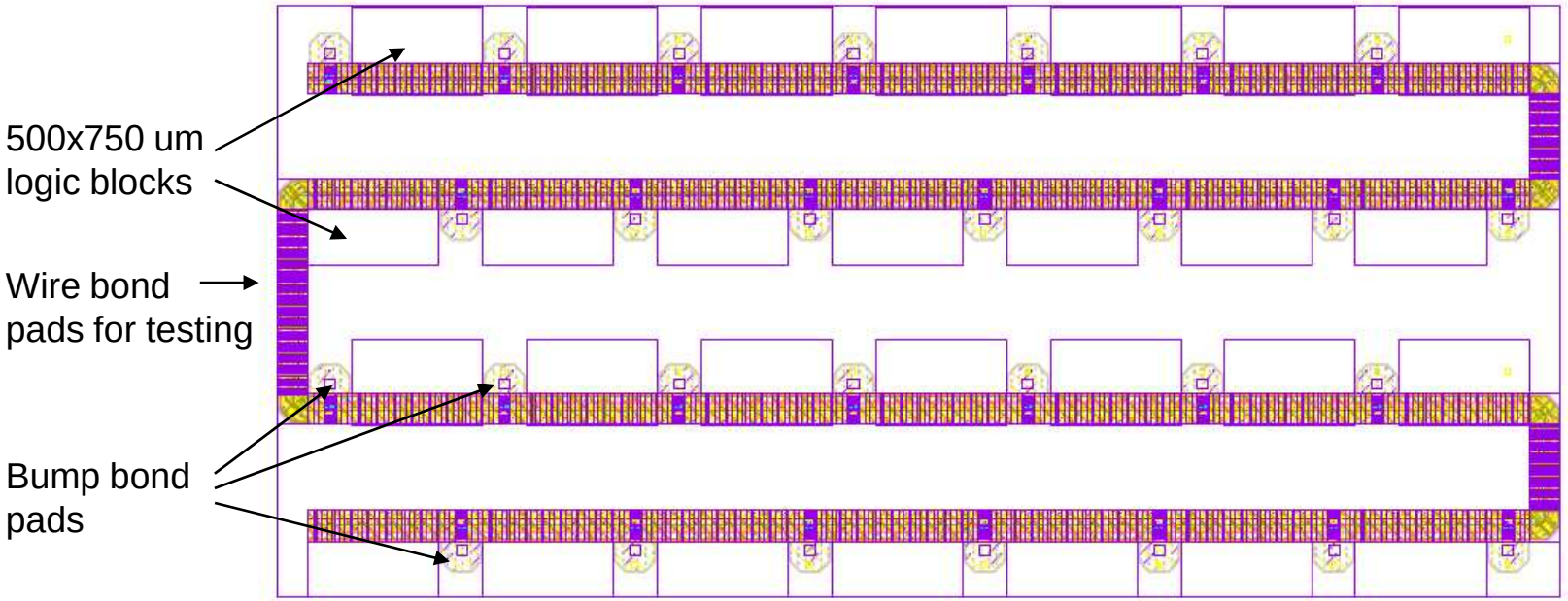
ASIC2 Sequencer Overview



ASIC2 Services



Example “1-seat” logic test structure



- 240um bump bondable pads on 1mm pitch
- Small wire-bond pads to test the generated logic signals
- Implement as many of the logic blocks and signal distribution as possible
- Folded design models a full-width logic slice serving a large array of pixels

ASIC2 Concept

- Logic columns
  - Power pads over the logic used to distribute global power supplies
- Central row of control logic
  - 500um profile

  - Bump Bond Pads for control & IO signals
    - Clocks
    - Synchronisation
    - Mode
    - Configuration
    - Serial data out
    - Power