Recent progress

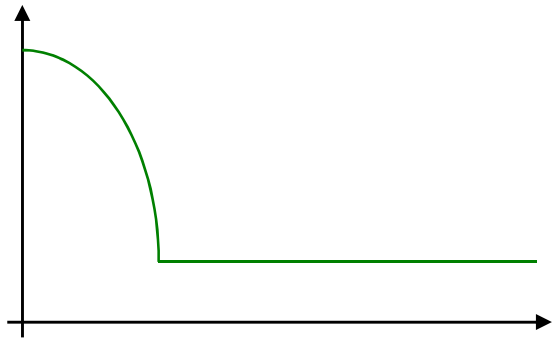
Jamie

29th Feb 08

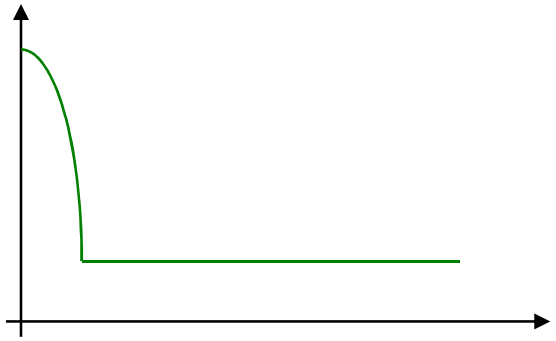
Shapers

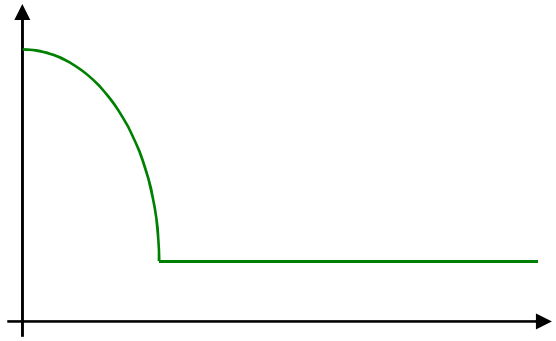
Samplers

-source



+source



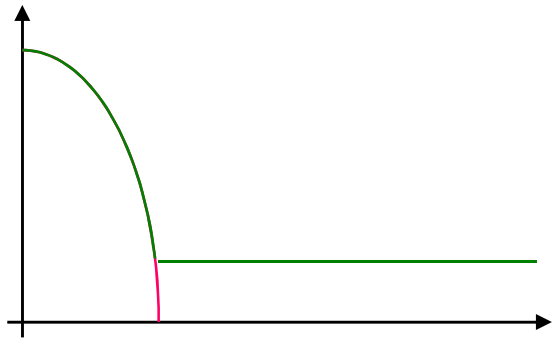


- What we got

Shapers

Samplers

-source



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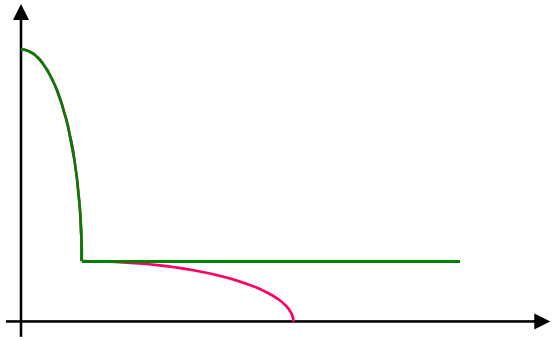
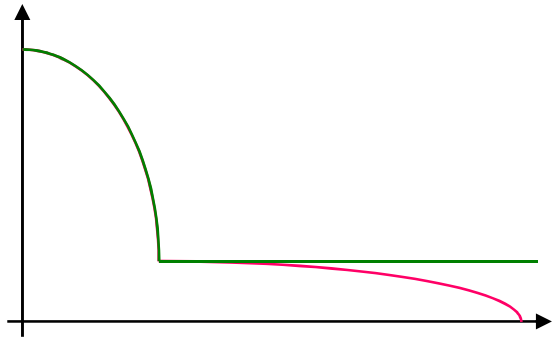




- What we expect

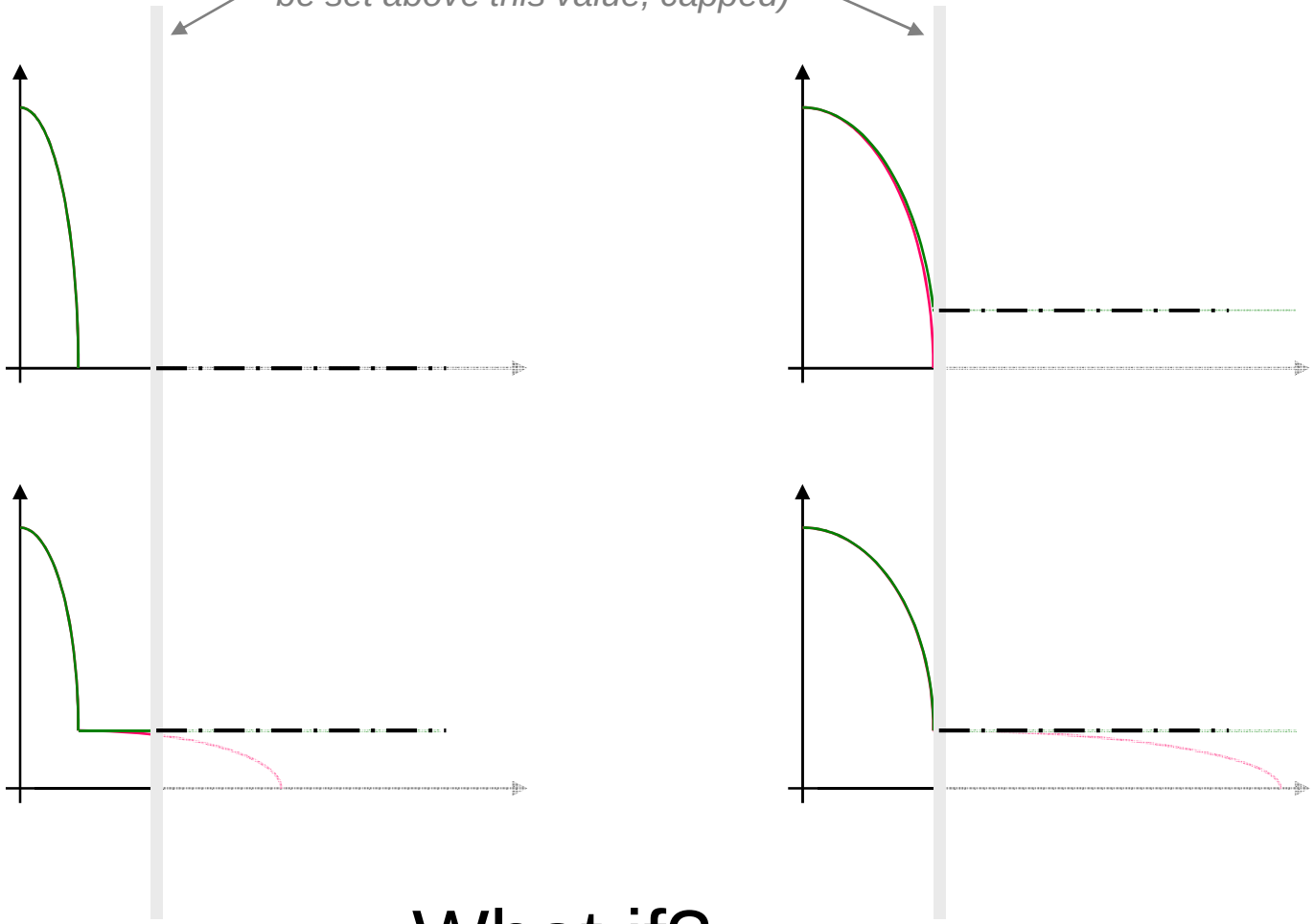
Shapers

Samplers

(sat limit means thresholds cannot be set above this value; capped)

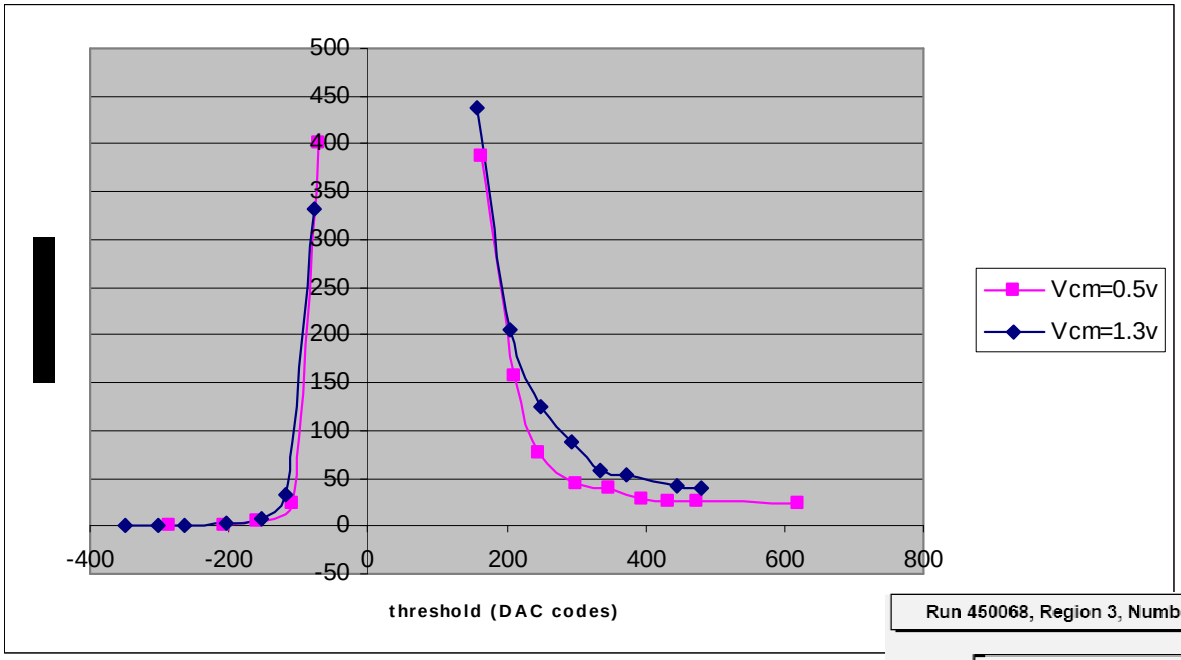
-source

+source



- What if?

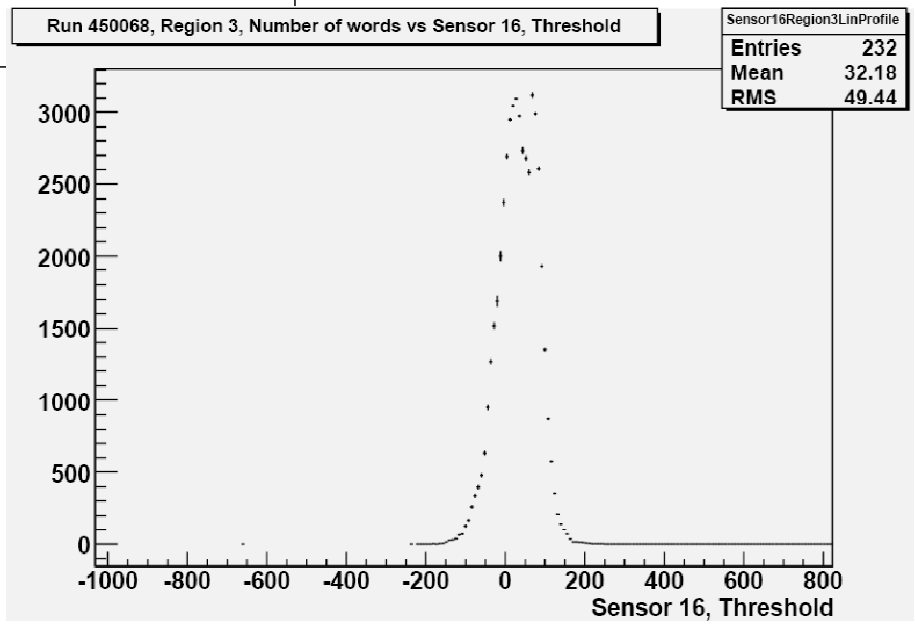
Manual Threshold Scan



To check there are no ill-effects from driving the threshold directly with the DACs, some PCB pins were lifted and the global VTH lines driven from a power supply.

(The number of hits was estimated from the typical time between ORE2 and ORE3 observed on the logic analyser)

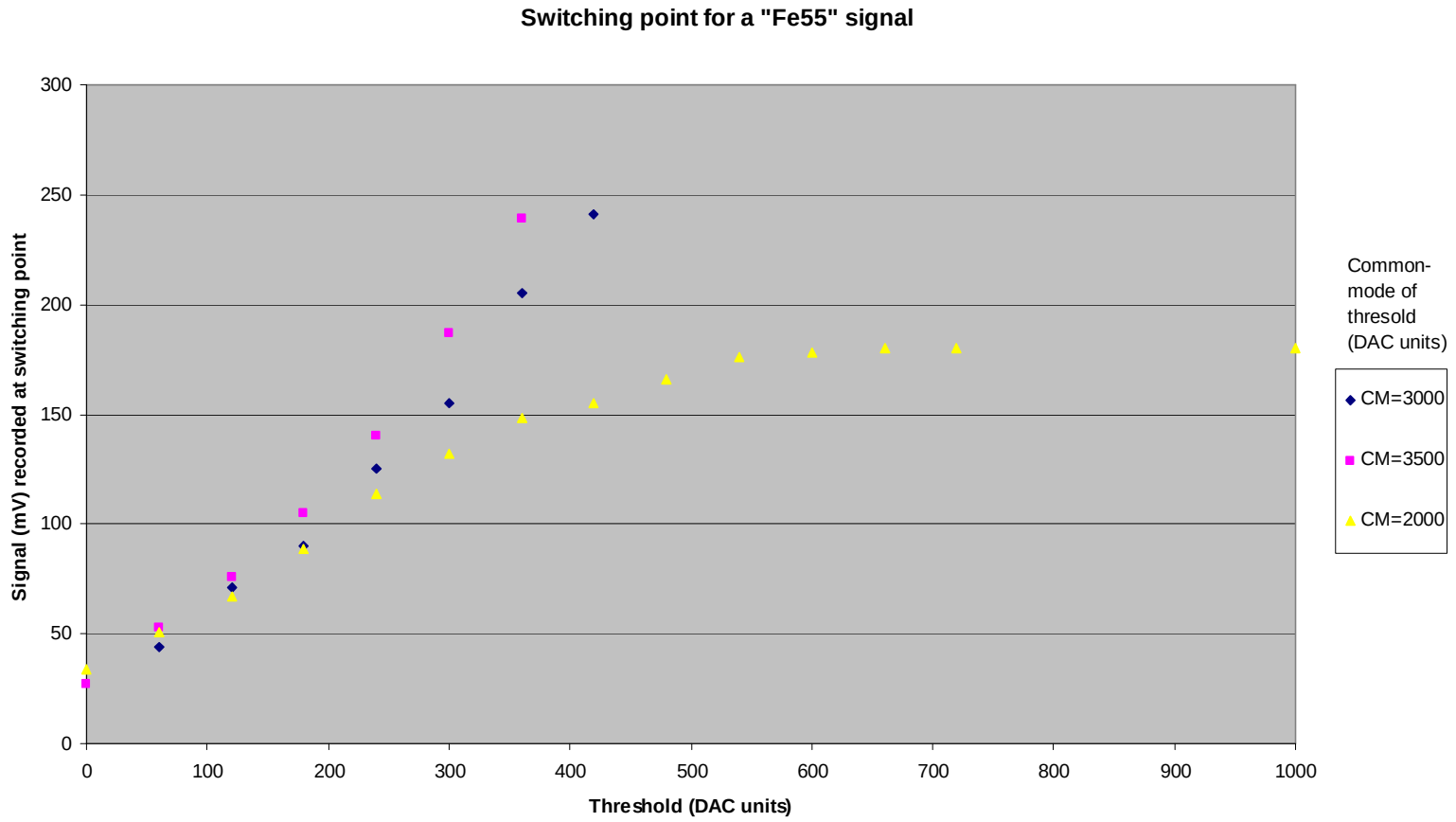
Sensor 16 (5um epi + DPW)



DAC pins were re-attached and an automated scan performed for comparison

Threshold Behaviour

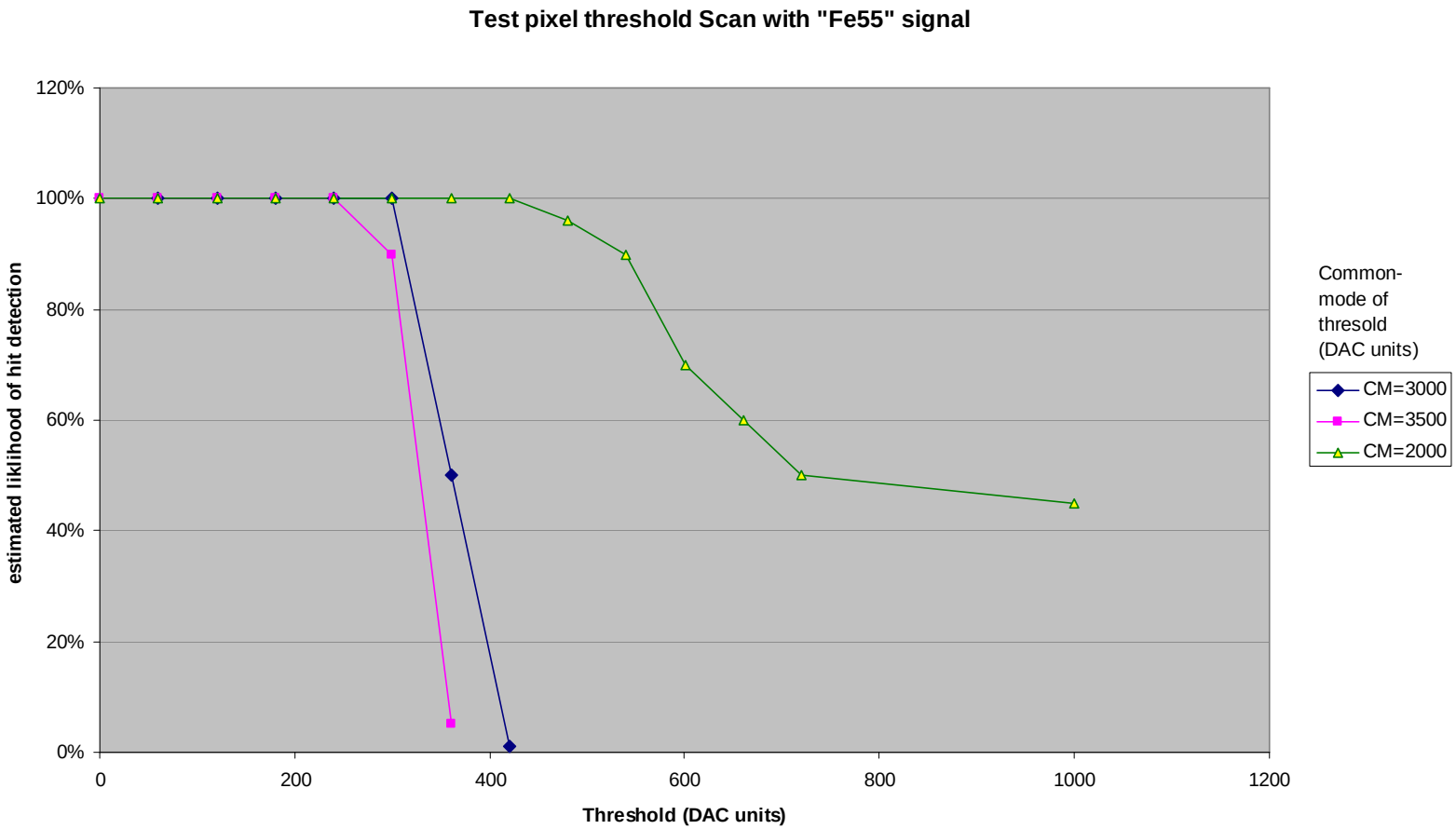
Test command: { diodeDrive 20 10 5 2600 2563 } injects a signal into the test pixel that gives a ~210mV step response, ie similar to Fe55 peak. The threshold is scanned (manually) and the output of the comparator observed with respect to the input: The value of (signal-reset) is plotted when the comparator fires.



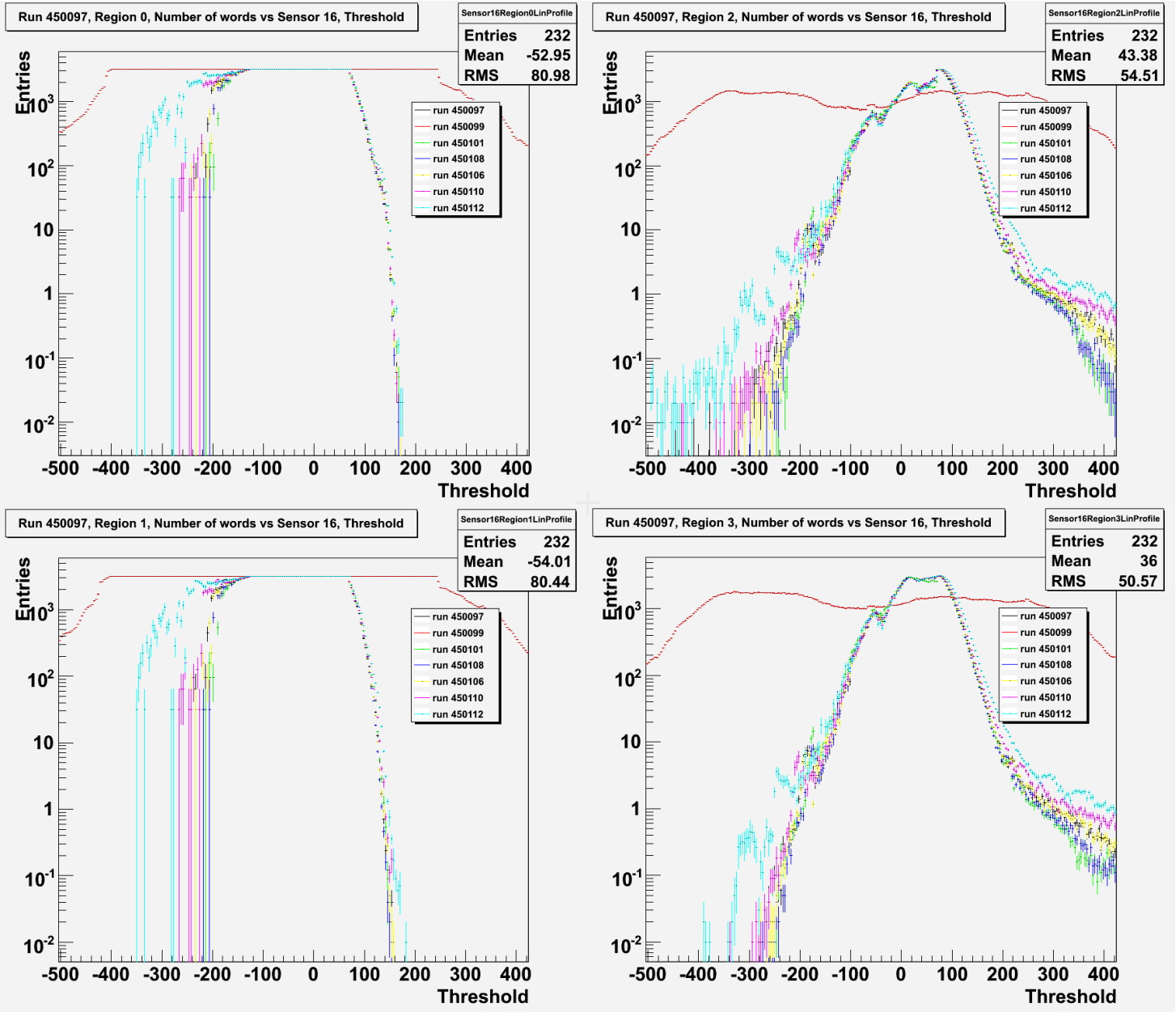
Doesn't show the upper range of the threshold, just how it detects a "Fe55-like" signal

Threshold Behaviour

Test command: { diodeDrive 20 10 5 2600 2563 } injects a signal into the test pixel that gives a ~210mV step response, ie similar to Fe55 peak. The threshold is scanned (manually) and the output of the comparator observed (by eye) on the oscilloscope: An estimate is made of the correct operation of the comparator (a value >0% and <100% indicates noise on the comparator output)

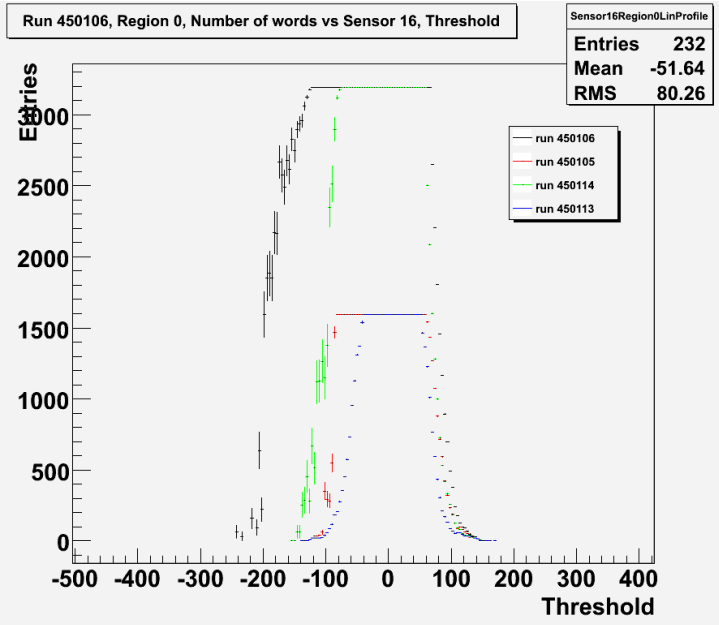


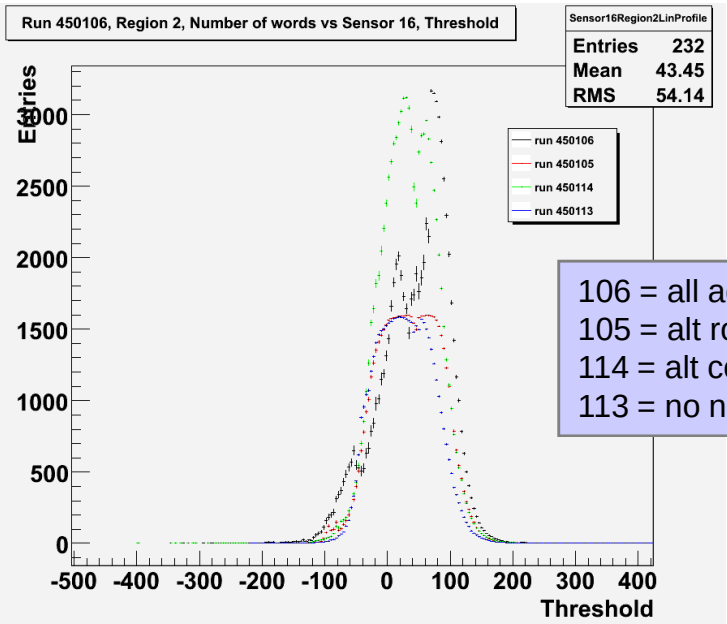
Threshold Common-Mode



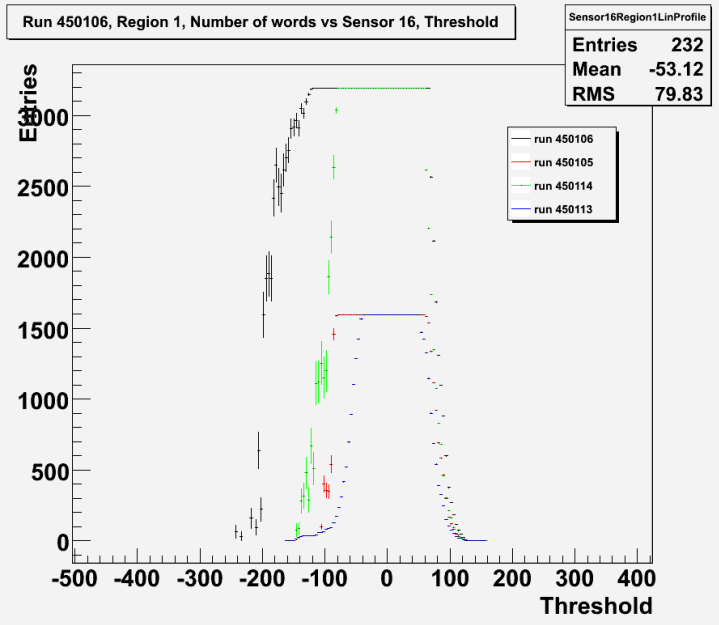
097 = 2048
099 = 3584
101 = 3072
108 = 2560
106 = 2048
110 = 1536
112 = 1024

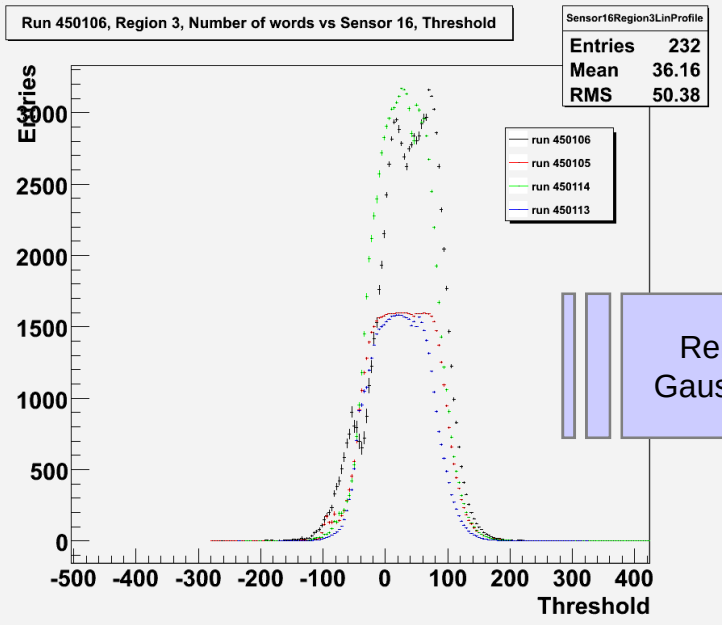
Some different masks





106 = all active
105 = alt rows masked
114 = alt cols masked
113 = no neighbours

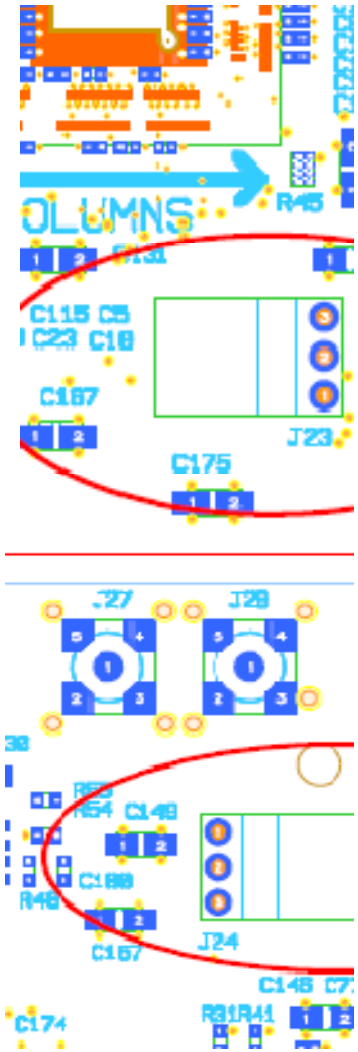




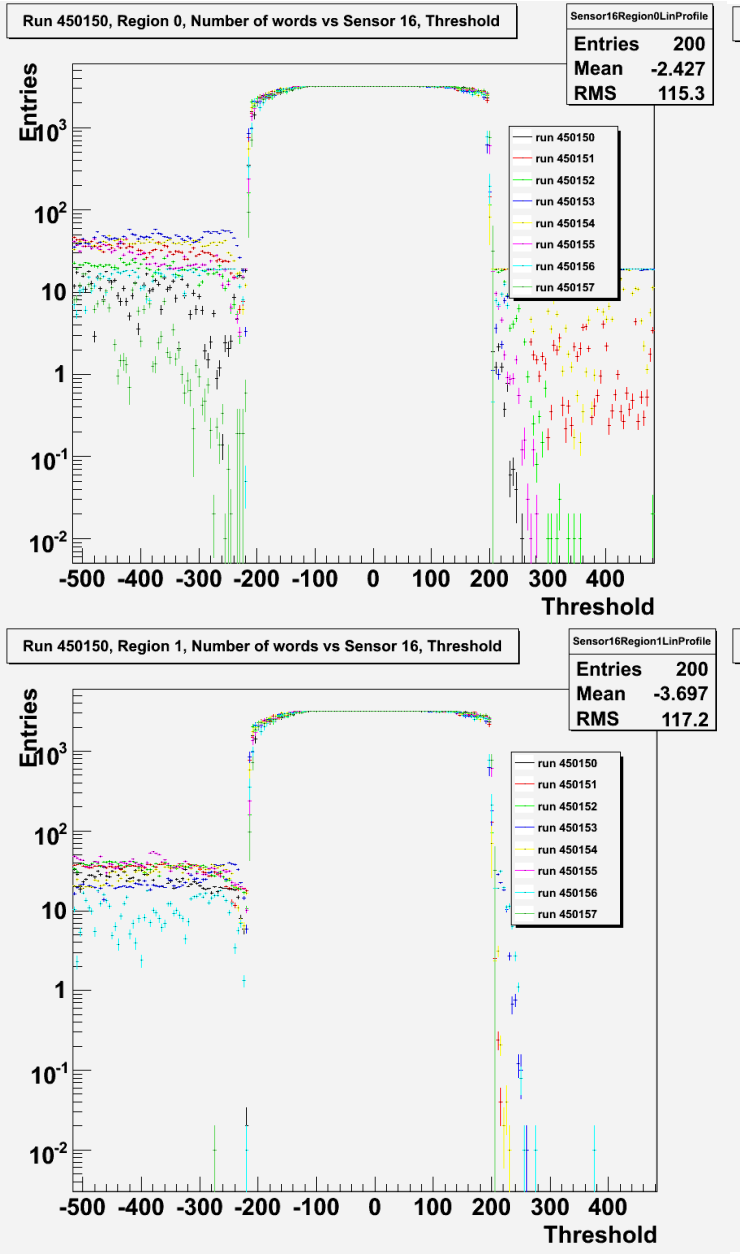
Renato's Gaussian fits

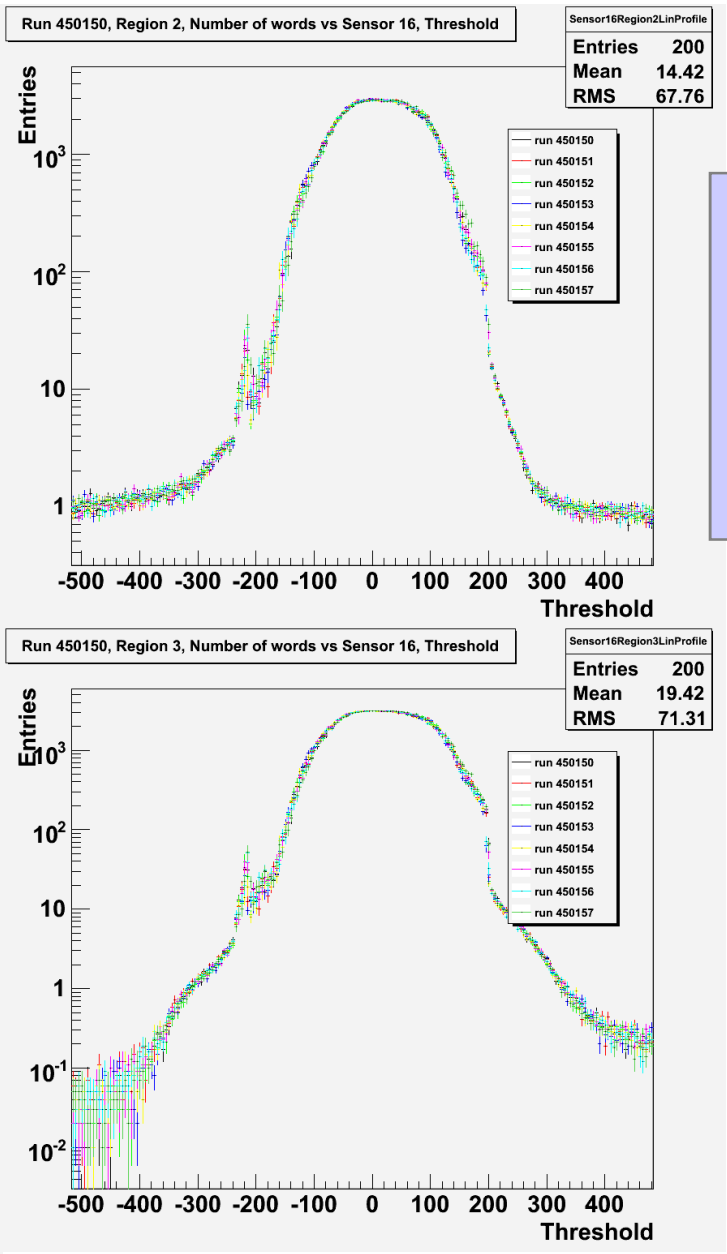
Jumper options

- J23: Substrate
  - GNDA (analog, default)
  - GNDD (digital)
  - NONE (floating)
- J24: VRST
  - VDDA1V8pix (default)
  - DAC
- Au BASE PLATE
  - Floating
  - Grounded



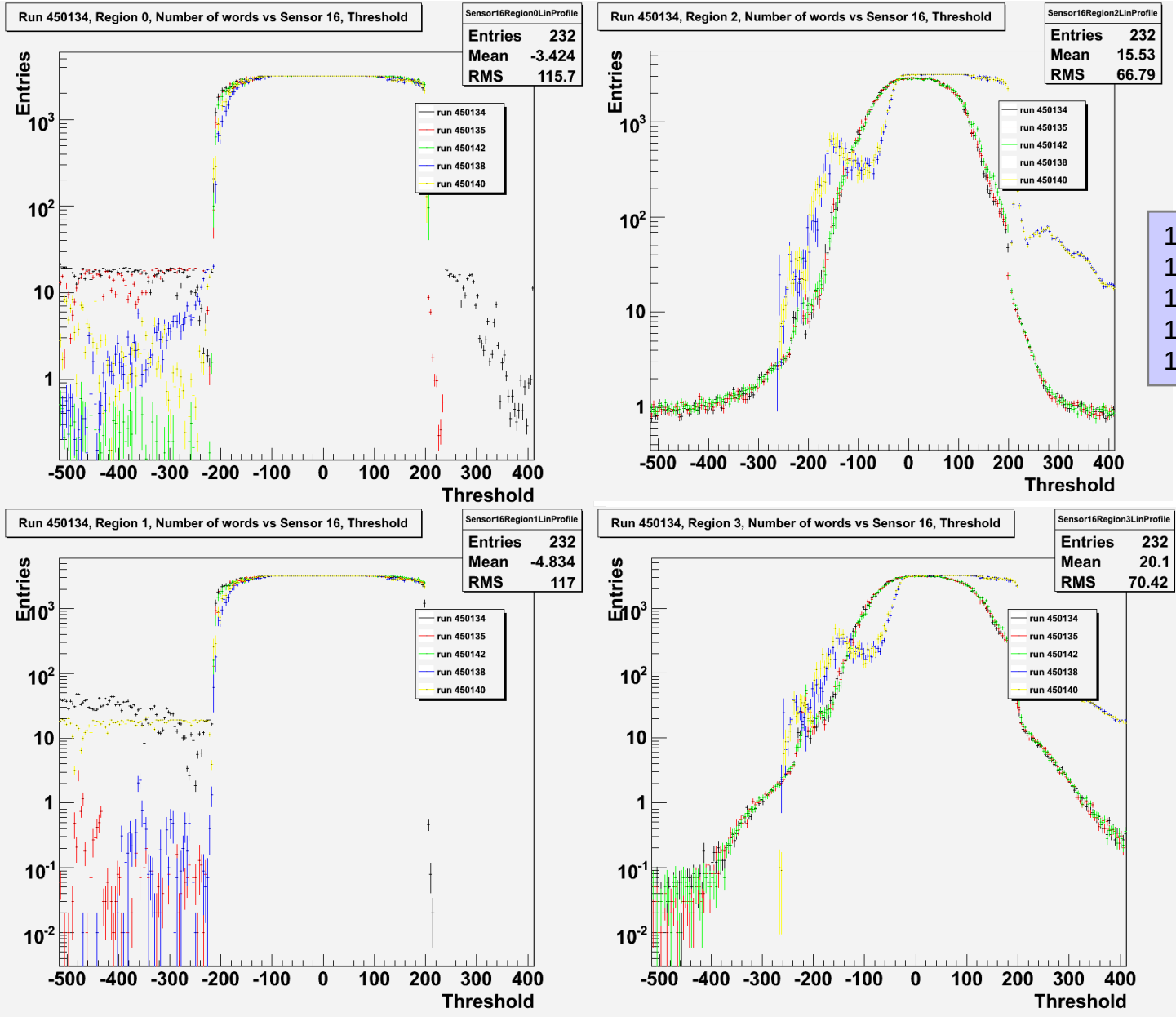
Substrate connection J23





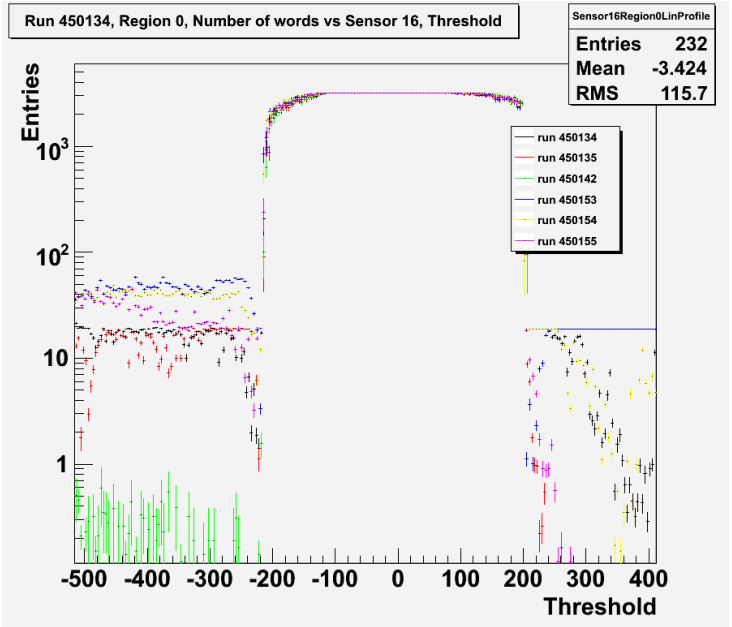
150	GNDD
151	
152	
153	GNDA
154	
155	
156	NONE
157	
158	

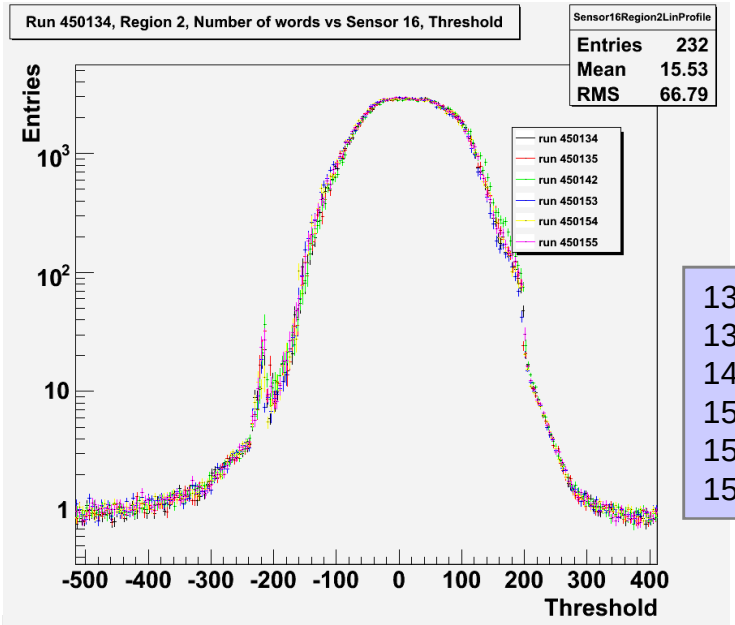
Vrst connection J24



134
135 } VDDA
142
138
140 } VDAC

Base plate grounding





134
135 } FLOAT
142

153
154 } GNDED
155