MAPS for a “Tera-Pixel” ECAL at the International Linear Collider

J.P. Crooks

Y. Mikami, O. Miller, V. Rajovic, N.K. Watson, J.A. Wilson
University of Birmingham
J.A. Ballin, P.D. Dauncey, A.-M. Magnan, M. Noy
Imperial College London
J.P. Crooks, B. Levin, M.Lynch, M. Stanitzki, K.D. Stefanov, R. Turchetta, M. Tyndel, E.G. Villani
STFC-Rutherford Appleton Laboratory

Science & Technology Facilities Council

CALICE Calorimeter for LC

Introduction

SiW ECAL for ILC

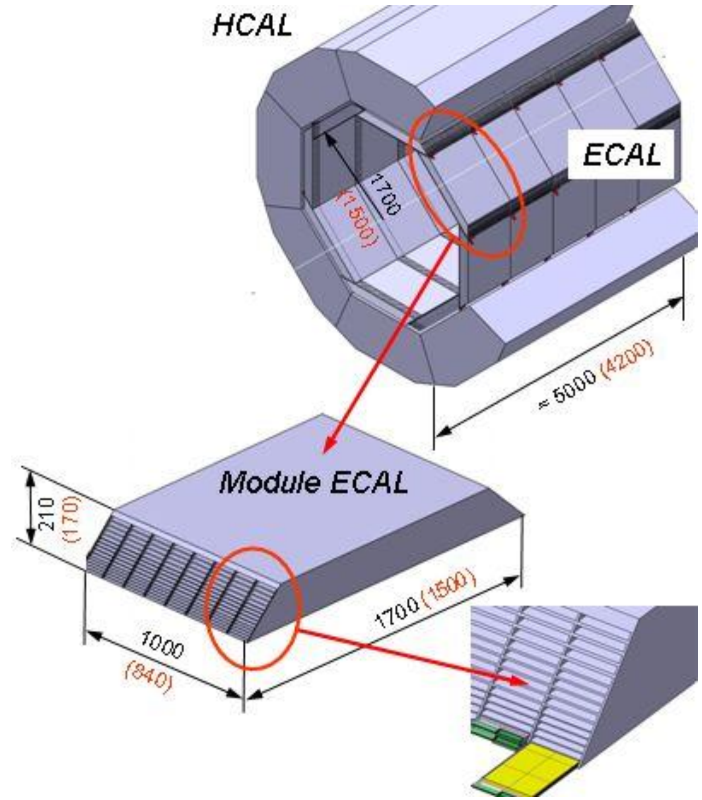
- 30 layers silicon & tungsten
- Prove Monolithic Active Pixel Sensor (MAPS) as a viable solution for the silicon!

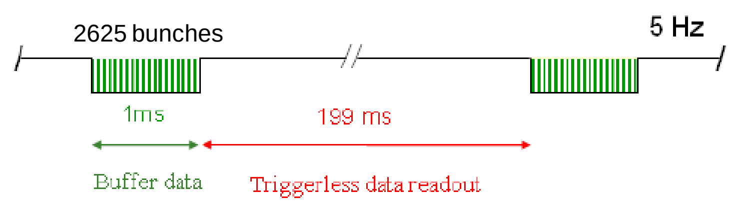
Machine operation

- 189ns min bunch spacing
- 199ms between bunch trains for readout

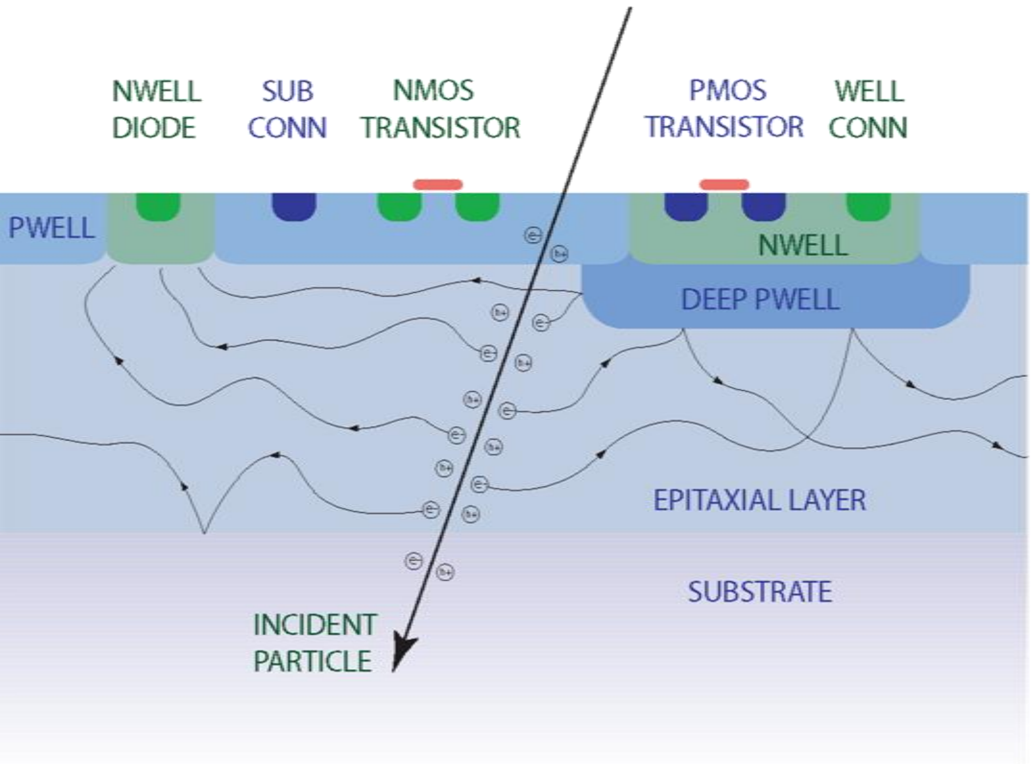
Sensor Specification

- Sensitive to MIP signal
- Binary readout from 50micron pixels
- Store timestamp & location of “hits”
- Noise rate 10^{-6}
- Design to hold data for 8k bunch crossings before readout





INMAPS Process



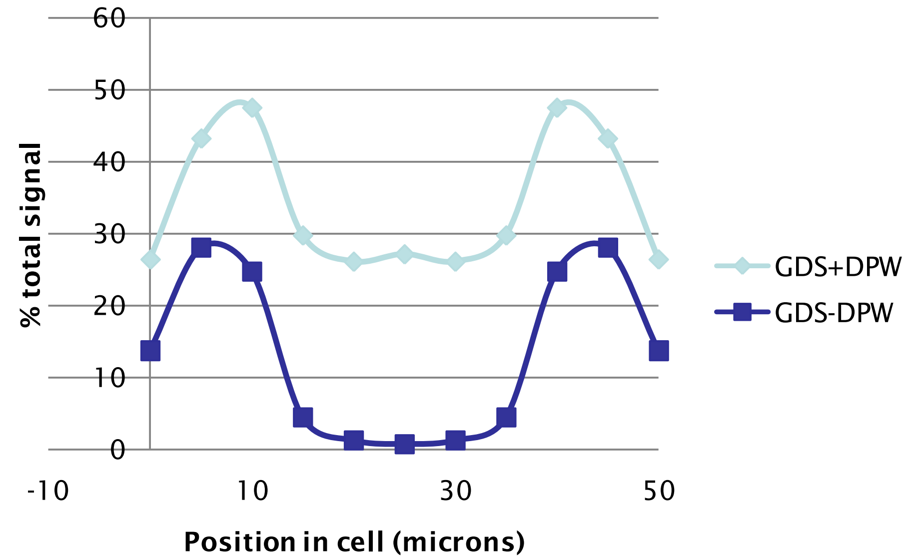
- Standard 0.18 micron CMOS
- 6 metal layers
- Analog & Digital VDD @ 1.8v
- 12 micron epitaxial layer
- Additional module: Deep P-Well
  - Developed by foundry for this project
  - Added beneath all active circuits in the pixel
  - Should reflect charge, preventing unwanted loss in charge collection efficiency
- Device simulations show conservation of charge
- Test chip processing variants
  - Sample parts were manufactured with/without deep p-well for comparison

Device Simulations

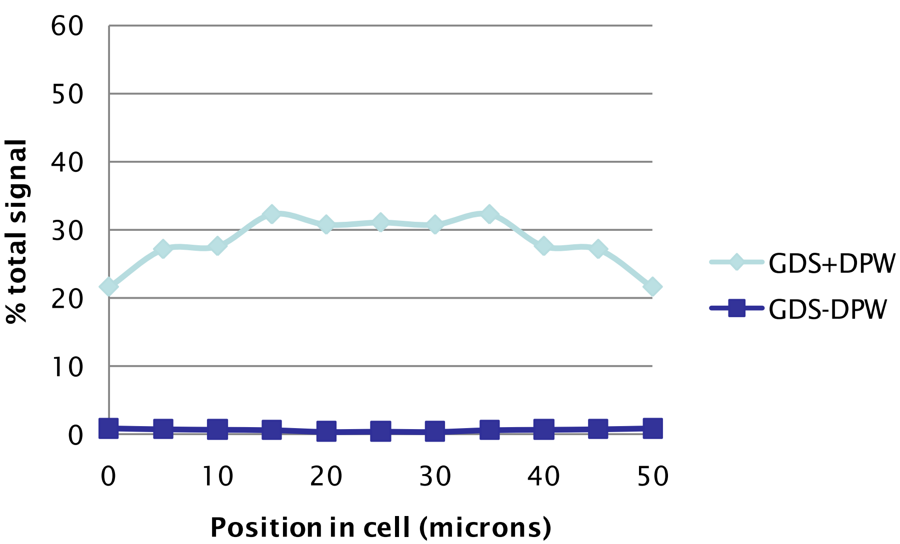
TCAD model of 3x3 pixels

- Charge injected in 21 reference points
- Response at each diode in 3x3 pixels recorded
    - Charge collected
    - Collection time (to 90%)
- Profile mirrored to create full 150x150um terrain

Profile B; through cell

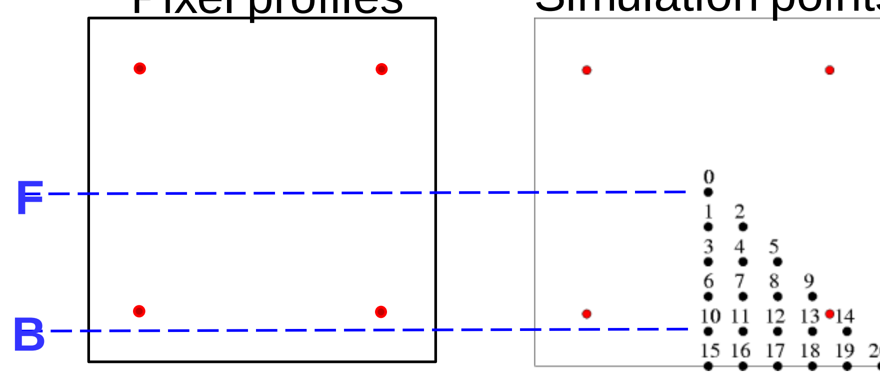


Profile F; through cell



Pixel profiles

Simulation points

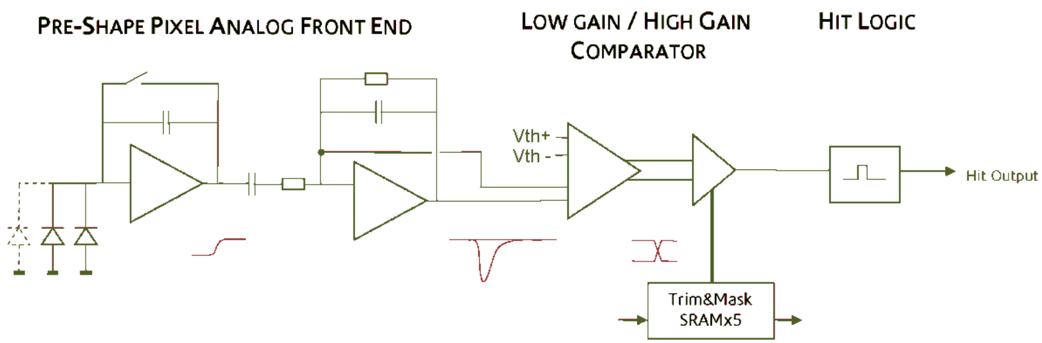


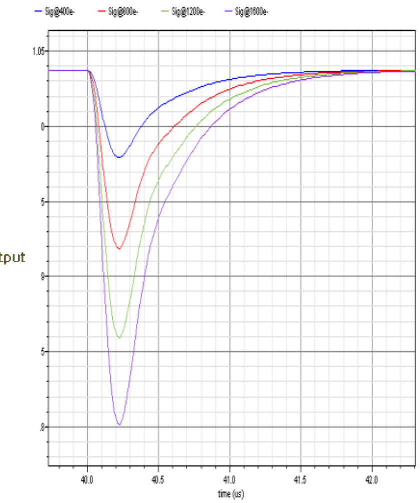
Pixel Architectures

preShape

- Gain 94uV/e
- Noise 23e-
- Power 8.9uW

- 150ns “hit” pulse wired to row logic
- Shaped pulses return to baseline

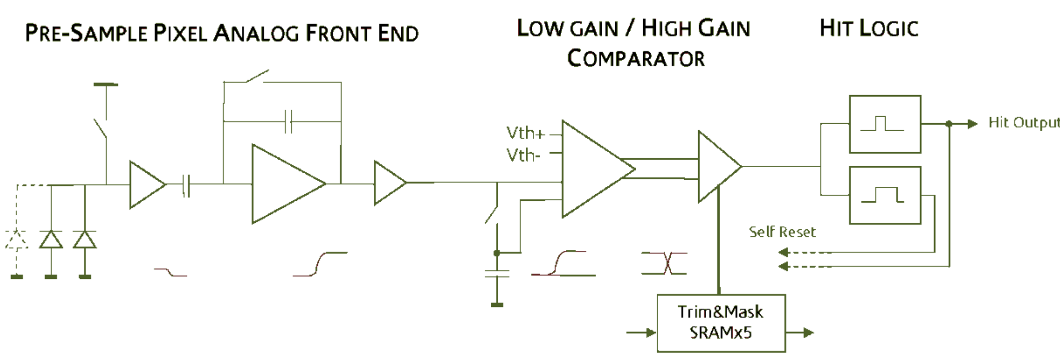


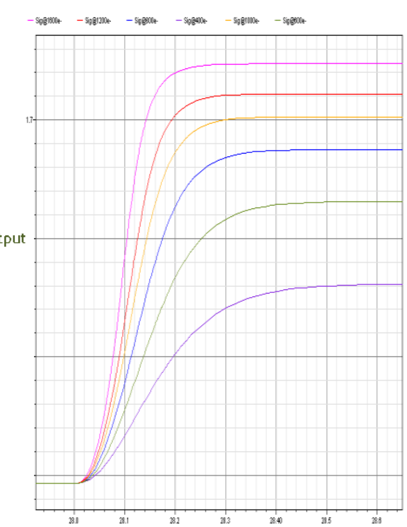


preSample

- Gain 440uV/e
- Noise 22e-
- Power 9.7uW

- 150ns “hit” pulse wired to row logic
- Per-pixel self-reset logic



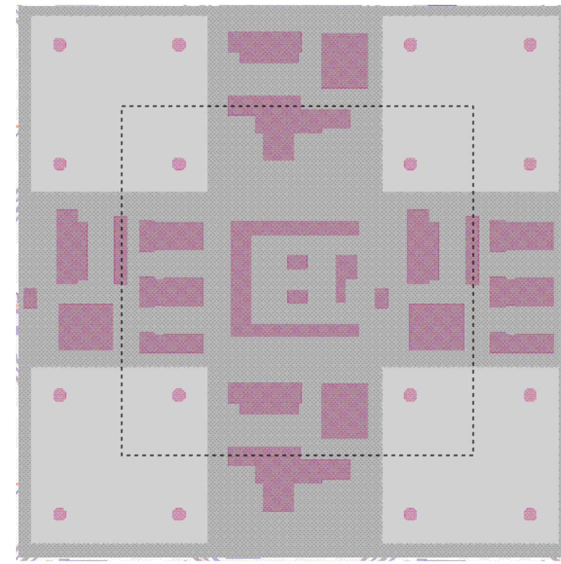


Pixel Layouts

preShape Pixel

- 4 diodes
- 160 transistors
- 27 unit capacitors

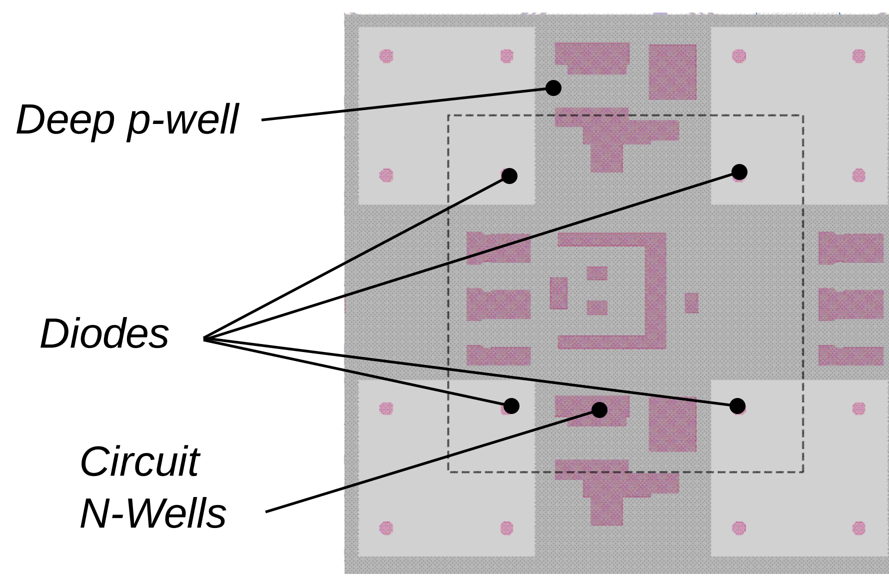
- Configuration SRAM
  - Mask
  - Comparator trim (4 bits)
- 2 variants: subtle changes to capacitors



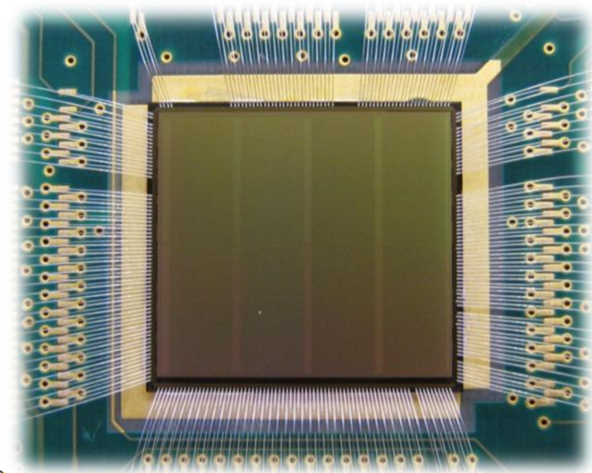
preSample Pixel

- 4 diodes
- 189 transistors
- 34 unit capacitors
- 1 resistor (4Mohm)

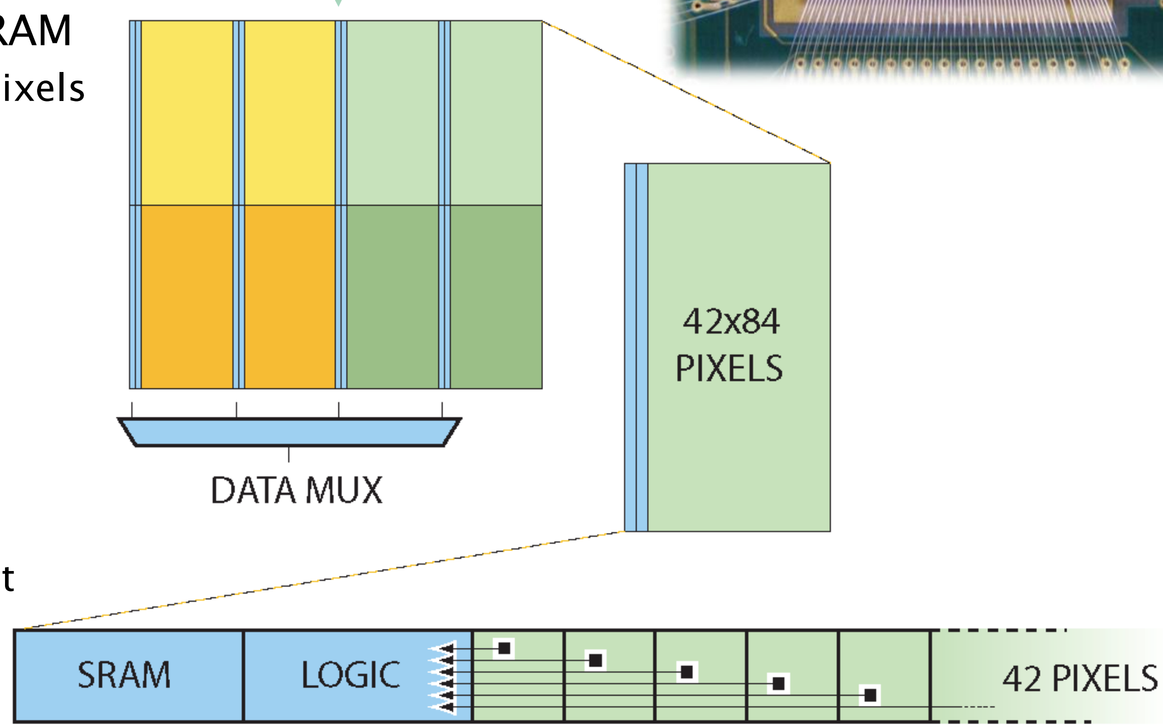
- Configuration SRAM
  - Mask
  - Comparator trim (4 bits)
- 2 variants: subtle changes to capacitors



Test Chip Architecture



- 8.2 million transistors
- 28224 pixels; 50 microns; 4 variants
- Sensitive area 79.4mm2
  - *of which 11.1% "dead" (logic)*



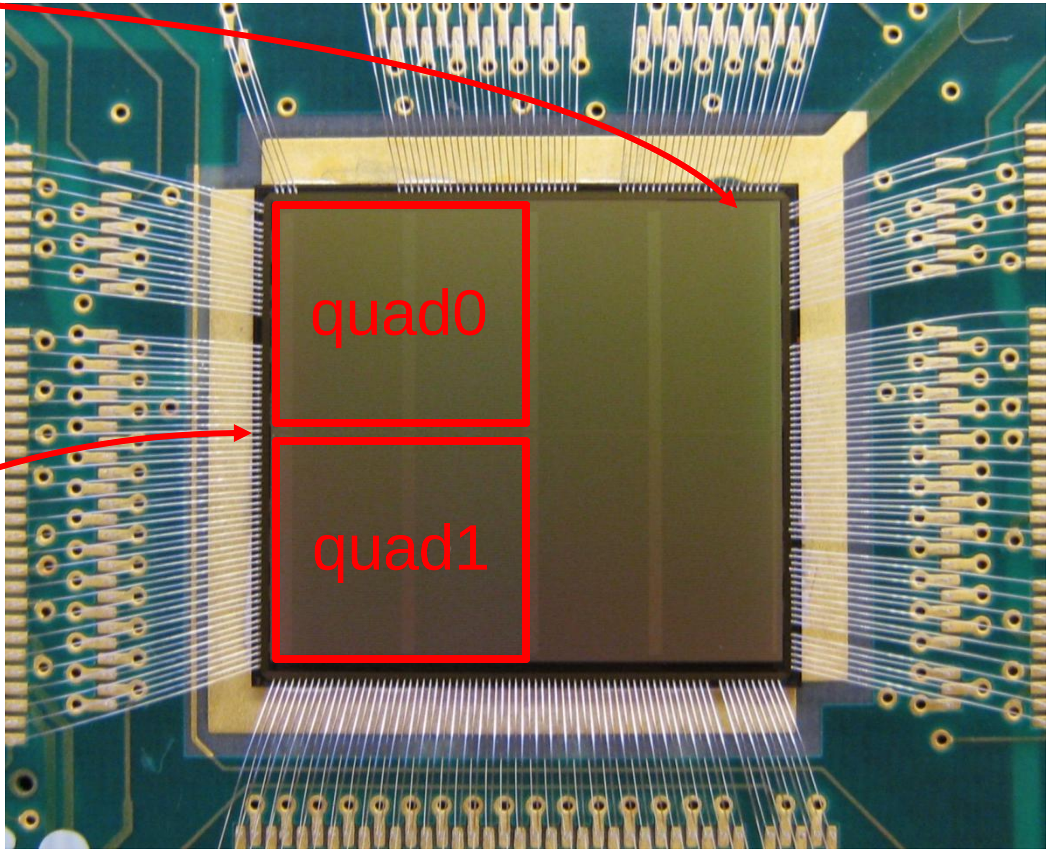
- Four columns of logic + SRAM
  - Logic columns serve 42 pixels
  - Record hit locations & timestamps
  - Local SRAM
- Data readout
  - Slow (<5Mhz)
  - Current sense amplifiers
  - Column multiplex
  - 30 bit parallel data output

Sensor Testing: Overview

Test pixels
- preSample pixel variant
- Analog output nodes
- Fe55 stimulus
- IR laser stimulus

Single pixel in array
- Per pixel masks
- Fe55 stimulus
- Laser Stimulus

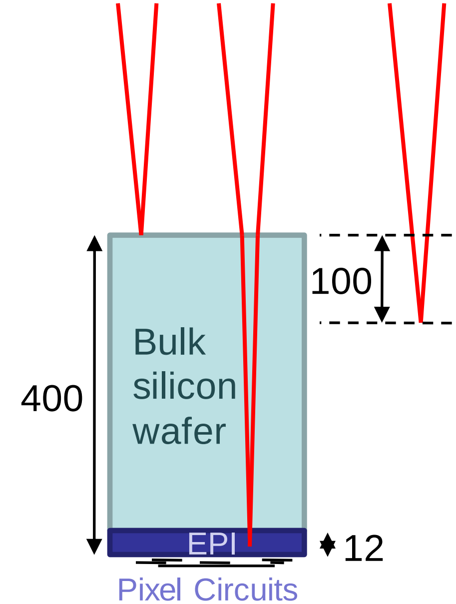
Full pixel array
- preShape (quad0/1)
- Pedestals & trim adjustment
- Gain uniformity
- Crosstalk
- Beam test

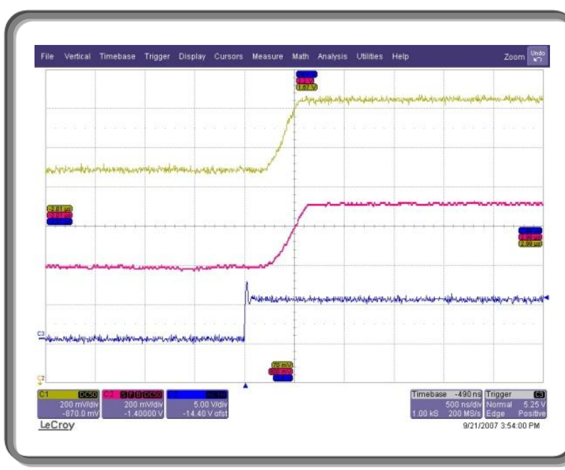


Test pixels: Laser Stimulus

- 1064nm pulsed laser
- 2x2um square area of illumination at focal point
  - Simulates point-charge deposit in pixel
- Illuminate back of sensor
- Silicon is ~transparent at this λ
- Adjust focus to hit the EPI layer
  - Account for refractive index!
- Scan XY position to 1um accuracy
- Test pixels & laser run asynchronously
- Oscilloscope triggered by laser sync pulse shows analog response from test pixel
- Measure (histogram)
  - Amplitude
  - Time delay

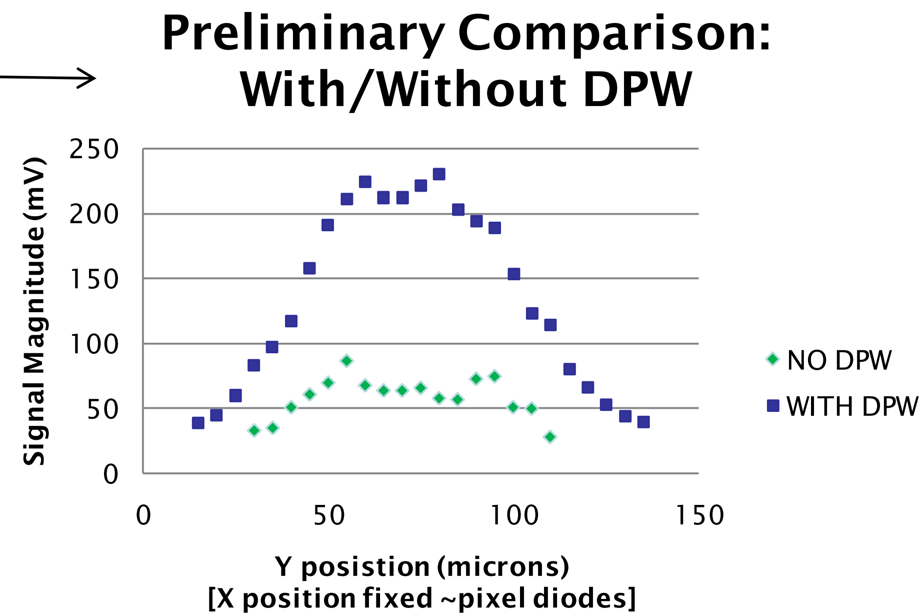
    = (System Delay) + (charge collection)

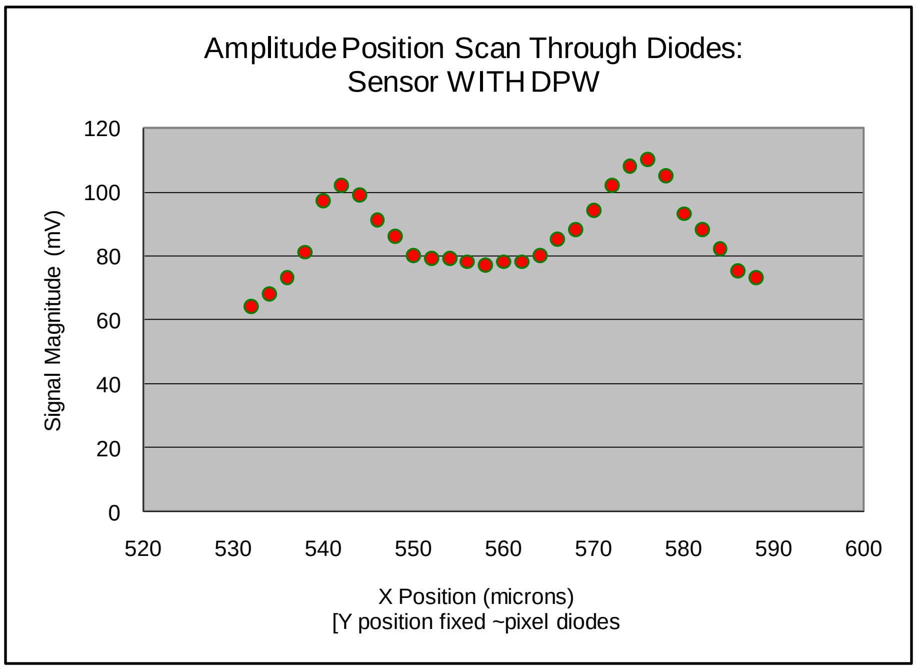




Test pixels: Laser Stimulus

- First look (Nov '07)
  - without / with DPW
  - 4x4um spot, 5um steps
  - Poor focussing!
- Recent scans
  - Optimised Focus
  - 2x2um spot, 2um steps

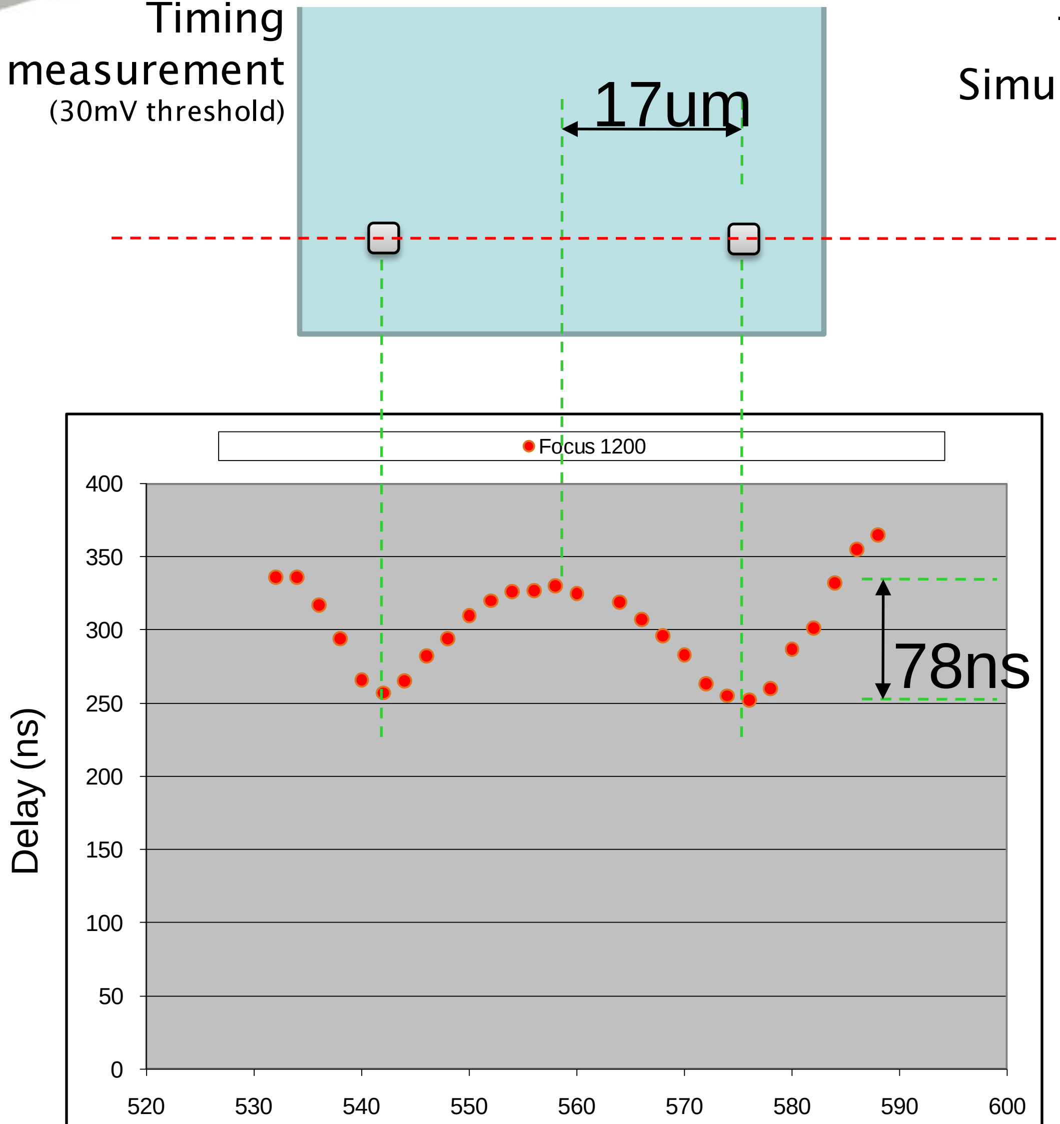




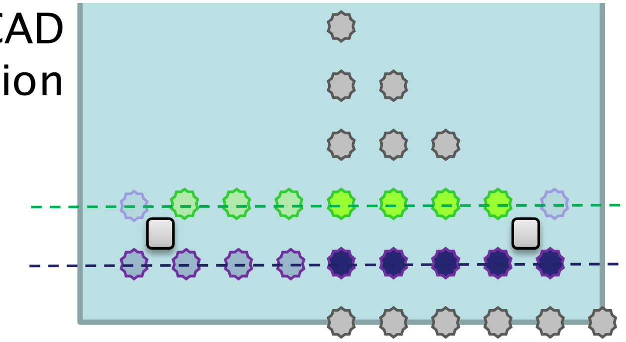
- Automated laser profile of full test pixel area begins…
  - With/without DPW
  - Different depths epi

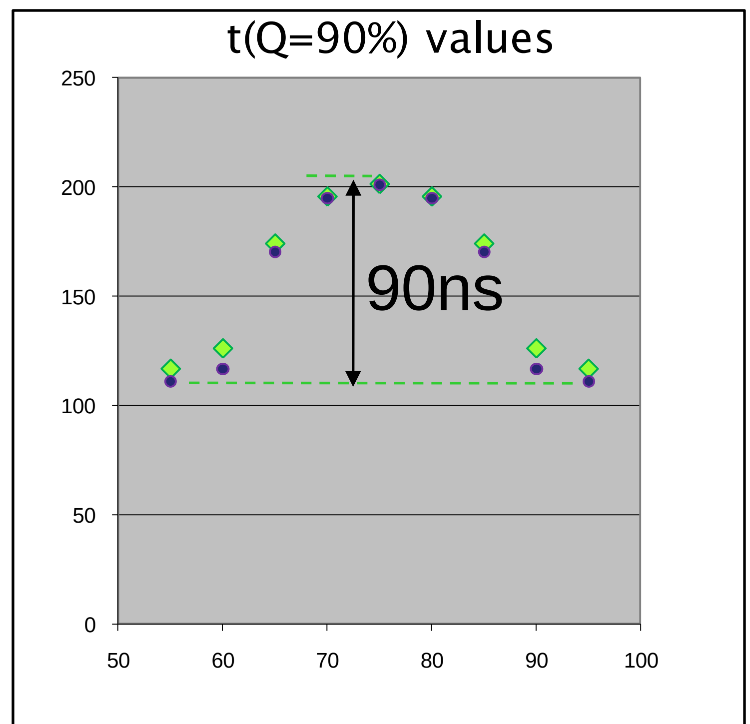
Test pixels: Laser Stimulus

Timing measurement
(30mV threshold)



TCAD Simulation

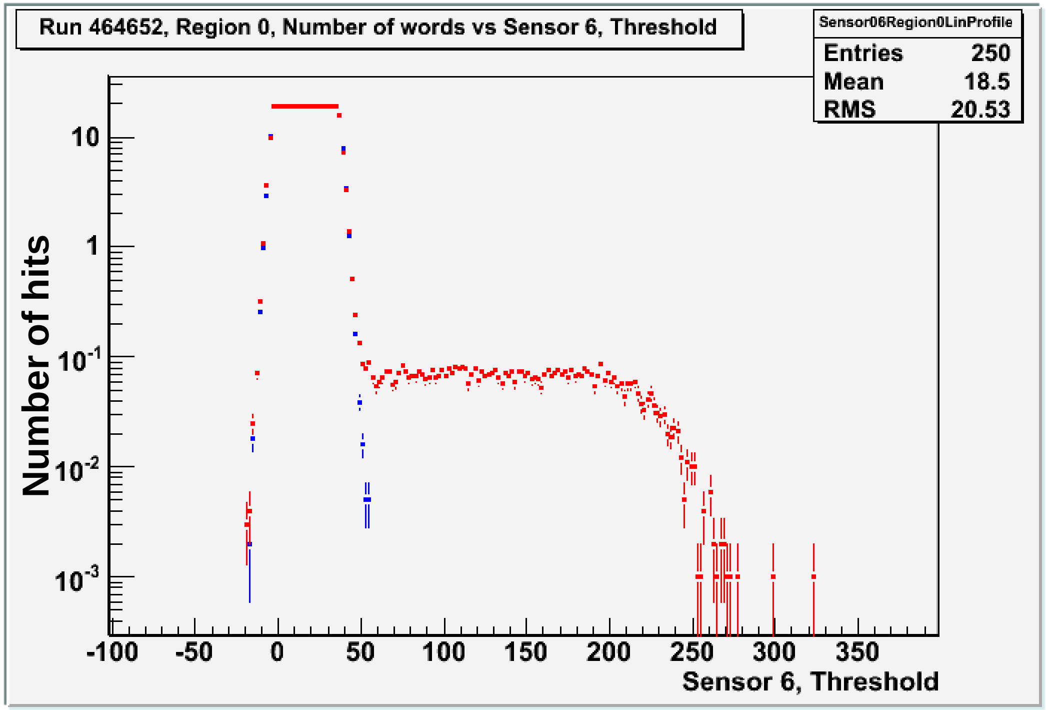




Evaluating single pixel performance

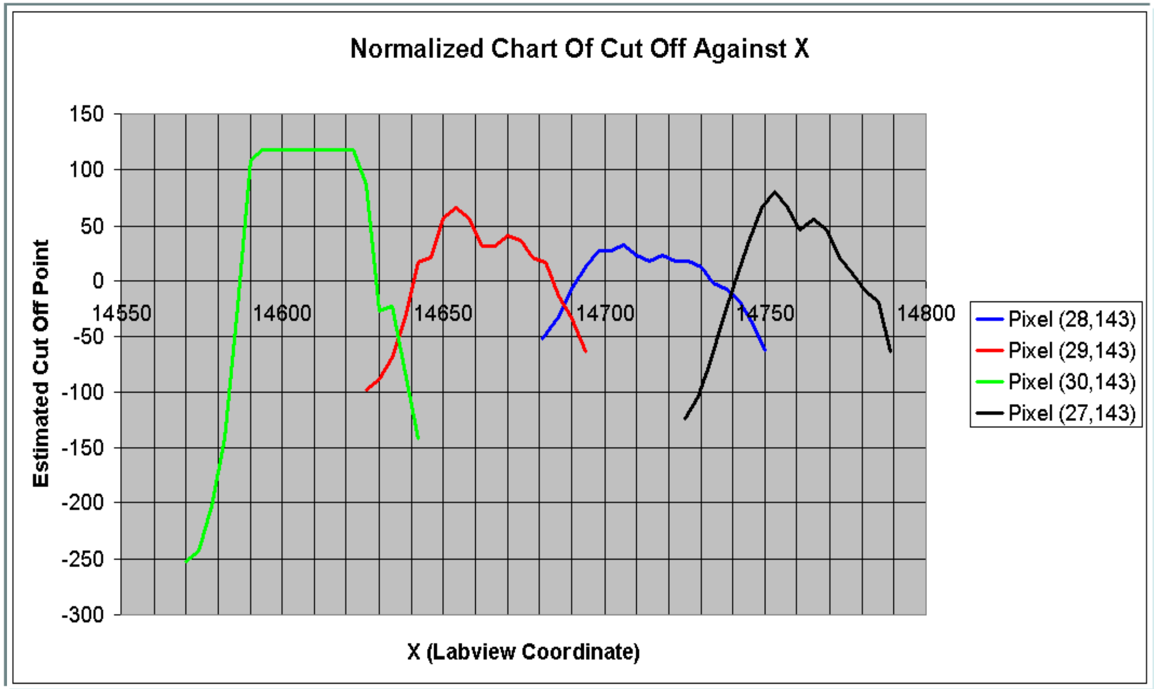
- Binary readout from pixels in the array
  - Can mask individual pixels
- Evaluated with a threshold scan…
  - Record #hits for a given threshold setting
  - 1 threshold unit ~0.4mV
  - Low thresholds → noise hits
  - Max #hits defined by memory limit *(=19 per row)*
  - Comparator is edge-triggered
    - Very small or negative thresholds don't trigger comparator
  - Signal should generate hits at higher thresholds than the noise
  - No hits expected for very high thresholds

Single active pixel
with/without laser firing



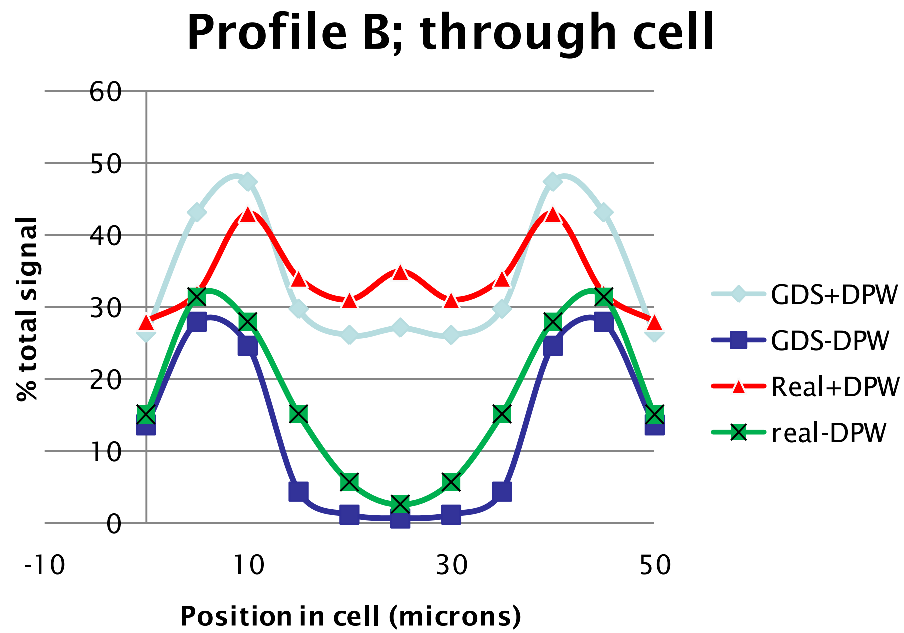
Single Pixel in Array: Laser/Alignment

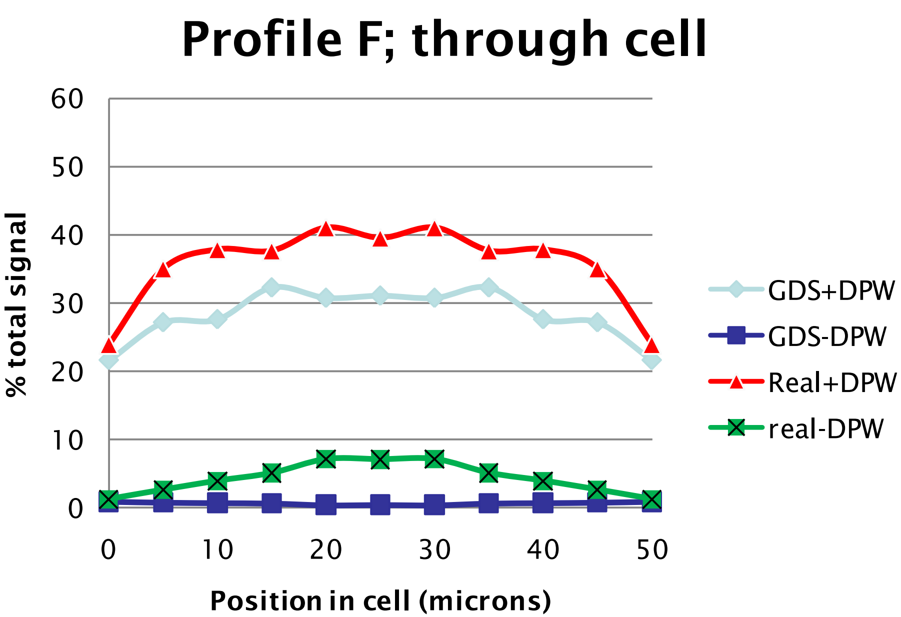
- Use laser for alignment
  - Back of sensor has no features for orientation
  - Mounting is not necessarily square to <1um
  - Laser position scans in X & Y
  - Threshold scan technique
  - Estimate signal magnitude from drop-off
    - By eye
    - By function fit?

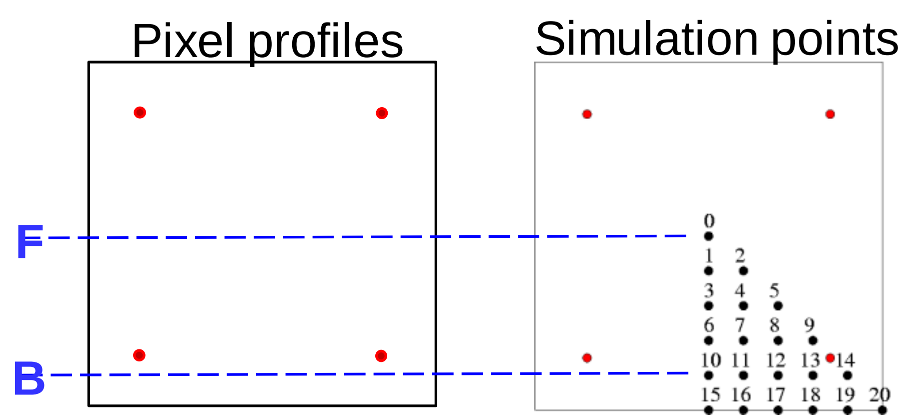


Single Pixel in Array: Laser Stimulus

- Amplitude results
  - With/without deep pwell
  - Compare
    - Simulations “GDS”
    - Measurements “Real”

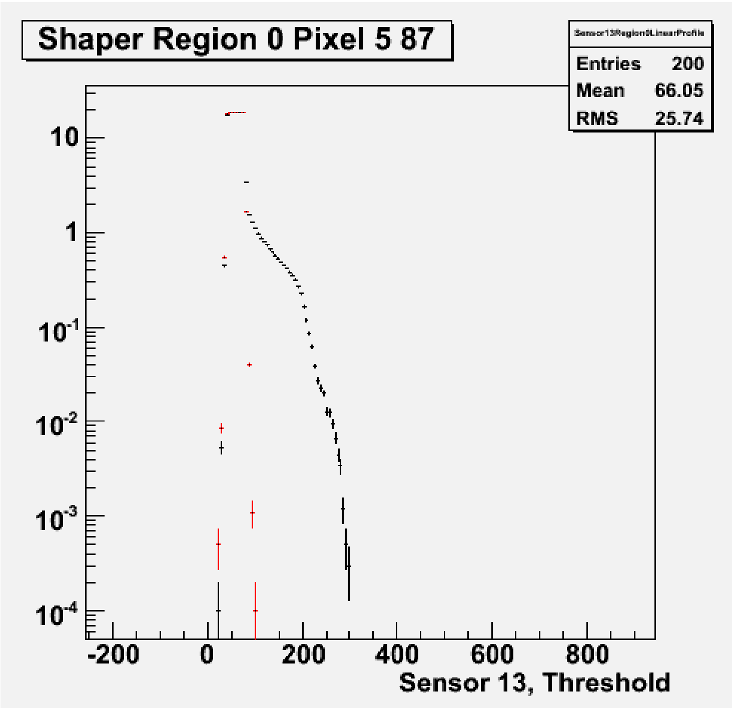


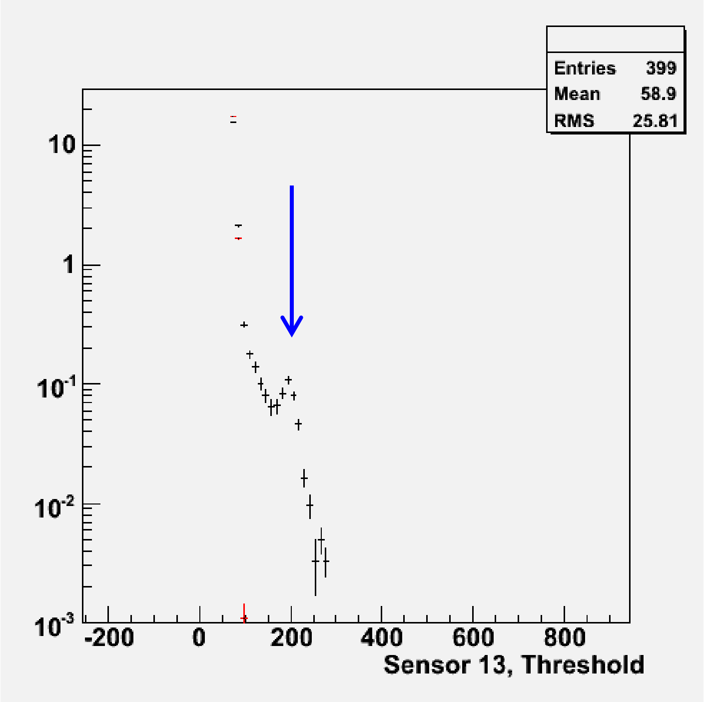




Single Pixel in Array: ^{55}Fe Source

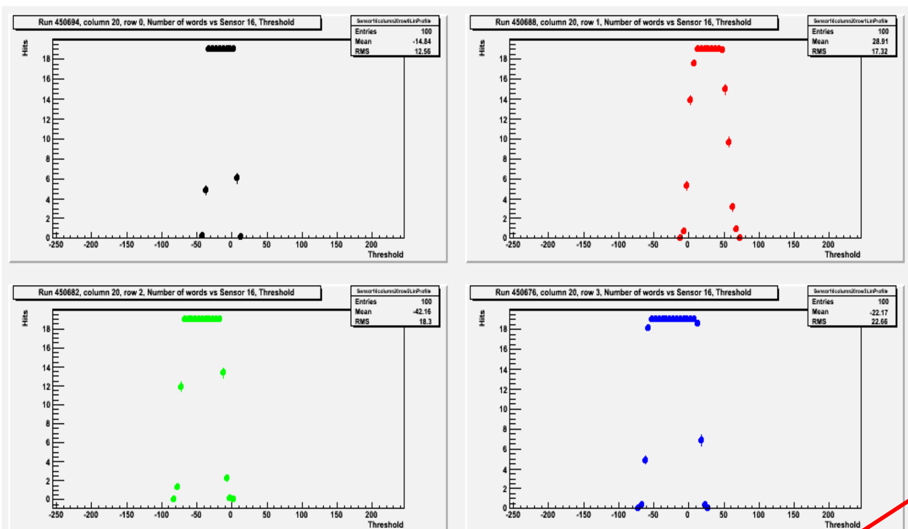
- ^{55}Fe gives 5.9keV photon
  - Deposits all energy in ~1μm^3 volume in silicon; 1640e$^-$
  - Sometimes will deposit maximum energy in a single diode and no charge will diffuse
    → absolute calibration!
- Binary readout from pixel array
  - Need to differentiate distribution to get signal peak in threshold units (TU)
  - Differential approximation

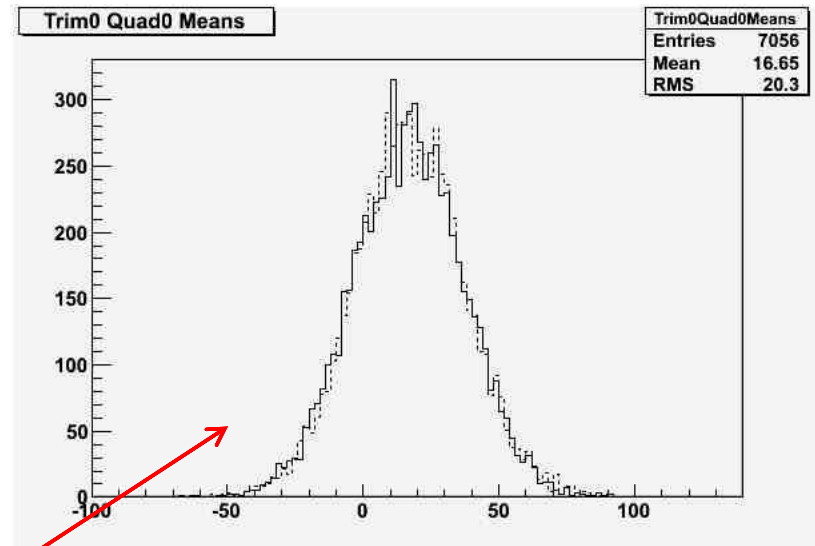




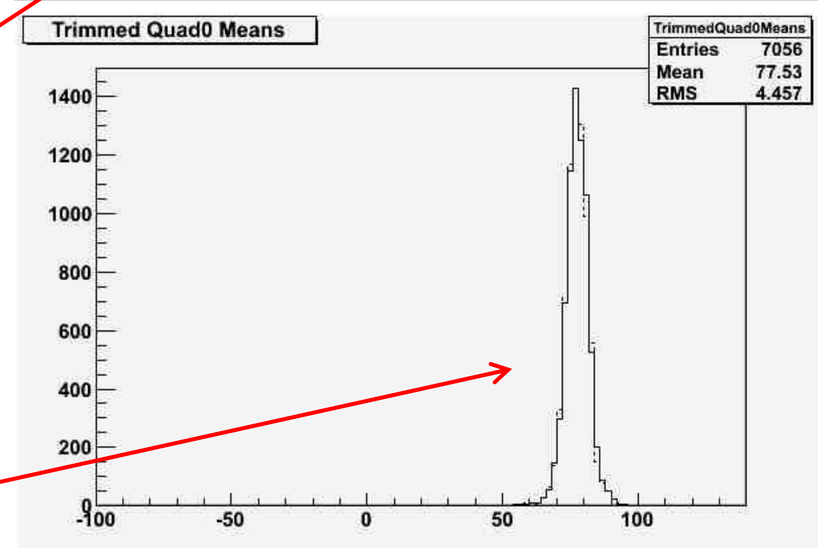
Array of PreShape Pixels: Pedestals

- Threshold scan of individual pixels
- Note differing threshold scans of noise!



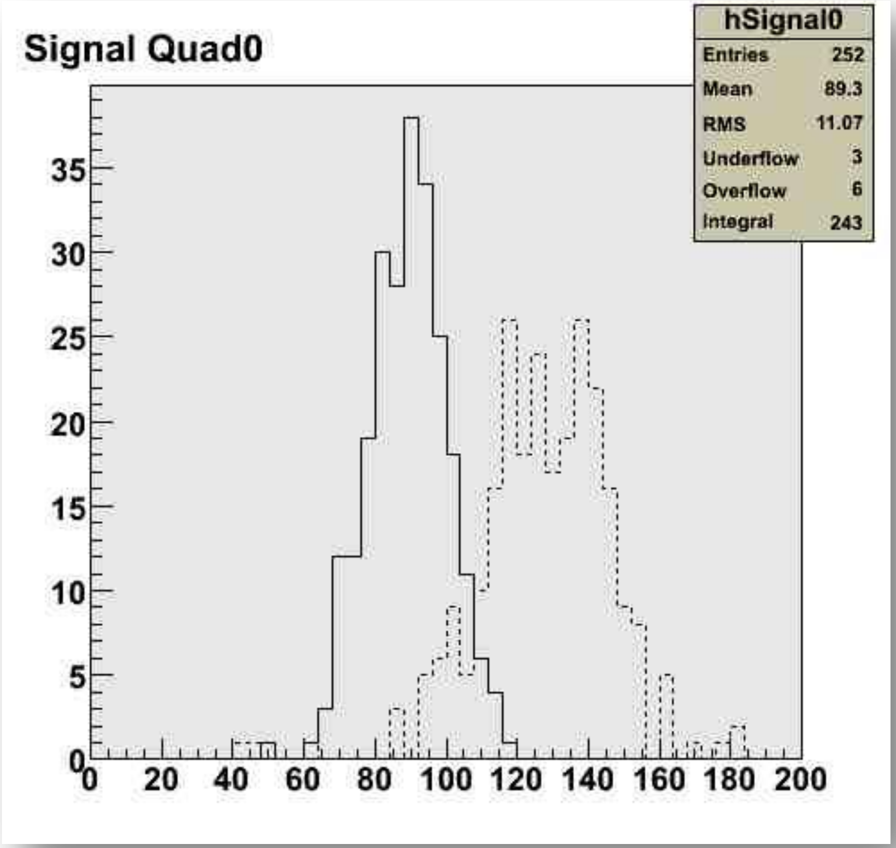


- Plot the distribution of pedestals
  - Falling edge
- Calculate necessary trim adjustment
- Per-pixel trim file
  - uni-directional adjustment
- Re-scan pixels individually with trims
- Re-plot the distribution of pedestals



Array of PrePhape Pixels: Gains

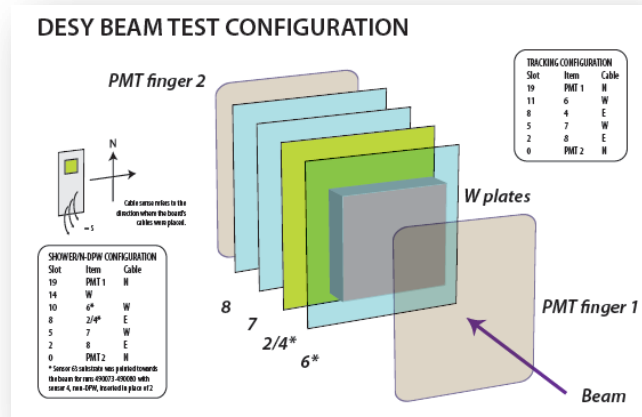
- Use laser to inject fixed-intensity signal into many pixels
- Relative position should be equivalent for each pixel scanned
- Adjust/trim for known pixel pedestals

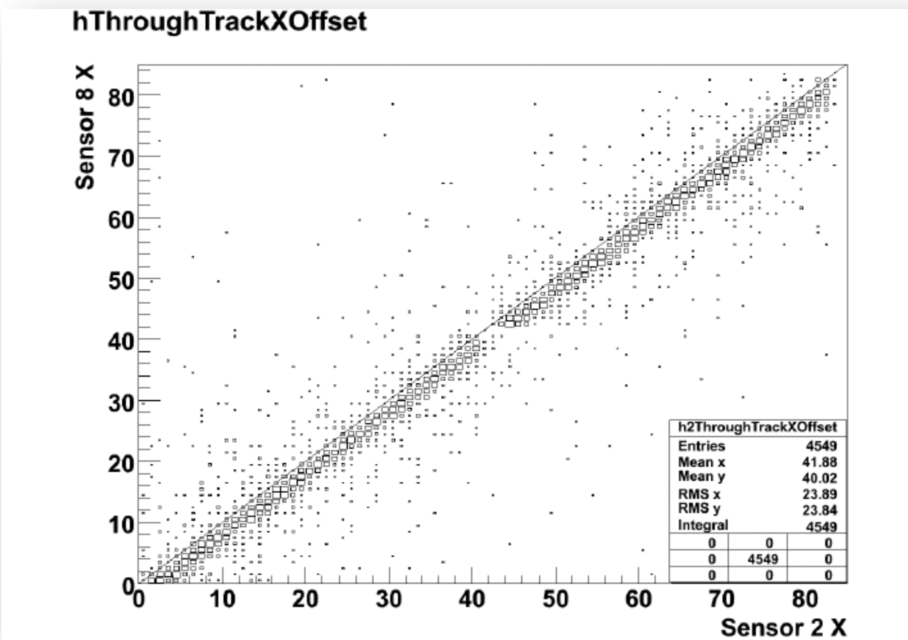


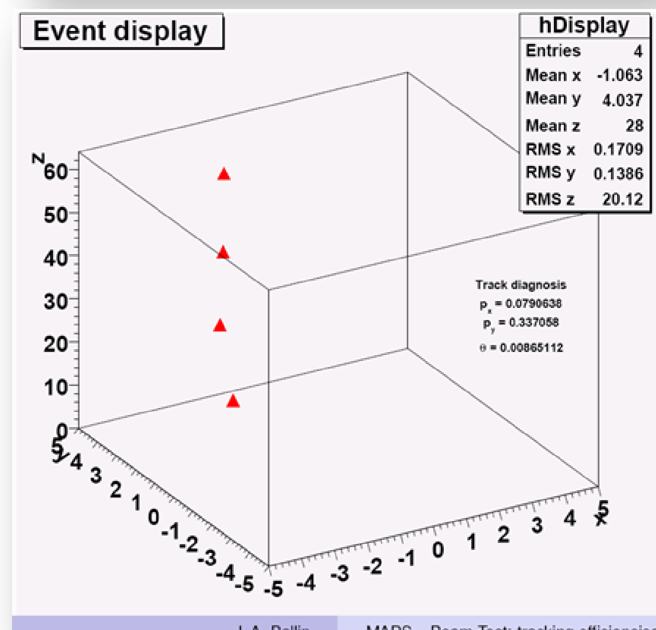
- Gain uniform to 12%
- Quad1 ~40% more gain than Quad0
- Quad1 ~20% better S/N than Quad0

Array of PreShape Pixels: Beam Test

- Took advantage of beam-test opportunity
  - very soon after receiving sensors
  - before long shut-down at DESY
- Proof of 4-sensor system
- Did see particles in multiple layers ☺
- Sensor pedestals were not trimmed at this time
  - Little usable data ☹





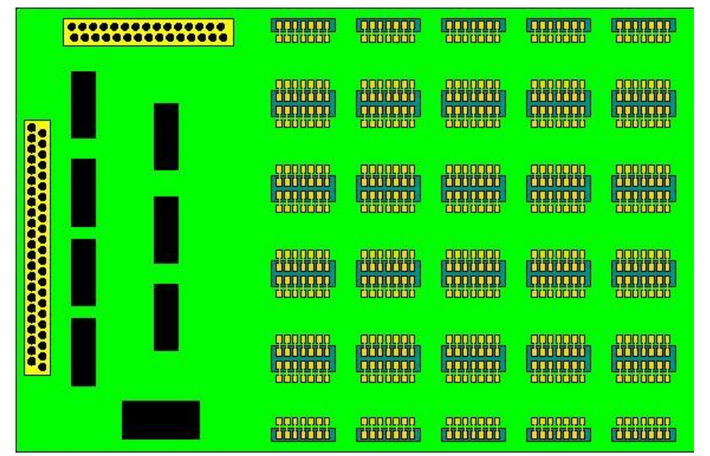


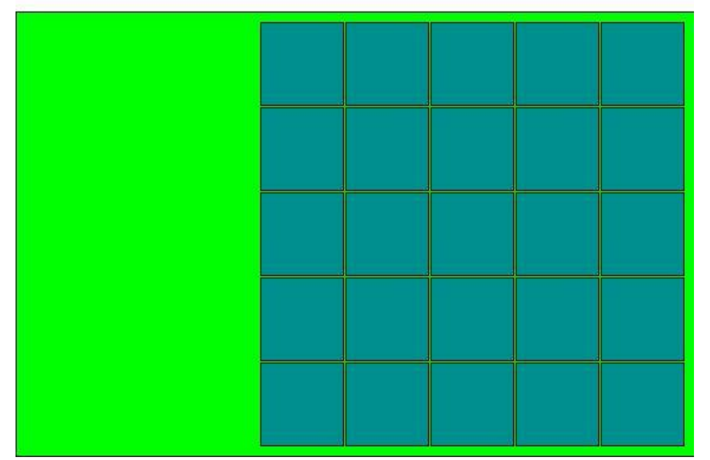
Immediate Future

- Characterisation of v1.0 is still ongoing
  - Automated laser tests
  - Cosmics stack
- Version 1.1 due back late September
  - One pixel variant selected (preShape quad1)
  - Upgrade trim adjustment from 4bits to 6bits
  - Compatible format: size, pins, pcb, daq etc.
  - Minor bugs fixed
  - Additional test pixels & devices
- Version 1.1 Full Characterisation
  - Automated laser tests
    - test pixels
    - array
  - Source tests
  - Cosmic tests
  - Beam test early 2009
    - With trims this time!

Long Term future

- Version 2 is part of a proposal submitted last week!
    - Larger sensor 25x25mm
    - Tiled to create a 125x125mm layer of pixels
        - Minimum dead space between sensors
        - Wire bonded through PCB holes
    - Stacked in 16 layers to ultimately prove the Digital ECAL concept





Conclusions

- First Sensor
  - Successful operation of highly complex pixels
    - See α & β radioactive sources
    - See laser injection of charge
    - See beam particles (albeit with low efficiency at the time)
  - Proved viability of the Deep P-Well for applying MAPS to particle physics
  - Selected a preferred pixel design to take forward
  - Some minor bugs
    - Low level data corruption
    - Some coupling between power domains generating false hits
- Revised Sensor
  - Uniform array of improved pixels
  - Full characterisation ready to go!
- Exciting future
  - Prove "Digital ECAL" concept using CMOS sensors